

Optimization of CCD Output Amplifier for SN Ratio Improvement

T. Nakano, N. Mutoh, and N. Teranishi
Microelectronics Research Laboratories NEC Corporation
1120, Shimokuzawa, Sagamihara, Kanagawa, 229, Japan

Abstract-We propose an optimization method for SN ratio improvement in a CCD output amplifier. Reset noise, thermal noise, and $1/f$ noise were taken into consideration in developing this method. As a result of calculating SN ratio dependence on the driver transistor dimensions (gate width and length) for the first stage amplifier, we found that shorter gate length and optimal gate width produce the maximum SN ratio. We also found that the reset noise reduction ratio in an external circuit strongly influences on the optimal gate width.

1. Introduction

In order to reduce chip size and to increase resolution in CCD image sensors, it is necessary to improve the SN ratio because reductions in image-cell size result in reductions in signal charge.

In CCD image sensors having floating diffusion output amplifiers, the dominant random noises are reset noise, amplifier noise, which consists of thermal and $1/f$ noise, and shot noise. Here, the dimensions for the first stage driver transistor in the output amplifier are extremely important parameters for improving the SN ratio, because the driver transistor is responsible for generating both amplifier noise and reset noise.

Several researchers have reported optimization of the first stage driver transistor [1,2,3]. However, they did not sufficiently consider the $1/f$ noise

component in the amplifier noise, because $1/f$ noise is hard to deal with. Nor did they consider the noise reduction ratio in the external noise reduction circuit, although the final SN ratio strongly depends on the noise reduction ratio.

We attempted to develop a method by which the dimensions of the first stage driver transistor in the CCD output amplifier could be optimized, so as to obtain the best possible final SN ratio. Such optimization takes the noise reduction ratio for an external noise reduction circuit into consideration.

2. Noises of CCD image sensor having floating diffusion output amplifier

Figure 1 shows a typical CCD output node structure and an external noise reduction circuit. The CCD output node consists of an on-chip three-stage source follower amplifier, a sense capacitor (a combination of a floating diffusion capacitor, a wiring capacitor and the capacitor of the first driver transistor of the amplifier), an H-CCD, and a reset transistor.

Signal charge transferred to the sense capacitor through the H-CCD is detected via the on-chip amplifier and the external noise reduction circuit, before being discharged to the reset drain by the reset transistor. In the CCD, this action is repeated periodically.

Reset noise is caused by thermal fluctuation in reset transistor, and is superimposed on the zero level of signal, when floating diffusion signals are reset.

This reset noise value is determined by the sense capacitor and the dimensions of the amplifier's first driver transistor, and is reduced by an external noise reduction circuit (CDS etc.), which samples the difference between the signal level and the zero level.

Amplifier noise can be reduced by designing the dimensions well, because the amplifier noise, which consists of thermal and 1/f noise, is dependent on the amplifier transistor dimensions. The dominant amplifier noise factor is the first driver transistor, because the dimensions of this transistor must be small enough so that the sense capacitance is small. Amplifier noise is changed by the external noise reduction circuit MTF.

Shot noise is based on the dark current in the photo-diode and V-CCD; it cannot be reduced by the external noise reduction circuit.

3. Optimal first driver dimensions for obtaining high SN ratio

As mentioned above, the reset and amplifier noises of the three types of CCD noise are related to the first driver dimensions, and the SN ratio is influenced by the noise reduction ratio.

We derived a formula which represents the relationship between the dimensions (effective gate width W, effective gate length L) and noise equivalent electrons for individual noise components, considering the noise reduction ratio for each noise component. Generally, the operating voltage of a source follower amplifier changes when the dimensions change. However, because the operating voltage is limited to maintain amplifier response linearity, we assumed that the operating voltages are fixed, so as to express 1/f noise as a function of dimensions only.

Because reset noise equivalent electron

Nrs is proportional to the square root of sense capacitance Cfj, which is proportional to gate area L·W, thermal noise is proportional to $\sqrt{L/W}$, 1/f noise is proportional to $\sqrt{1/(L·W)}$, and shot noise Nst and signal S are independent of L and W, individual noise and sense capacitance Cfj are described by

$$Cfj = \alpha \cdot L \cdot W + \beta \quad (1)$$

$$Nrs = A(1-x)\sqrt{Cfj} \quad (2)$$

$$Nth = B(1-y)\sqrt{\frac{L}{W}} \cdot \frac{Cfj}{q} \quad (3)$$

$$Nf = C(1-z)\sqrt{\frac{1}{LW}} \cdot \frac{Cfj}{q} \quad (4)$$

$$Nst = D \quad (5)$$

$$S = E \quad (6)$$

where A, B, C, D, E, α , and β are constants and x, y, and z are noise reduction ratios.

The SN ratio can be obtained as

$$S/N = \frac{S}{\sqrt{Nrs^2 + Nth^2 + Nf^2 + Nst^2}} \quad (7)$$

We regard the part of the function of L and W as N^2 .

$$N^2 = Nrs^2 + Nth^2 + Nf^2 \quad (8)$$

$$= \beta \cdot (1 - \alpha LW) \cdot (A'^2 + B'^2 L^2 + C'^2 + \frac{B'^2 L^2 + C'^2}{\alpha LW})$$

$$\text{where } A' = A(1-x)/q, B' = B(1-y)\sqrt{\alpha}/q,$$

$$C' = C(1-z)\sqrt{\alpha}/q$$

This formula indicates that a minimum N^2 exists, which is given under optimal W.

$$W_{opt} = \frac{\beta}{\alpha \cdot L} \cdot \sqrt{\frac{B'^2 L^2 + C'^2}{A'^2 + B'^2 L^2 + C'^2}} \quad (9)$$

Substituting Eq. (9) into Eq. (8), the following formula can be obtained.

$$N^2(W=W_{opt}) = \beta \cdot \left(1 + \sqrt{\frac{B'^2 L^2 + C'^2}{A'^2 + B'^2 L^2 + C'^2}} \right) \quad (10)$$

$$\{A' + \sqrt{(B'^2 L^2 + C'^2) \cdot (A'^2 + B'^2 L^2 + C'^2)} + B'^2 L^2 + C'^2\}$$

Because L is greater than 0, Eq. (10) increases monotonically with increase in L . This means that, when W is set to the optimal value, a smaller L improves the SN ratio, although $1/f$ noise component is proportional to $1/(LW)$. This is because $1/f$ noise can be kept almost constant because optimal W increases when L decreases according to Eq. (9). In this way, we can obtain the optimal dimensions to produce a maximum SN ratio.

4. Optimal dimension for typical noises and noise reduction ratio

In the previous section, we derived the optimal dimensions which produce the maximum SN ratio. In this section, we discuss the optimal dimension dependence on each noise reduction ratio. We regard one of the noise reduction ratios (x, y, z) as a parameter and regard the other noise reduction ratios and noises as typical values.

Figure 2 shows the relationship between SN ratio and effective gate width. One of the noise reduction ratios (x, y, z) is a parameter, while the other noise reduction ratios and noises are typical values, and L is 3.5 μ m. As can be seen in figure 2, the SN ratio strongly depends on the reset noise reduction ratio, and an optimal W that produces a

maximum SN ratio exists.

Figure 3 shows the relationship between SN ratio and effective gate length. One of the noise reduction ratios (x, y, z) is a parameter, the other noise reduction ratios and noises are typical values, and W is the optimal value. As can be seen in figure 3, the SN ratio is strongly dependent on the reset noise reduction ratio at typical gate length $L=3.5\mu$ m, and shorter gate length produces the maximum SN ratio.

Figure 4 shows the relationship between optimal W and the noise reduction ratio. As can be seen in figure 4, optimal W is strongly dependent on the reset noise reduction ratio when the actual reset noise reduction ratio is between 90% and 100%. We must take the reset noise reduction ratio into consideration when determining W .

5. Conclusion

In conclusion, the calculated SN ratio dependence on the driver transistor dimensions for the first stage amplifier reveals that a shorter gate length and an optimal gate width produce the maximum SN ratio, although the $1/f$ noise component is proportional to $1/(LW)$. It was also found that the reset noise reduction ratio in an external circuit strongly influences the optimal gate width.

As a result, when we design a source follower amplifier, this method prevents us from being confused by many dimension parameters, and makes it possible to design an amplifier with the maximum SN ratio.

Reference

- [1] P. Centen, IEEE Trans. ED, vol.38, no.5, pp.1206-1216, 1991.
- [2] T. Ozaki et al., IEEE Trans. ED, vol.38, no.5, pp.969-975, 1991.
- [3] J. Hyneczek, et al., IEEE Trans. ED, vol.39, no.11, pp.2497-2507, 1992.

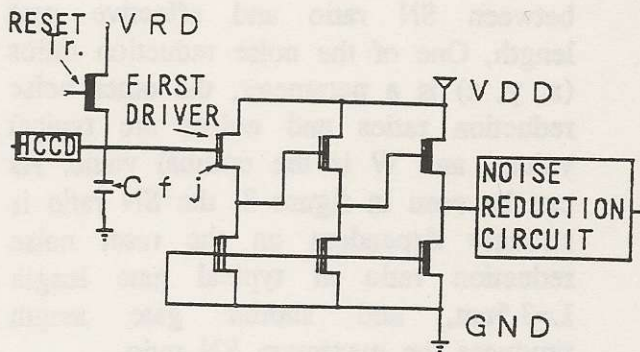


Fig.1 CCD output amplifier.

Driver transistor dimensions for the first stage in an amplifier are extremely important parameters for improving the SN ratio.

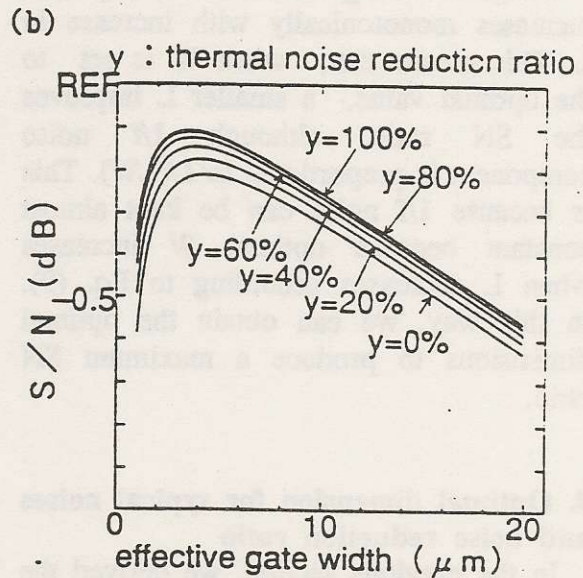
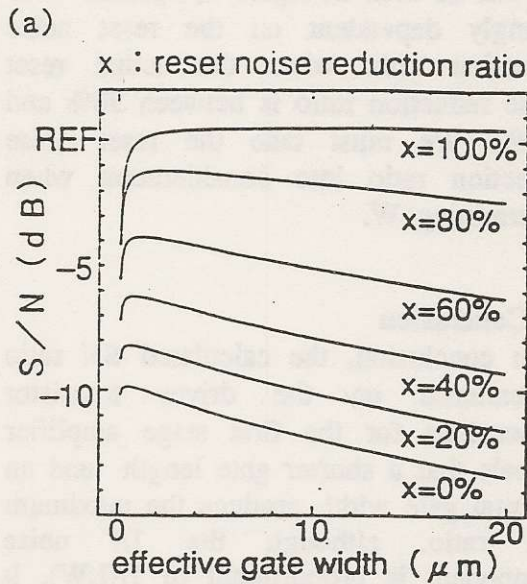
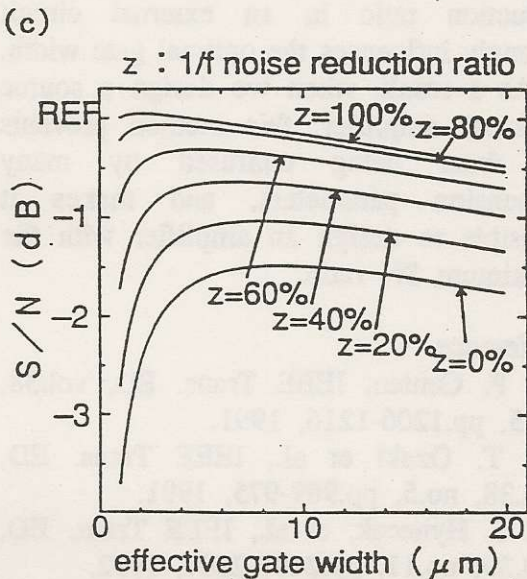


Fig.2 SN ratio dependence on noise reduction ratio as a function of effective gate width.

Parameters are

- (a) Reset noise reduction ratio.
- (b) Thermal noise reduction ratio.
- (c) 1/f noise reduction ratio.



There is an optimal effective gate width that produces the maximum SN ratio in the first driver dimension for the amplifier.

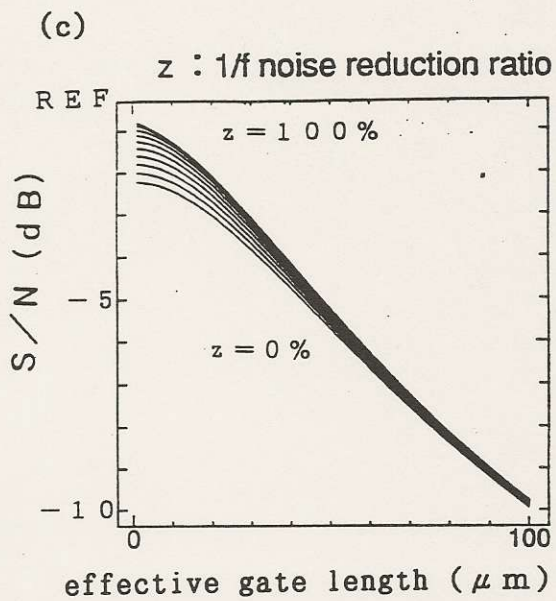
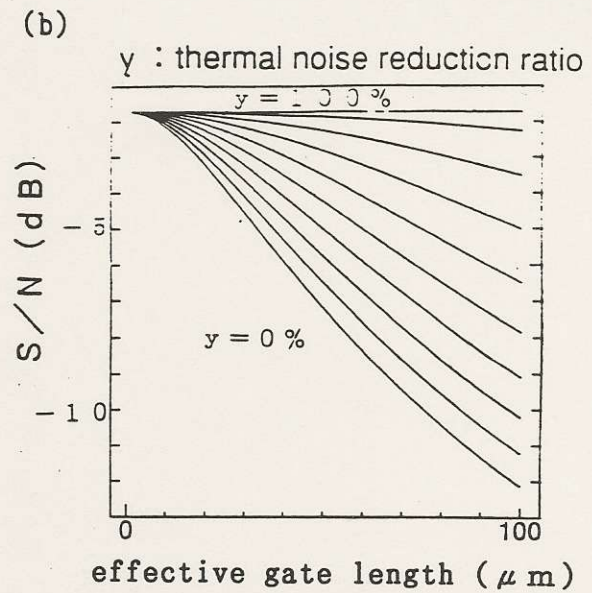
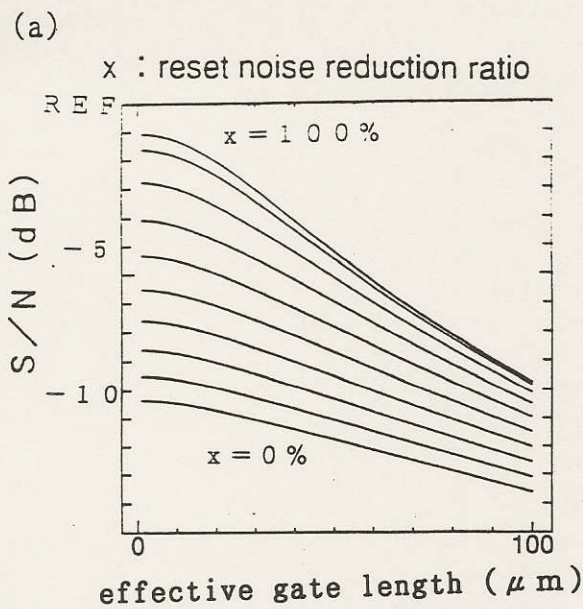


Fig.3 SN ratio dependence on noise reduction ratio as a function of effective gate length.

Parameters are

- (a) Reset noise reduction ratio.
- (b) Thermal noise reduction ratio.
- (c) $1/f$ noise reduction ratio.

Shorter gate length producing maximum SN ratio, when optimal W is given.

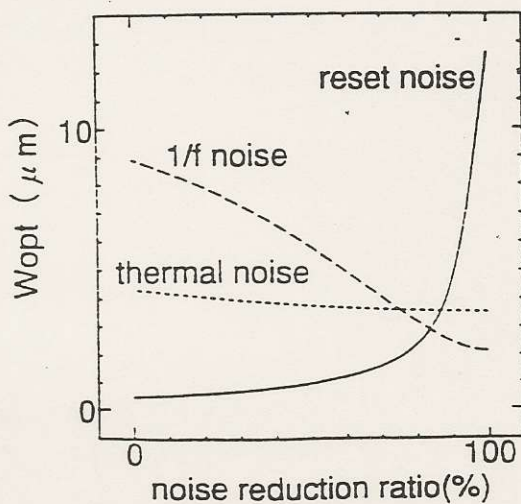


Fig.4 Relation between noise reduction ratio and optimal effective gate width W_{opt} .

Optimal W depends on noise reduction ratio, especially the reset noise reduction ratio, because the actual reduction ratio is between 90% and 100%.