High Speed CMOS Binary Active Pixel Image Sensor

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Abstract

A highly integrated active pixel sensor with on-chip 1 bit thresholding circuitry achieving an 8,000 frame per second data rate is a prototype for a larger sensor designed for a 1 Giga-bit per second data rate. The fabricated 4.3 mm x 4.5 mm prototype contains a 128 x 128 photo-diode array and outputs data on an 8-bit wide bus at 16 MHz. The chip contains a serial digital output port and a serial analog output port for low speed testing and characterization. The only required chip controls are a 16 MHz clock and mode control for selecting the output port. The on-chip digital control logic generates internal array readout timing and sequencing for the pipelined readout of thresholded array data.

The active pixel with a 31% fill factor is 16 x 16 μm and outputs data onto a shared column output. Per column output circuitry clamps pixel output data onto a capacitor and compares it to an externally applied threshold voltage. High speed readout of the previously captured row data through the chip 8-bit 16 MHz output bus occurs simultaneously as the columns for the next row are processed in parallel. The pipelined approach was found to generate unacceptably high noise levels. Output pad switching generates noise that couples through the substrate to the per column clamping circuitry upsetting the comparator inputs. The low noise non-pipelined design approach for the final 1024 x 1024 array design will contain a 128-bit 16 MHz output bus producing 1,000 frames per second.

The serial analog output port sensitivity is 2.3 μV/electron and has an output voltage referred dark current of 9 mV/second. Observed readout noise on the analog port is 15 - 25 mV. A peak quantum efficiency of 0.12 was lower than expected because of the use of a silicide on the photo-active regions. Observed on-chip noise from digital circuits affecting thresholded pixel data is greatly reduced through the use of external ground and power planes as well as separate chip power for digital and analog circuitry. The design and high speed test results for this 1 μm n-well CMOS sensor called the prototype Fast Optical Thresholding Oil Sensor (FOTOS) will be presented.

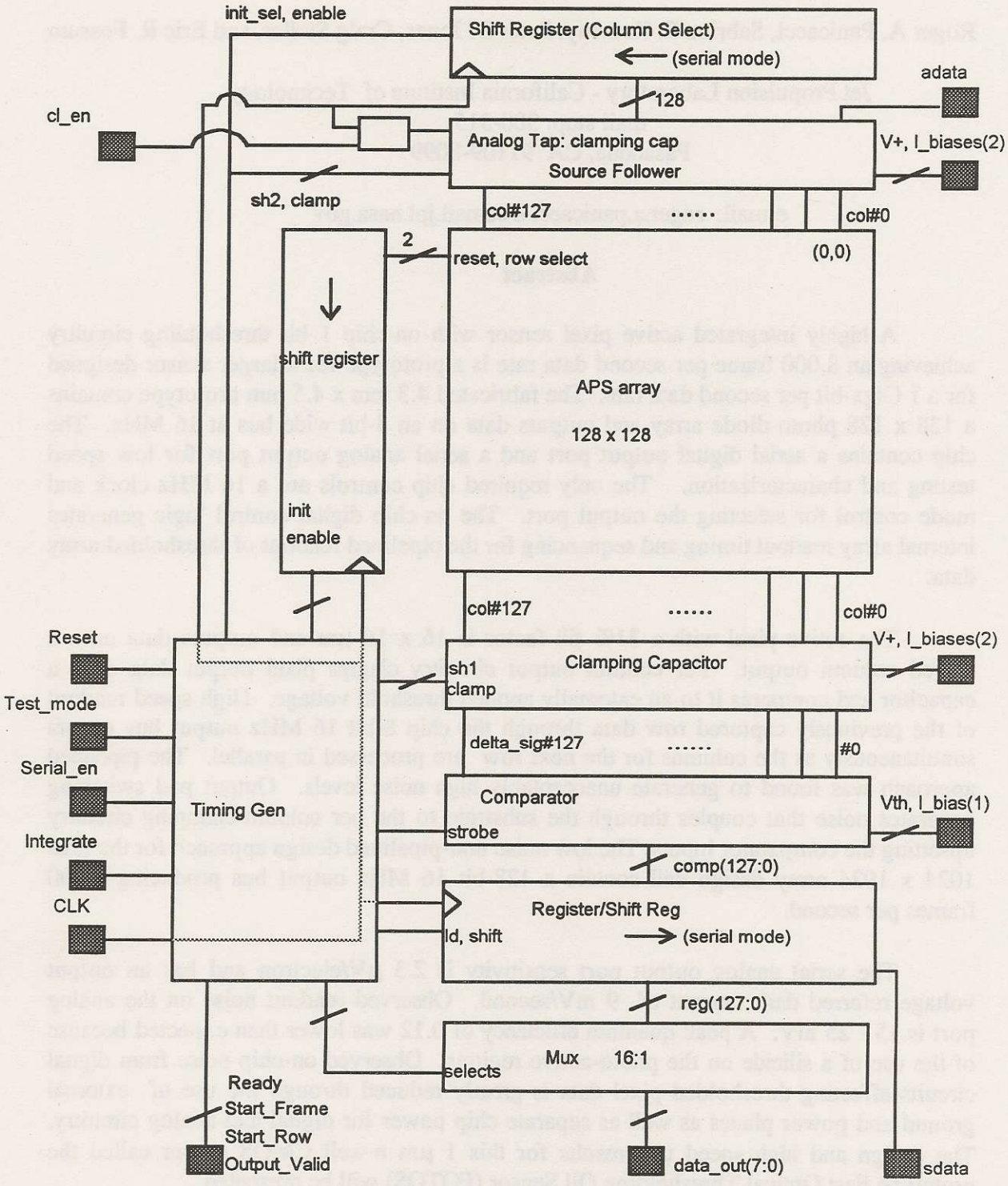
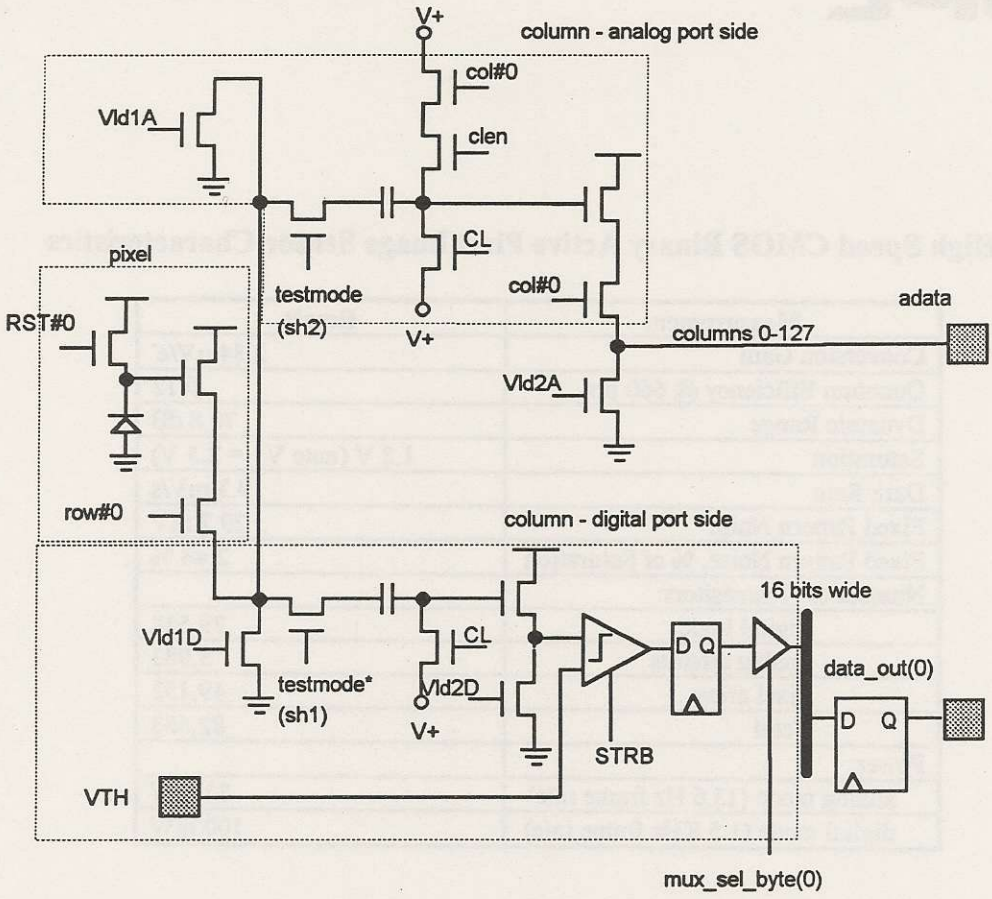


Figure 1. High Speed CMOS Binary APS Block Diagram



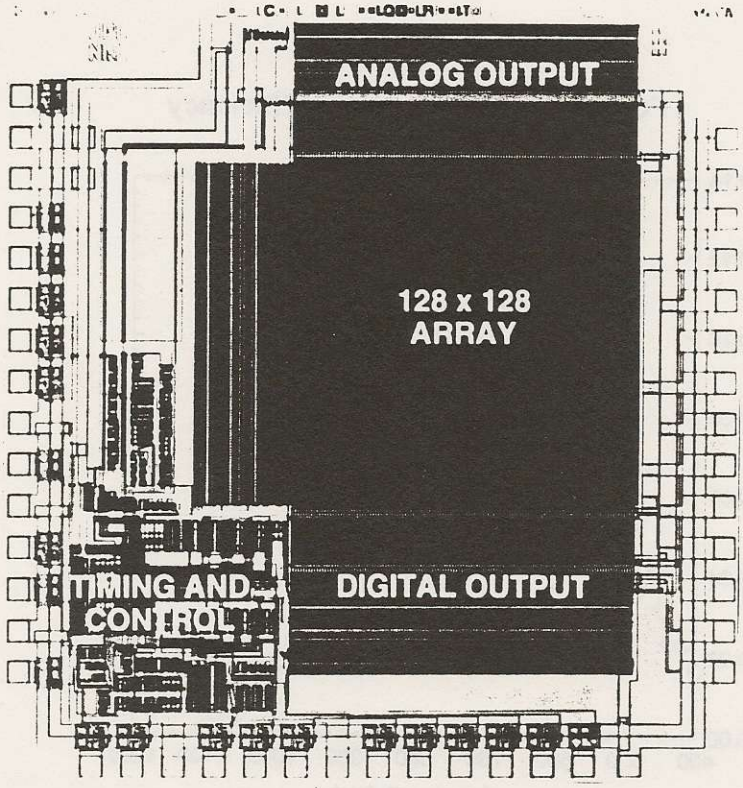


Figure 2. Circuit diagram of APS datapath and photograph of the FOTOS chip

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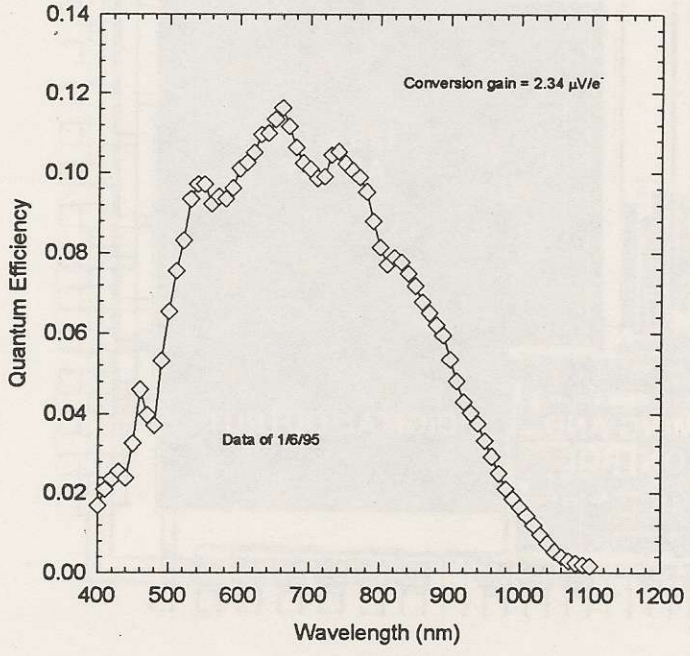
High Speed CMOS Binary Active Pixel Image Sensor Characteristics

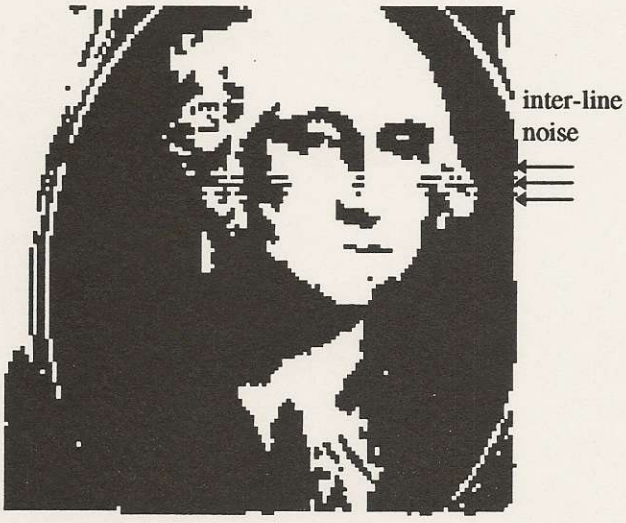
Measurement	Result
Conversion Gain	2.34 μV/e⁻
Quantum Efficiency @ 660 nm	0.12
Dynamic Range	70.8 dB
Saturation	1.2 V (note V+ = 2.5 V)
Dark Rate	9.3 mV/s
Fixed Pattern Noise	29.7 mV
Fixed Pattern Noise, % of Saturation	2.48 %
Number of Transisitors:	
digital logic	29,518
analog circuits	3,983
pixel array	49,152
Total	**82,653**
Power:	
analog mode (13.6 Hz frame rate)	32 mW
digital mode (1.5 KHz frame rate)	100 mW

FOTOS FS128-21 Quantum Efficiency

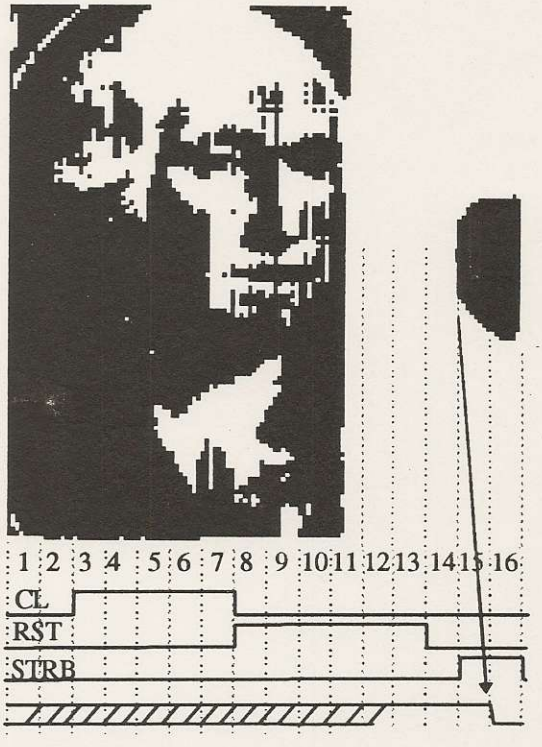


(a) Analog Port Image

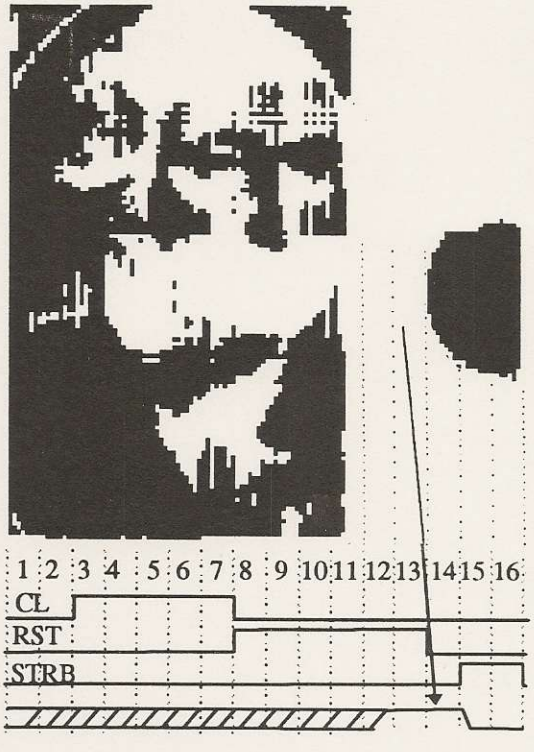
(b) Digital Parallel Port Image



(c) Output bus noise **not** timed to couple back to comparator input strobe edge.



(d) Output bus noise timed to couple back to comparator input strobe edge.



data output bus

Figure 3. (a) Analog port image, (b) digital parallel port image with inter-row noise coupling for center rows, (c) low light level image with a white-black test strip placed on top of dollar bill target to create a 1-0 transition on output bus, (d) same as (c) but with the test strip moved across target to create on-chip noise at the strobe edge, producing corrupted pixel data at the comparator.