

On-Chip Current-Mode Focal Plane Signal Processing for a CMD Image Sensor

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Abstract On-chip current-mode signal processing for a Charge Modulation Device (CMD) image sensor is under investigation. The design of current-mode circuits including a fixed pattern noise suppression circuit and a current-mode second-order incremental Σ - Δ analog-to-digital converter is described. Preliminary experimental results will be presented at the workshop.

I. INTRODUCTION

A Charge Modulation device (CMD) image sensor[1]-[3] is a type of active pixel image sensor [4]. It features one phototransistor per pixel, high speed operation, low power consumption and flexibility in implementing various readout schemes. Also, since its driving and readout circuits are implemented with CMOS, further integration of signal processing function can be easily achieved.

Current-mode signal processing, instead of the conventional voltage-mode signal processing, seems natural and appropriate for the CMD image sensors since the output of the CMD is in the current domain. Switched current (SI) circuits have gained considerable interest for analog sampled-data processing. Advantages of the SI technique over the voltage-mode technique include low power consumption, low supply voltage, potential for high speed operation, compatibility with standard CMOS process, and less real-estate.

Current-mode signal processing for the CMD image sensor is under investigation. An image sensor with on-chip fixed pattern noise (FPN) suppression and on-chip analog-to-digital conversion (ADC) is expected to increase sensor system performance, while reducing sensor system size, weight and cost [5]. In Section II, FPN suppression using a current copier cell is described. In Section III, building blocks for a current-mode over-sampling Σ - Δ ADC which is expected to achieve high resolution (≥ 10 bit) are described.

II. FPN SUPPRESSION WITH A CURRENT COPIER CELL

a. Current Copier Cell [6]-[7]

The principle of a current copier cell, also called a dynamic current mirror, is shown in Fig. 1. A single transistor M_M is combined with 3 switches S_X , S_Y , S_Z that are implemented by means of additional transistors, and a capacitor C . In the first phase (phase 0), M_M operates as the input device of a mirror, with its gate and drain connected to the input current source. When equilibrium is reached, capacitor C at the gate is charged to the gate voltage V required to obtain $I_D = I_0$. The value of I_0 is thus stored as a voltage across C . In the second phase (phase 1), M_M operates as the output device of a mirror, with its drain disconnected from the gate and connected to the output node. It sinks an output current I_1 , that is controlled by the same gate voltage V and thus is equal to I_0 .

b. FPN Suppression with a Current Copier Cell

FPN in a CMD image sensor is mainly caused by the offset current mismatch of the pixel CMD phototransistor. In order to suppress the FPN within an imager chip, the current copier cell was used [8]. Two current copier cells are assigned to each column. Current I_{RD} from a selected CMD pixel,

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which consists of the light dependent current I_{sig} and the offset current I_{off} ($I_{RD} = I_{sig} + I_{off}$), and current I_{RS} which is equal to I_{off} ($I_{RS} = I_{off}$) are memorized on the two current copier cells during the horizontal blanking period. The currents are readout in parallel during the succeeding horizontal period. An external analog circuit produces a subtracted signal, which should be FPN free.

Resulting FPN level of 0.5 % p-p for the saturation signal was reported[8]. This residual FPN is seen as vertical stripes.

A newly developed circuit configuration and pulse timing for FPN suppression is shown in Fig. 2. During ϕ_1 phase, current I_{RD} is memorized on the first copier. During ϕ_2 phase, current I_{RS} flows into the circuit while the first copier is in the copying phase (I_{RD} is output) and the additional current sink I_0 is connected to the common node of the both copiers. The current, $I_{RD} - I_{RS} + I_0 = I_{sig} + I_0$, is thus memorized on the second copier. I_0 prevents settling time degradation for small I_{sig} . During ϕ_3 phase, the second copier outputs the memorized current, $I_{sig} + I_0$, with I_0 flowing. The output current flowing into the load is I_{sig} . Thus, FPN can be suppressed. Note that the variation in I_0 does not generate FPN. A cascode transistor is used to reduce the output conductance effect.

III. CURRENT-MODE Σ - Δ ANALOG-TO-DIGITAL CONVERTER

a. Rationale for Σ - Δ ADC

Typical pixel data rate in scientific applications is around 100kHz and resolutions greater than 12 bits are required. High resolution with medium conversion speed is possible using oversampling technique [9].

Oversampling methods have recently become popular because they avoid many of the difficulties with conventional methods for A/D and D/A conversion. Conventional converters require high precision analog circuits. Oversampling converters, on the other hand, can use simple and relatively high-tolerance analog components. Though they require fast and complex digital signal processing stages, their robustness is suited for fast growing VLSI technology.

b. A current-mode second-order incremental Σ - Δ ADC [10][11]

Compared to the conventional voltage-mode approach which is usually a switched capacitor approach, the current-mode approach is expected to be faster and less sensitive to component variations. The critical elements in switched capacitor approach include the MOS op amp, which is the slowest analog component and the one most vital to conversion accuracy, and linear capacitors. Our current-mode approach uses no MOS op amps or linear capacitors. The main building block is a current copier cell which is described above.

A first-order Σ - Δ ADC requires 2^n cycles to perform a n-bit A/D conversion. A higher order Σ - Δ , built by incorporating additional error loops, can speed up the conversion. However, the addition of more than one integrator in the feedback tends to cause stability problems. This problem can be overcome by cascading two first-order stages resulting in an incremental Σ - Δ ADC topology [11]. Since it consists only of cascaded first-order stages, it is immune to loop instabilities. At the same time, compared to a first-order topology, it vastly improves the conversion speed. The number of cycles (m) needed for a k-th order Σ - Δ ADC to achieve n-bit resolution is given by

$$m = (k!2^n)^{\frac{1}{k}}$$

A block diagram of the current-mode second-order incremental Σ - Δ modulator is illustrated in Fig. 3. The algorithm for the second-order incremental ADC (for an integrator gain of unity) is given by

$$I_1(p) = pI_{in} - \sum_{i=1}^p a_i I_R$$

$$I_2(p+1) = p(p+1)I_{in} / 2 - \sum_{i=1}^p a_i (p+1-i)I_R - \sum_{i=2}^{p+1} b_i I_R$$

where p denotes p -th integration period, I_{in} the input current, I_R the reference current, I_1 , (I_2) the first (second) integrator's output, a_i (b_i) the first (second) comparator's output ("1" or "0"), respectively.

c. Building Blocks

c-1. Constant Feedthrough Current Copier Cell

One of limitations in the current copier cell is the charge injection due to switching. Figure 4 shows a current copier cell in which the feedthrough is expected to be independent of the input current levels. Constant feedthrough levels yield just an offset in the resulting digital data.

During the period when the pulses ϕ_1 and ϕ_a are ON, the value $I_{IN} + I_0$ is memorized on C_M . When the pulse is OFF, the clock feedthrough corresponding to δI_M , which depends on I_{IN} , is added on C_M . Thus, $I_{IN} + I_0 + \delta I_M$ is stored on C_M . During the period when the pulse ϕ_b is ON with ϕ_1 remaining ON, the value $I_0 + \delta I_M$ is memorized on C_C . When ϕ_b is OFF, the clock feedthrough corresponding to δI_C , which is constant under the condition of $I_0 \gg \delta I_M$ because of the constant I_0 , is added on C_C . Thus, $I_0 + \delta I_M + \delta I_C$ is stored on C_C . During the period when the pulse ϕ_2 is ON, the output current with constant feedthrough I_{OUT} given by

$$I_{OUT} = (I_{IN} + I_0 + \delta I_M) - (I_0 + \delta I_M + \delta I_C) = I_{IN} - \delta I_C$$

is obtained.

c-2. Integrator

An integrator consists of an n-channel and a p-channel CFT CCC. The n-channel copier acts as an accumulator and a p-channel copier acts as a memory, denoted Σ and M in Fig. 3, respectively. In the first phase, input current is memorized on an n-channel copier. In the second phase, the memorized current is copied on a p-channel copier. In the third phase, new input current and the copied current on the p-channel copier are added on the n-channel copier.

c-3. Comparator

Each comparator follows an integrating stage. A basic result of this is that the comparator's offset and noise are not as important as in other A/D configurations where comparators directly measure the analog input.

Fig. 5 shows a current comparator[12]. The first inverter operates as an integrating current-to-voltage converter.

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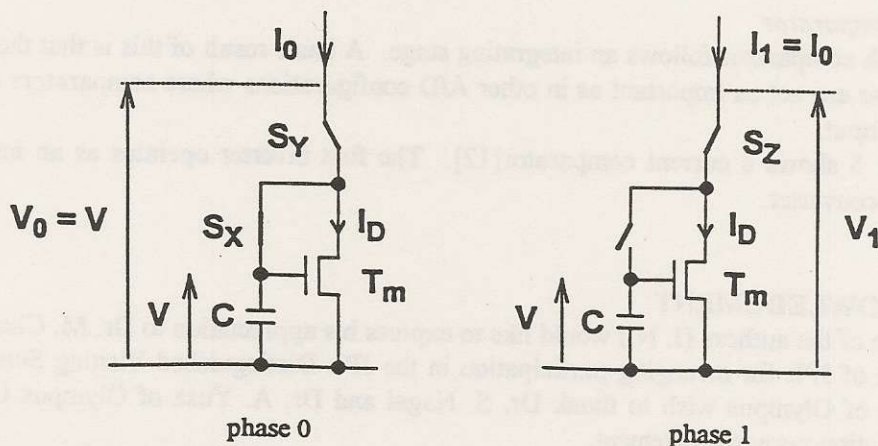
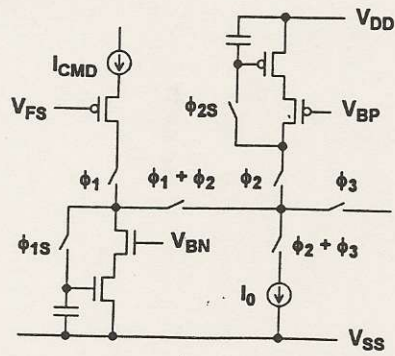
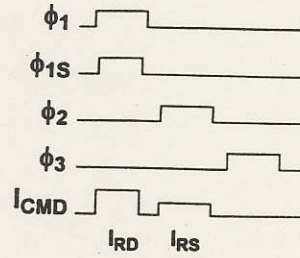


Fig. 1 Principle of current copier cell.

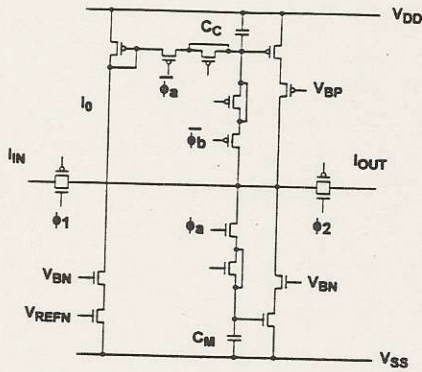


(a) circuit configuration

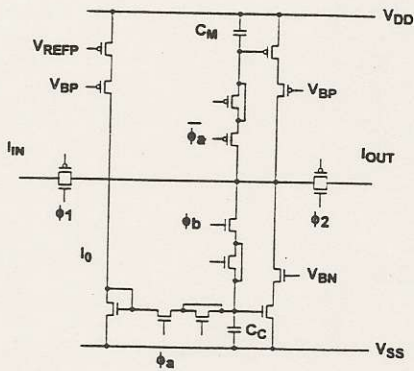


(b) pulse timing

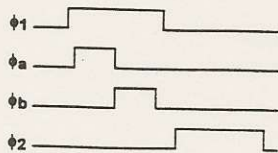
Fig. 2 Circuit configuration (a) and pulse timing diagram (b) for FPN suppression.



(a) n-channel copier



(b) p-channel copier



(c) pulse timing

Fig. 4 New current copier cell.

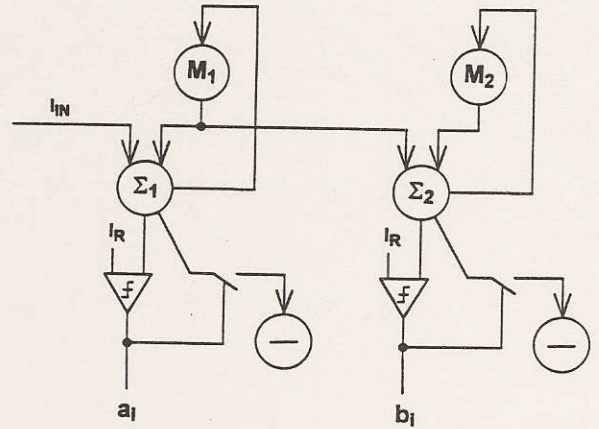


Fig. 3 Block diagram of the current-mode second-order incremental Σ - Δ modulator.

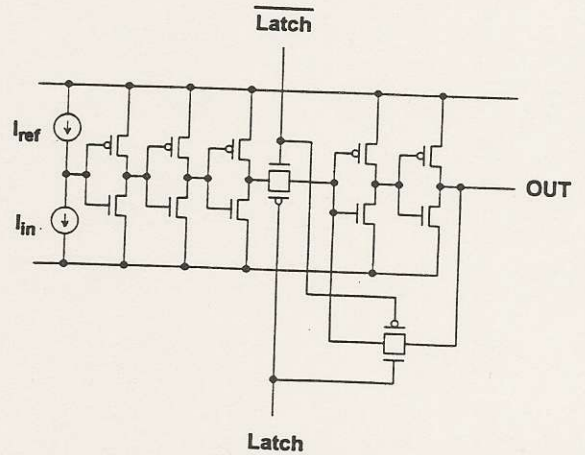


Fig. 5 Current comparator.