CMOS Active Pixel Sensor Array with Programmable Multiresolution Readout

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For a variety of image processing tasks, such as biological vision modeling, stereo range finding, pattern recognition, and progressive transmission of compressed images, it is desirable to have image data available at varying resolutions to increase processing speed and efficiency. The user can then obtain a frame of data at the lowest resolution necessary for the task at hand and eliminate unnecessary processing steps. Multiresolution image data is usually generated through an image pyramid approach implemented in software. Typically each image level in the pyramid is a low-pass filtered and down sampled version of the prior level, although block averaging and down sampling can also be used to generate the pyramid. Construction of the multiresolution pyramid is often the most computationally intensive and time consuming portion of the image processing task (e.g. hundreds of milliseconds for a 512 x 512 image).

In this work, a novel CMOS active pixel sensor (APS) array that can be read out at any user-defined resolution is described. Rather than build up and store an entire image pyramid and then choose the correct resolution, the imager itself is read out at the desired resolution utilizing block averaging. At each resolution less than the highest (readout of every pixel), a local average of the pixels is used to create the lower resolution "pixel" value. By combining the programmable windowing capability of APS arrays with multiresolution readout, tremendous savings in processing time can be realized. For example, a low resolution image (say 64 x 64 out of 512 x 512) can be read out and quickly processed to determine areas of interest. The subsequent frame can then be read out at a much higher resolution in the specific window which contains the area of interest.

The architecture for the multiresolution sensor consists of a 128 x 128 array of active pixels which are randomly accessed by row and column decoders. The multiresolution readout circuit, located at the bottom of the columns, consists of 3 banks of capacitors interconnected through a set of programmable switches and 3 shift registers which are used to store the digital patterns applied to the switching network. Operation consists of column averaging followed by row averaging. Pixel signals are sampled onto the first set of capacitors, which are then appropriately interconnected such that charge redistributes to perform signal averaging of n adjacent pixels, where n is the horizontal size (number of columns) of the block average (kernel). The kernel row averages are then sampled onto the first capacitor in each n-capacitor block of a row averaging bank of capacitors. The process is repeated for each row in the kernel and then the row averages are themselves averaged together through charge redistribution, resulting in the final block average. In order to perform correlated double sampling, two banks of capacitors are used for row averaging: one averages and stores the kernel reset levels while the other averages and stores the kernel signal levels.

The 128 x 128 multiresolution APS IC was implemented in a single poly, double metal, 1.2 μm process. The pixel utilizes a photogate structure, measures 19.2 x 19.2 μm^2, and has a 30% fill factor. Correlated double sampling to suppress pixel kTC noise, 1/f noise, and fixed pattern noise due to threshold voltage variations has been implemented on-chip. The array is designed to be read out at a video frame rate and is expected to have a dynamic range of 75 dB.

Multiresolution Image Processing

512 x 512

256 x 256

128 x 128

64 x 64
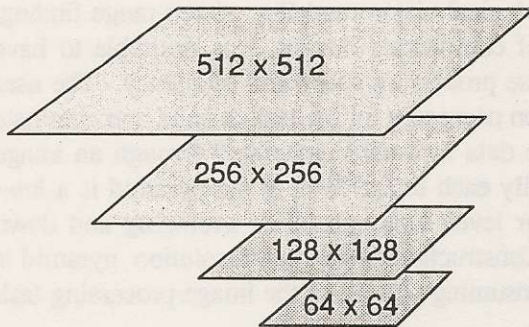
- Store raw image data
- Build a multiresolution image pyramid
  - » Low Pass filtering and downsampling by 2
  - » Block averaging and downsampling by 2

Problem: Computationally Intensive / Software Implementation Slow
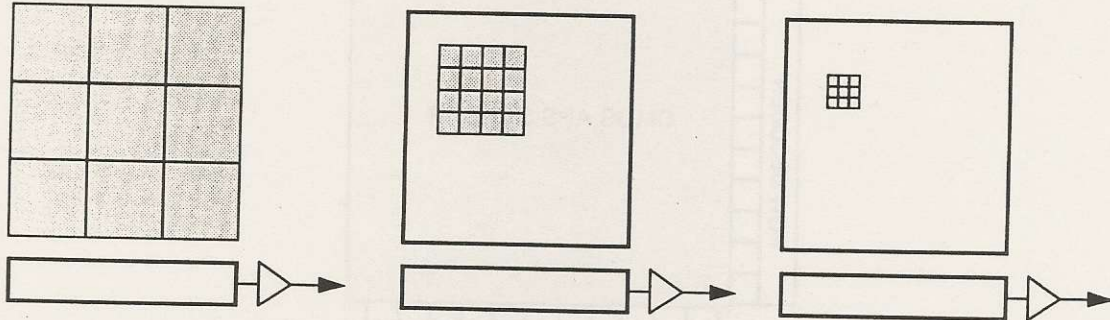e.g. Decomposition of 512 x 512 image into 5 levels on a Sparc 10 typically requires several seconds

Multiresolution Readout Sensor:
Pyramid Readout
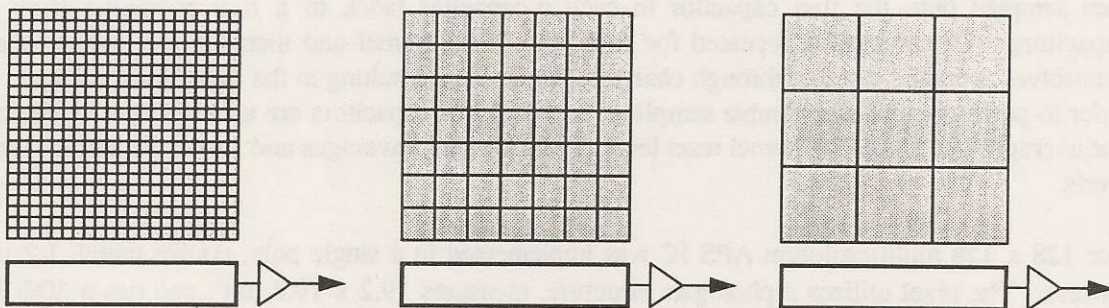
Read Out Array at Desired Resolution

128

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Multiresolution APS

Multiresolution Readout Sensor:
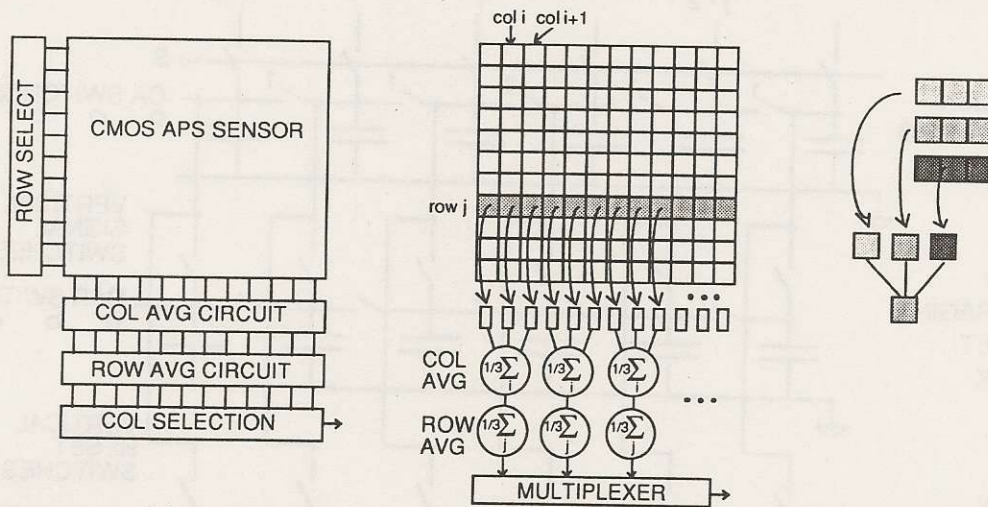# Window Readout

Applications

- Autonomous Navigation
- Pattern Recognition
- Target Tracking

- Progressive Transmission of Compressed Images
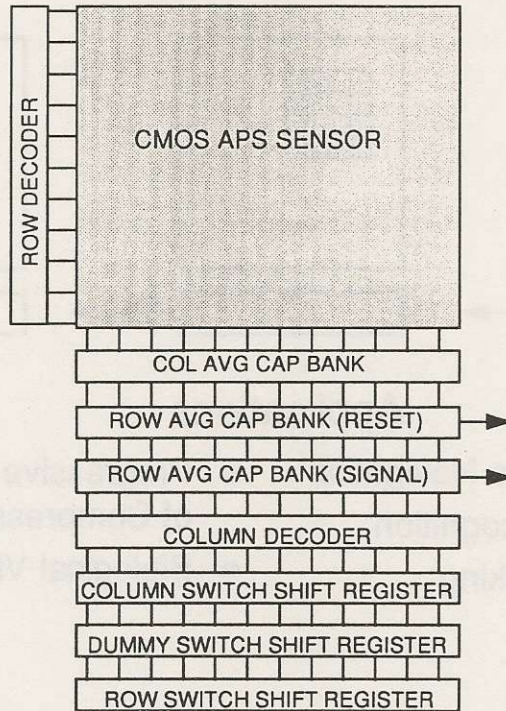- Biological Vision Modeling

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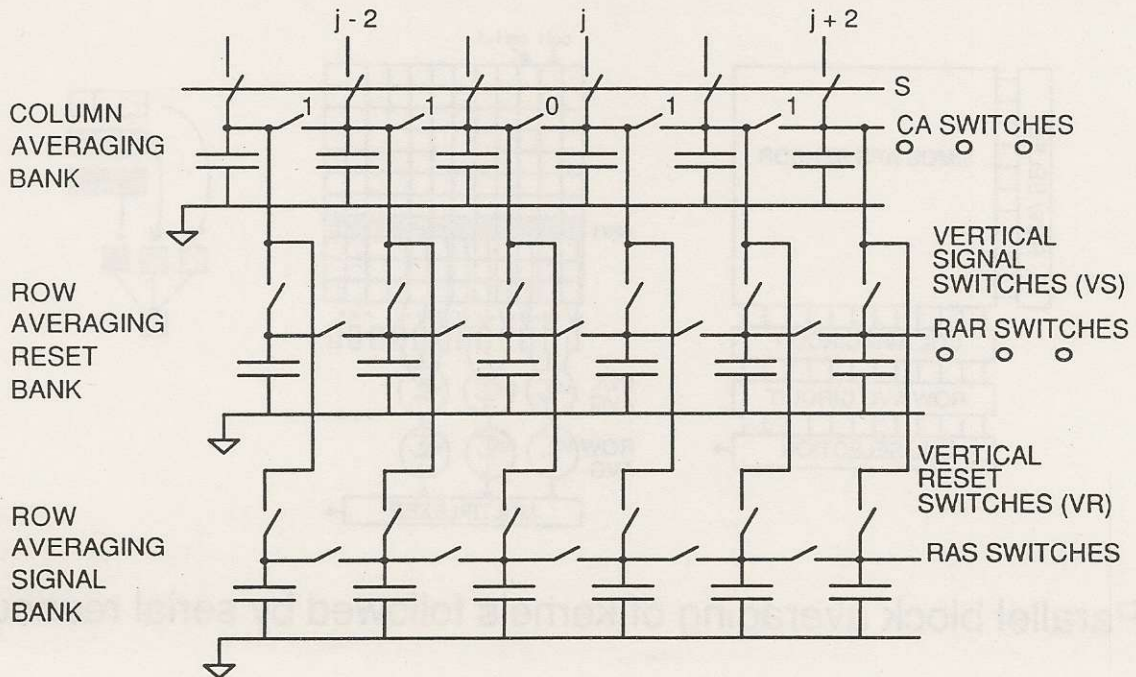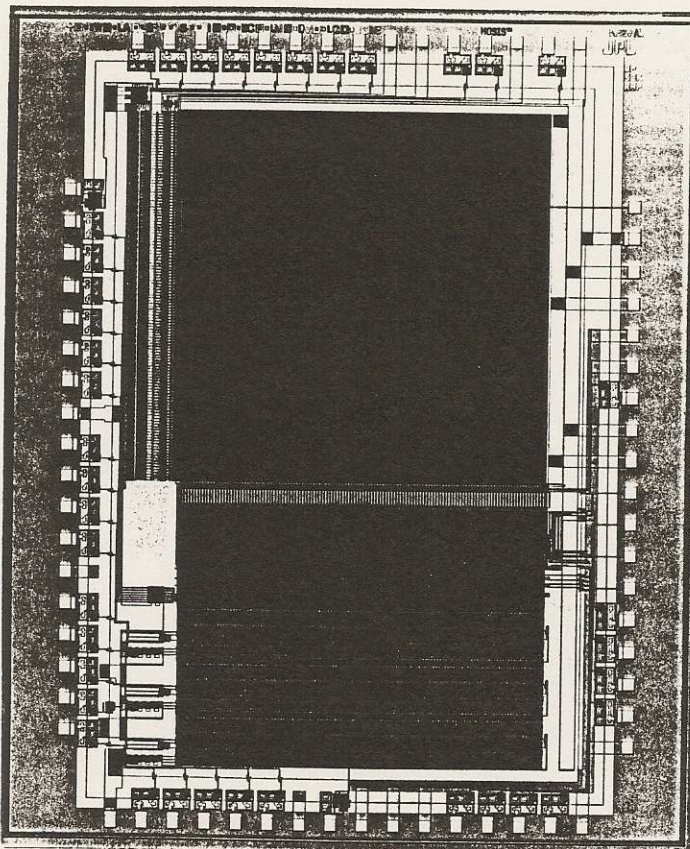
Multiresolution APS

Conceptual Column Parallel Approach

Parallel block averaging of kernels followed by serial readout

Passive Capacitor Implementation
Block Diagram

```
        ┌──┬──────────────────────────┐
        │R │                          │
        │O │                          │
        │W │   CMOS APS SENSOR        │
        │D │                          │
        │E │                          │
        │C │                          │
        │O │                          │
        │D │                          │
        │E │                          │
        │R │                          │
        └──┴──────────────────────────┘
        ┌─────────────────────────────┐
        │     COL AVG CAP BANK         │
        ├─────────────────────────────┤──→
        │  ROW AVG CAP BANK (RESET)    │
        ├─────────────────────────────┤──→
        │  ROW AVG CAP BANK (SIGNAL)   │
        ├─────────────────────────────┤
        │      COLUMN DECODER          │
        ├─────────────────────────────┤
        │ COLUMN SWITCH SHIFT REGISTER │
        ├─────────────────────────────┤
        │ DUMMY SWITCH SHIFT REGISTER  │
        ├─────────────────────────────┤
        │  ROW SWITCH SHIFT REGISTER   │
        └─────────────────────────────┘
```

Capacitor Banks

COLUMN AVERAGING BANK — CA SWITCHES

ROW AVERAGING RESET BANK — VERTICAL SIGNAL SWITCHES (VS) — RAR SWITCHES

ROW AVERAGING SIGNAL BANK — VERTICAL RESET SWITCHES (VR) — RAS SWITCHES

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Multiresolution APS

Specifications and Projected Performance

Array Size:	128 x 128
Pixel size:	19.2 μm
Process:	1.2 μm CMOS
Fill factor:	30 %
Programmable Window Size:	n rows x m columns
	n,m = 1,...,256 m>=n
Frame Rate:	
Full resolution	30 Hz (T_f = 33.3ms)
Lower resolution	$\{T_f/n + n(\text{small overhead})\}^{-1}$
e.g. 64 x 64	$\{33.3\text{ms}/4 + 4(8\mu s)\}^{-1}$ = 119.7 Hz
Dynamic Range:	75 dB