A Real-Time Digital Signal Processor for Use with the Interline Transfer Color CCD Imager

Shin-Shu Wang Chi-Hsin Wu Nai-Yun Hu

Image Processing Department
Industrial Technology Research Institute
Opto-electronics & System Lab.
Chutung, Taiwan, ROC

Abstract

This paper presents a newly-developed digital signal processor (DSP) for use with the interline transfer CCD image sensor. The single-chip CCD sensors samples the sense using a complementary color filter array (CFA) integrated on the surface of the sensor. The DSP accepts digitized image signals from the CCD sensor, performs luminance and chrominance signal processing, and outputs NTSC Y/C and digital CCIR601 signals.

Introduction

CCD imaging system are now extremely demanding in color image processing functions[1,2]. Digital processing allows accurate implementation of complex image processing algorithms, permitting various digital functions that were not available by using analog processing. A significant advantage of digital implementations is reliable, drift-free manufacturable systems with no adjustable components. A digital chip that accomplishes the necessary digital signal processing (DSP) has been developed. . The camera system employing a CCD image sensor and DSP is shown in Figure 1. Since the system is intended for low-cost applications, it is necessary to use a single CCD image sensor rather than three sensors, as is done in expensive professional color video cameras. Single-chip color CCD image sensors sample the scene using a color filter array fabricated on the surface of the sensor. Only a single color signal is sampled by any particular photosite. A DSP is used to perform black level compensation, scanning line buffering, edge enhancement, color separation, color matrixing, gamma correction , and output formatting in real time. All the processing circuits are finally implemented in a 8.9 mm x 8.9 mm die area and designed using 0.8 μm CMOS technology.

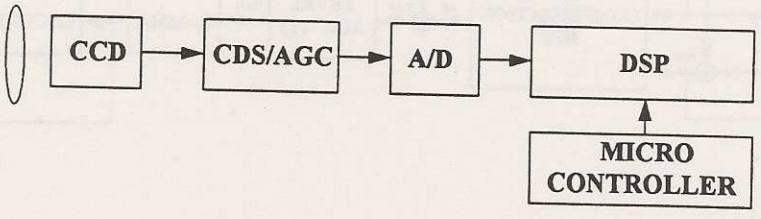

Figure 1 The camera system

Interline Transfer Color CCD Image Sensor

The CCD image sensor to be used is fabricated with a complementary color filter array shown in Figure 2. In the drawing, Mg, Ye, G and Cy respectively represent magenta, yellow, green and cyan color filter. That kind of low-cost

commercial CCD array is designed to support NTSC interlaced field format. This divides each frame into two fields, one with all the even pixel row, and the other with all the odd rows. The image sensor reads two pixels simultaneously, with a one pixel difference between even field and odd outputs. In this way, four added complementary color signals are dot-sequentially obtained from the CCD image sensor. These signals, passing through correlated-double-sampling (CDS, for noise reduction) and automatic gain control (AGC) circuits, are quantized by a 10-bit A/D converter and applied to DSP.

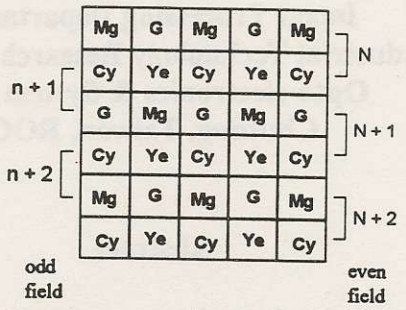

Figure 2 Complementary color filter array

The Digital Signal Processor

A block diagram of the functions performed by the DSP is shown in Figure 3. The first operation is an optical *black level clamp*. Because dark current of CCD image sensors is very dependent on the operating temperature, the clamping circuit is used to clamp the input video to the average sensor optical black reference value.

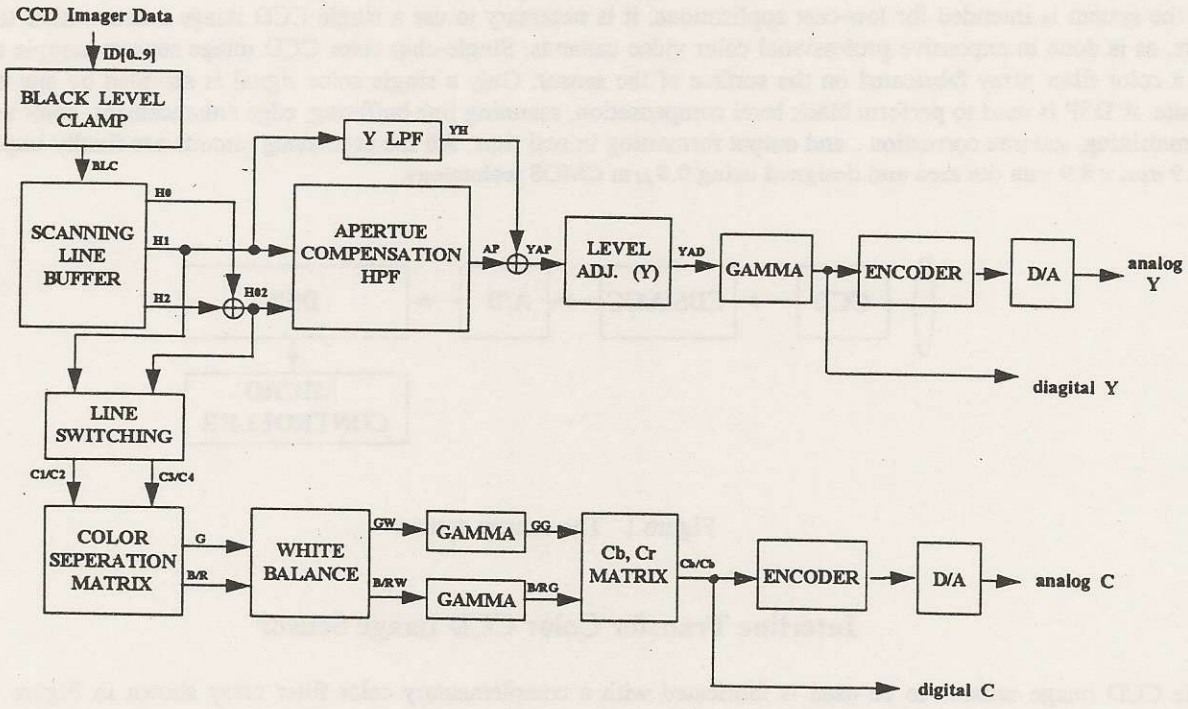

Figure 3 The block diagram of DSP

Scanning line buffer comprises two 1H digital line memory to store two horizontal scanning lines. Then following matrix circuit adds or subtracts the appropriate three-line signals to perform accurate luminance (Y) and chrominance (C) separation without "running" or color smearing, color noise or dot interference.

The four added complementary color signals obtained from CCD sensor are represented by C1, C2, C3 and C4:

$$C1 = Cy + G, \quad C2 = Ye + Mg$$
$$C3 = Cy + Mg, \quad C4 = Ye + G$$

where

$$Cy = g + b \qquad Ye = r + g \qquad Mg = r + b \qquad G = g$$

Line switching circuit is used to generate C1/C2 for one scanning line and C3/C4 signals for another in an alternative way.

In drder to obtain the primary color components R, G and B, the *color separation* calculation shown below can be used

$$CY = 2r + 3g + 2b = (C1 + C2 + C3 + C4) / 2$$
$$CR = 2r - g = (C2 - C1)$$
$$CB = 2b - g = (C3 - C4)$$

Then CR, CB signals will be fed into color LPFs to reduce bandwidth of color signal. The transfer function of this LPF is

$$H(z) = 0.125(1+z^{-4}) + 0.25(z^{-1} + z^{-3}) + 0.3125z^{-2}$$

Because data rate of chrominance signal is half that of luminance signal, the result output signals will be averaged and down-sampled. Finally, the R, G and B values can be obtained as follow

$$R = matr * CY + CR$$
$$G = matg * CY + CB$$
$$B = matb * CY - (CR + CB)$$

The coefficients matr, matg and matb values depend on the color-mixture functions of the phosphors in the display, and the responsivities of the RGB signals prior to calculation.

The *gamma* compensation circuits for R and B/G signals are the same as that for Y processing. The lower 9 bits of 10-bit input data are passed through ROM table and compressed to 8 bits.

CbCr matrix is used to generate unbiased value of Cb, Cr from Gamma-corrected RGB input signals according to CCIR 601

$$Cb = 0.512 (B - G) - 0.174 (R - G)$$
$$Cr = -0.083 (B - G) + 0.512 (R - G)$$

This enable the DSP to support 4:2:2 16-bit YCrCb output format.

White balance is the process of equalizing the R, G and B values for a neutral target under the existing illumination conditions. The gain values are computed by a microcomputer and loaded in into DSP via a serial interface.

Aperture compensation or "edge enhancement" is performed to increase the amplitude of signals corresponding to high horizontal and vertical spatial frequencies. A luminance detail signal pertaining to both vertical and horizontal edge information is computed by utilizing two high pass filters. This helps to compensate for the MTF falloff due to the camera lens and the phtosite aperture. The horizontal HPF and vertical HPF are given by

$$H_h(z) = (1+z^{-1})(-1+2z^{-1}-z^{-2})/2$$

Typically, very low level detail signals are not enhanced to prevent noise enhancement, mid-level detail are enhanced, while very large edge signals are not enhanced to prevent artifacts.

Encoder is designed specially for video cameras (imaging systems) requiring the generation of NTSC Y/C (S-video) video signals at a pixel clock rates of 14.318 MHz. Video timing control may be input with horizontal and vertical sync, or composite sync control signals. The interlaced YCrCb data is converted to YUV. The color difference signals are digitally low-pass filtered and modulated. Digital composite luminance and chrominance information each drives the 8-bit D/A converter that generates the analog Y and C video outputs.

Chip implementation

The chip has been designed and fabricated in a 0.8μm double-metal CMOS process. The chip details are given in TABLE 1. To minimize the chip areas, the signal processing has been carefully designed to eliminate the need for multipliers and to reduce the amount of memory element required.

Technology:	0.8μm CMOS
Gate count:	76K
Clock rate:	14.3MHz
Die size:	350mil x 350mil
Package:	100 pins QFP
Input data width:	10 bits
Output data width:	8 1bits

TABLE 1

Conclusion

Because the processing in DSP is arithmetic-intensive, the architecture is highly pipelined in order to achieve real-time video operation. This custom IC helps to develop compact and cost-effective CCD imaging product. This produces good picture quality and exhibits excellent sensitivity. In addition, The DSP is expected to be used in PC video applications.

Acknowledgment

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References

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