SIMULATION OF HIGH DENSITY CCD IMAGER STRUCTURES

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Simulation results are presented for design of high-density imager in the form of 3-phase BCCD with three layers of polysilicon gates. To assure a high charge transfer efficiency we have considered a process with a dual gate dielectric having 350Å SiO_2 layer covered with 650Å Si_3N_4 layer. 1-D process and device simulations were done using SUPREM III and PISCES IIB was used for 2-D device simulations.

I. 1-D Process and Device Simulation

The two major objectives of the process design of the high density CCD were to achieve a very high charge transfer efficiency and a maximum charge handling capacity. The BCCD channel was formed by arsenic and phosphorous bi-implantation on <100> p^- silicon wafer (6.0×10^{14} cm^{-3} boron uniform doped) as the substrate. The implant energy of arsenic is 120 KeV for arsenic, and 180 KeV for phosphorous in our simulation if not specified.

The maximum charge handling capacity per unit area simulated by SUPREM III has been determined by the difference of the full well potential (ϕ_{FULL}) to the surface potential (ϕ_{SURF}) as well as the minimum pinning potential of the adjacent wells. The determination of the full well condition is given ϕ_{FULL}>= MAX(ϕ_{PIN}, ϕ_{SURF})+10kT. Three CCD operation modes are defined for the simulation as follows:

Mode A: Operation with gate voltage swing, $\Delta V_G = 0 - V_{G(pinning)}$, where BCCD well is formed under zero biased gate, and the pinning biased gate forms the barrier between the wells.

Mode B: Operation with gate voltage swing, $\Delta V_G = V_\sigma - V_{G(pinning)}$,. In this case the full well of zero biased gate is determined by the pinning potential under the adjacent wells, but the maximum charge capacity is obtained by applying a positive optimized gate voltage (V_σ) to obtain the $\phi_{SURF} \cong \phi_{PIN}$.

Mode C: Operation with gate voltage swing, $\Delta V_G = V_G(+) - 0$, where zero biased gates form the barriers, while the well is created under the gate with a positive voltage V_G (+).

The results of 1-D process and device simulations by SUPREM III are illustrated in Figs. 1 to 7.

Typical doping profile of the BCCD implant in the form of arsenic and phosphorous on p-type Si substrate, and of the BCCD cross-section are shown in Fig.1. 1-D potential profiles for the BCCD doping of Fig.1 are shown in Fig. 2(a) and (b) for the three operating modes A, B, and C defined above.

Optimization of the charge handling capacity (CHC) in electrons/μm^2 as function of arsenic (x) and phosphorous (1-x) for total dose (1) of 1.3×10^{12} cm^{-2} is shown in Fig. 3. Inspection of this figure shows that for operation in mode A the CHC increases with the increase of arsenic up to the dose of As = 7.5×10^{11} cm^{-2}. At this point the condition for full well charge signal changes from being determined by the pining potential under the adjacent gate to that of the surface potential under the storage gate. Further increase of arsenic results in reduction of CHC. However, operating in mode B results in increase of CHC as phosphorous increases from 5.5×10^{11} cm^{-2} to 1.3×10^{12} cm^{-2}, as the optimized positive gate voltage $V_{G,Max} = V_\sigma$ is increased from 0V to 1.9V.

The effect on CHC as function of the arsenic implant dose and the total implant dose is illustrated in Fig. 4, for modes A and B.

Charge handling capacity, operating voltages, maximum electric field of the Si/SiO_2 interface are shown in Figs 5, 6, and 7 respectively, as function of total BCCD implant dose for a fixed As implant dose

of 1.0×10^{12} cm^{-2}. As illustrated in Fig. 5, CHC increases in proportion to the total dose for modes B and C. However, for mode A the CHC increases at a considerably slower rate with the total BCCD implant dose. Inspection of Figs 5 and 6 shows that while mode C has only 5 to 10% smaller CHC than mode B, it requires about 40% smaller clock voltage swing ΔV_G.

The maximum allowable N-type doping of the BCCD channel is expected to be limited by the electric breakdown at the SiO_2/Si interface, as shown in Fig. 7. For low doped silicon, the critical field strength is approximately 3.0×10^5 V/cm[1]. However, published values of BCCD charge handling capacities imply that considerably higher electric field can be tolerated at Si-SiO_2 interface of highly doped BCCDs. In SiO_2 and Si_3N_4, the critical strength is depended on the quality of the material as well as its thickness. For thin oxide and nitride layer, the critical strength is approximately 1.0×10^7 V/cm[1]. Our simulations showed that, the maximum electric field in SiO_2 and Si_3N_4 are lower than 2.5×10^6 V/cm as the total implant dose reaches 6.0×10^{12} cm^{-2}.

II. 2-D Device Simulation

The main objective of the 2-D simulation by PISCES IIB was to determine the effect on charge handling capacity due to reduction of gate length and channel stop width in order to optimize the high density BCCD structure. The doping profiles obtained from the 1-D process simulation were included in the 2-D structure with a 0.7 lateral diffusion ratio. The implant doses of arsenic and phosphorous were both chosen as 6.5×10^{11} cm^{-2}.

The charge capacity of the CCD channel as a function of the gate length is shown in Fig 8. An inspection of this figure shows that, the maximum CCD channel charge capacity increases significantly from about 3,300 electrons/μm^2 to 5,000 electrons/μm^2 as the channel length changes from 1.0 to 2.0 μm. The maximum charge handling capacity changes slowly (from about 6.000 to 6,300 electrons/μm^2) as the gate length increases from 3.5 to 5.0 μm.

Figure 9 shows the minimum electric fringing field and the maximum electron transit time of the BCCD operating in modes B and C as a function of gate length. Inspection of this figure shows that the maximum electron transit time is less than 1 nsec for the gate length less than 4.0 μm. On the other hand, the BCCD has a larger electric fringing field and smaller electron transit time for operation in mode C.

The effectiveness of the surface-channel CCD (SCCD) region as a channel stop between BCCD channel is illustrated in Fig 10. This figure shows the barrier heights of an empty well and a full well corresponding to a 3.0-μm wide BCCD channel operating in modes B and C. Inspection of Fig. 10 shows that when the nominal channel stop width (w) is 1.0 μm and more, the channel stop barrier height becomes greater than 10 kT/e.

Our 2-D simulation results also indicate that the effect of the lateral diffusion of the BCCD implant does not affect charge handling capacity which can be determined with 99% accuracy assuming channel width corresponding to the implant mask dimensions.

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[1] S.M. Sze, "Physics of Semiconductor Devices", Second Edition, *John Wiley & Sons, Inc.*, New York, 1981.

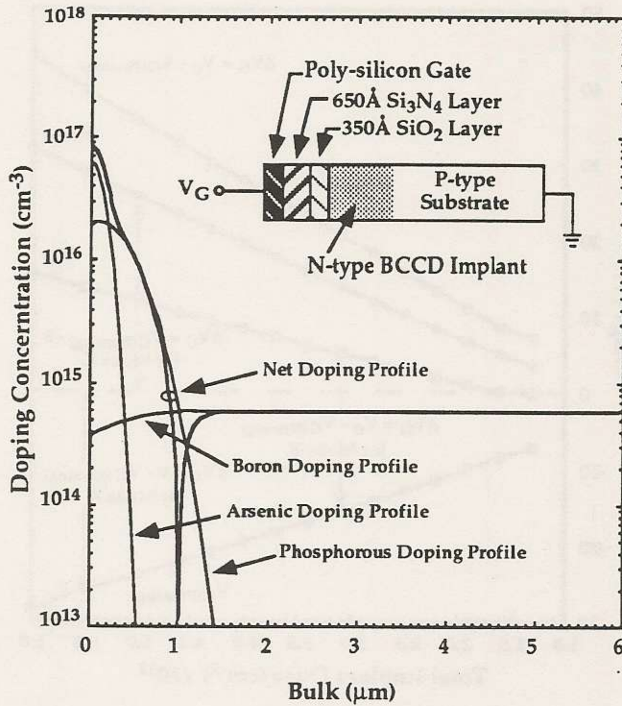


Fig. 1 Doping profile of BCCD implant (As = 1.05×10^{12} cm^{-2} @120KeV, P = 1.15×10^{12} cm^{-2} @ 180KeV) on P-type substrate (B = 6×10^{14} cm^{-3}).

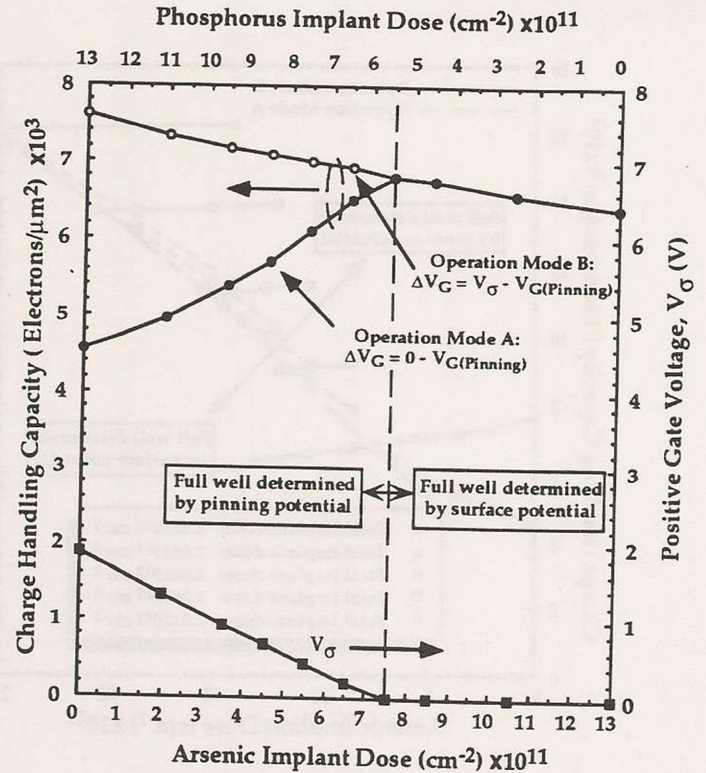
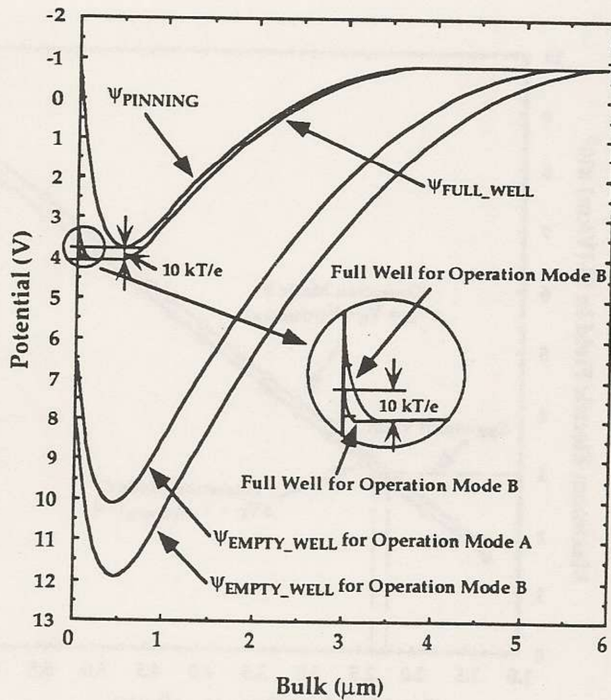
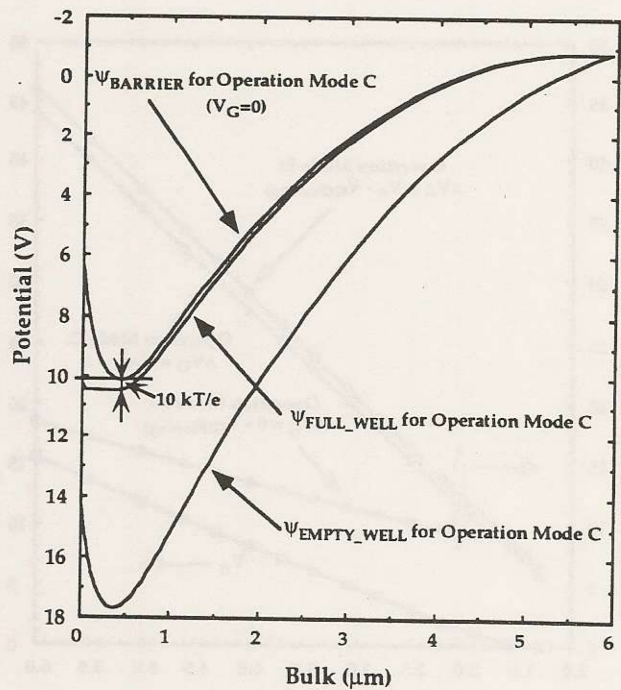


Fig. 3 Charge handling capacity (CHC) and optimized positive gate voltage $V_{G,Max} = V_\sigma$ as function of As and P implant doses for a total dose of 1.3×10^{12} cm^{-2}.



(a)



(b)

Fig. 2 Potential profiles of BCCD doping shown in Fig.1 for three operating modes: Mode A for $\Delta V_G = 0 - V_{G(pinning)}$ and Mode B for $\Delta V_G = V_\sigma - V_{G(pinning)}$ shown in (a) and Mode C for $\Delta V_G = V_G(+) - 0$ shown in (b).

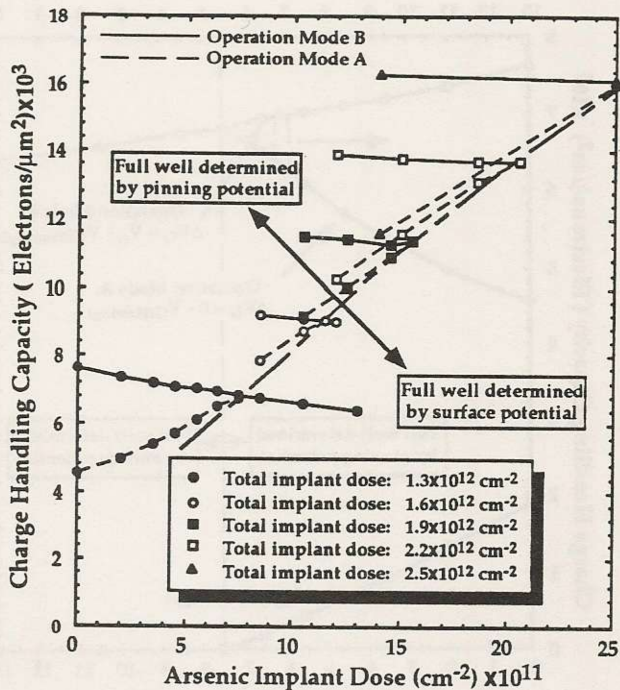


Fig. 4 CHC as function of As dose for total implant dose in the range from 1.3 to 2.5 x 10^{12} cm $^{-2}$. Solid lines indicate operation mode B for $\Delta V_G = V_\sigma - V_{G(pinning)}$ and dash lines are for mode A where $\Delta V_G = 0 - V_{G(pinning)}$.

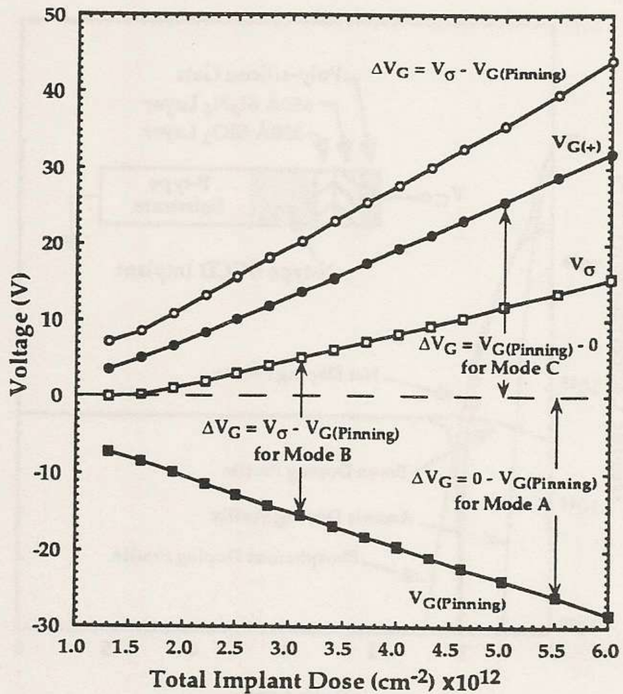


Fig. 6 Gate voltage swings, $\Delta V_G = V_\sigma - V_G$(pinning) and $\Delta V_G = V_G(+) - 0$, optimized positive voltage V_σ, and pinning gate voltage V_G(pinning) as function of total dose for BCCD operations and implants described in Fig.5.

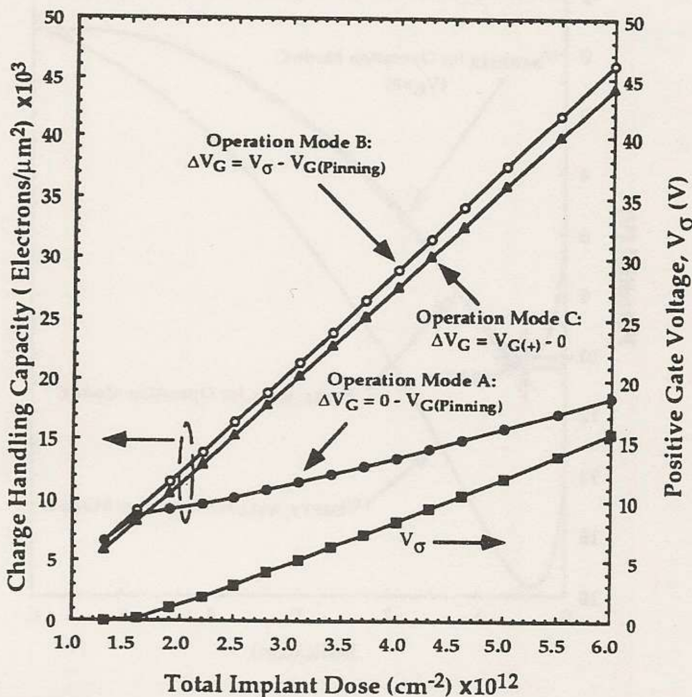


Fig. 5 CHC as function of total implant dose (with As dose of 1x10^{12} cm $^{-2}$) for operation with $\Delta V_G = V_\sigma - V_G$(pinning), for $\Delta V_G = 0 - V_G$(pinning), and for $\Delta V_G = V_G(+) - 0$.

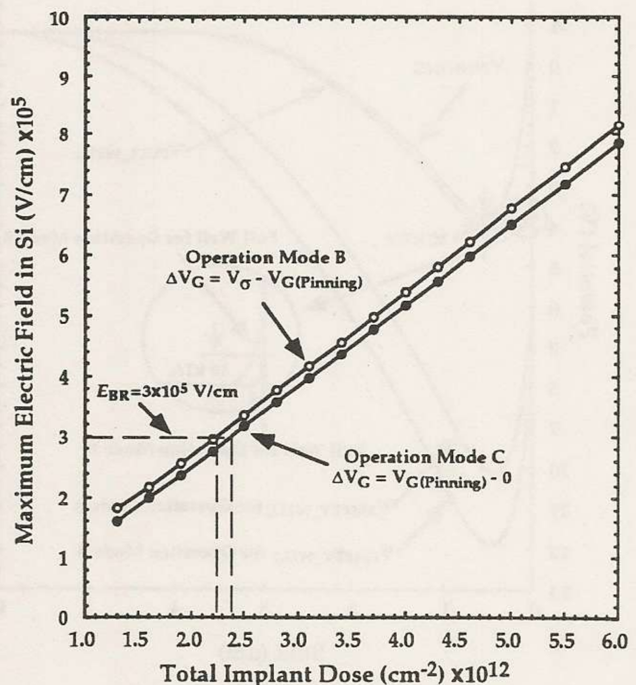


Fig. 7 Maximum electric field at the Si/SiO2 interface as function of total BCCD implant dose.

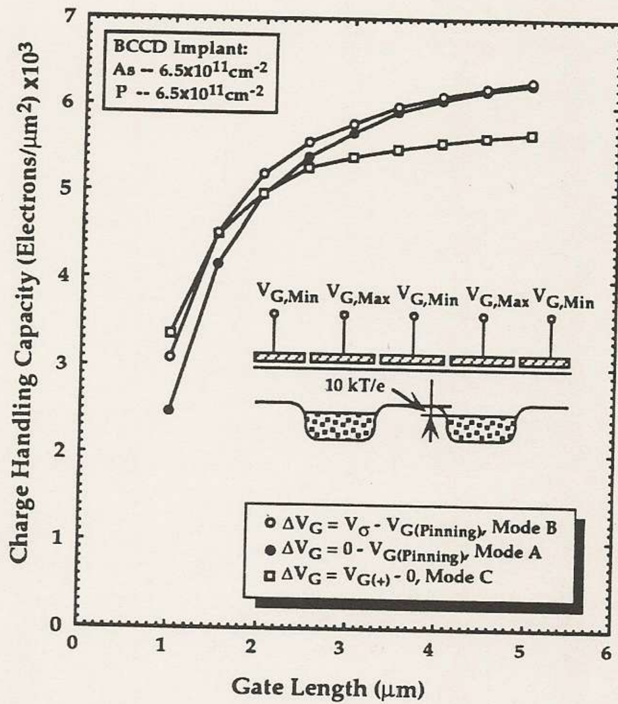


Fig. 8 CHC as function of BCCD gate length.

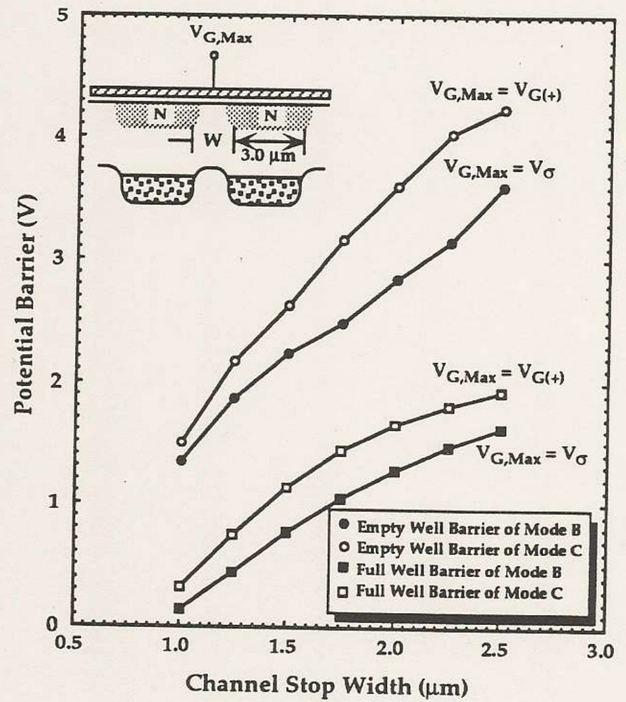
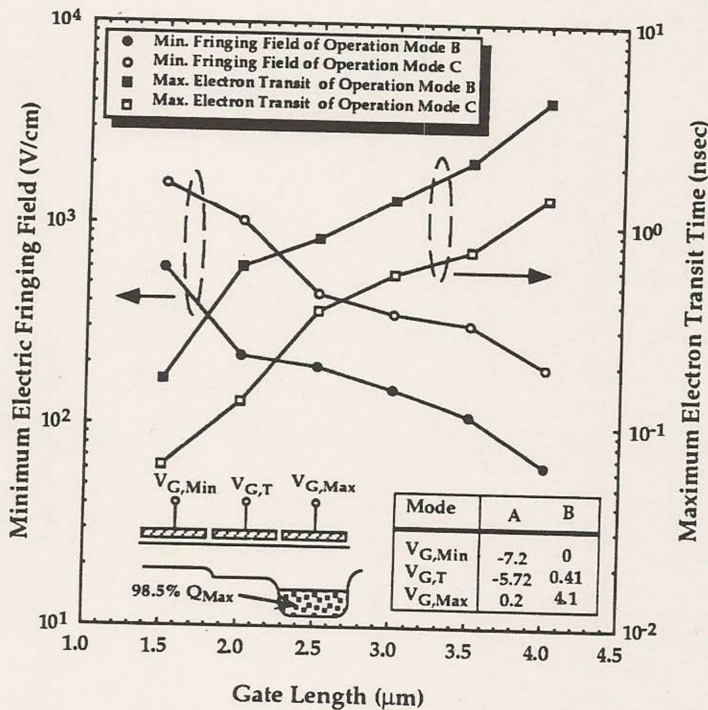


Fig. 10 Potential barrier between SCCD channel stop and empty and full potential well for a 3-um wide BCCD channel shown as function of channel stop width (w) for BCCD implant of As - 6.5×10^{11} cm^{-2} and P - 6.5×10^{11} cm^{-2} and P-type Si substrate with Boron concentration of 6.0×10^{14} cm^{-3} .



Mode	A	B
$V_{G,Min}$	-7.2	0
$V_{G,T}$	-5.72	0.41
$V_{G,Max}$	0.2	4.1

Fig. 9 Minimum electric fringing field under the transfer gate with clock voltage V_{GT}, and maximum electron transit time, when the receiving well with gate voltage $V_{G,Max}$ has 98.5% of full well charge signal, are shown as function of BCCD gate length.