# 3-Dimensional Numerical Analysis of Deep Depletion Charge-Coupled Devices

M. H. Kim†, J. Fothergill† and A. Holland‡

† Department of Engineering, University of Leicester, Leicester, LE1 7RH, U.K.
‡ Department of Physics and Astronomy, University of Leicester, LE1 7RH, U.K.

**Abstract:** A 3-D numerical simulation of a buried-channel CCD (Charge Coupled Device) with a deep depletion has been performed to investigate its electrical and physical behaviours. Results are presented for a deep depletion CCD (EEV CCD12, JET-X CCD) fabricated on a high-resistivity (1.5 kΩ-cm), 65 μm thick epi-layer, on a 550 μm thick $p^+$ substrate, which is optimised for X-ray detection. Accurate predictions of potential minimum and barrier height of a CCD pixel, as a function of mobile electrons, are found to give good charge transfer. Depletion depth approximation, as a function of gate and substrate bias voltage, gave average errors of < 6 % compared with the results estimated from X-ray detection efficiency measurements. The result obtained from the transient simulation of signal charge movement is also presented based on 3-dimensional analysis.

## 1. Introduction

Charge-coupled devices play an important role for Astronomical imaging in orbiting X-ray telescopes [1,2]. Optical properties of a CCD are determined by the absorption mechanism of the incident radiation into the silicon. In Astronomy CCDs, some signal loss mechanism limits a realisation of the state-of-art device for X-ray detection over the energy of 0.1-10 keV. Quantum efficiency loss at X-rays below 1 keV occurs through absorption into the passivated dielectric layers and the electrode structure as dead layers. For X-rays above 4.5 keV, most of the X-ray interactions are in the depletion layer, field-free region or $p^+$-substrate region due to the large absorption depth. In the latter 2 cases the charge diffusion will result in poor spatial resolution due to the lateral diffusion. Thus, for a good charge detection of X-rays below 1 keV and above 4.5 keV and for long wavelength IR (>750 nm), a CCD pixel should have an optimised structure with a thinner dead layer for efficient low energy X-ray detection and a thicker photo-sensitive layer for high energy X-ray detection. For the latter requirement, a high-purity bulk or substrate material is employed [3-5]. The "JET-X CCD" [3,6] is such a device under development by the X-ray astronomy group of the Leicester University in collaboration with EEV Ltd for the JET-X instrument on the Soviet mission Spectrum-X.

The "EVEREST" simulation package, a semiconductor device simulator, was chosen to investigate its electrical properties. This uses a finite-element method with an adaptive mesh technique for higher accuracy, lower computation time and efficient memory usage. Local efficient mesh refinement allows rapid variation of the charge current near the interfaces between the diffusion contact and input/output gate, and between the input gate and the first gate electrode, as well as in the fast changing distribution of channel doping etc. Finite-element simulation is achieved using discretised semiconductor equations, resulting in the transformation of non-linear equations into linear ones. This allows the geometry and mesh size to be more flexible than the finite difference technique.

A 3-D CCD simulation was performed to obtain an accurate potential profile, including mobile signal charge, in which Poisson's equation and the current-continuity equation are simultaneously solved. Some results for the potential minimum and barrier height for efficient charge storage and transfer are demonstrated. Different depletion edges obtained from the simulation are compared with those estimated from the detection efficiency measurements. We also present a result of signal charge movement obtained from a time-dependent simulation.

## 2. Description of the Device

A front-illuminated CCD was developed for the Joint European X-ray Telescope (JET-X) to optimise the X-ray detection properties of the energy range of 0.3 to 10 keV (42 Å to 1.2 Å) [3]. The

device consists of an array of 768×1024 27 μm square pixels, fabricated on a high-resistivity (1.5 kΩ-cm), 65 μm thick epi-layer on a 550 μm thick $p^+$ substrate. This device has a large area of 20.7×27.6 $mm^2$, which is divided into two identical sections for imaging and storage. Thus, it can be operated in frame transfer or full area imaging. It has a wide column buried channel (BC) implant to increase depletion depth, but with an additional narrow BC implant to confine charge during transfer and to increase radiation hardness [2].

In Figure 1, a device schematic is illustrated, where a phase 3 electrode structure was modified to improve the spectral response at X-rays below 1 keV by thinning one electrode, and the depletion depth and field-free layer are ~ 35 μm and ~ 30 μm, respectively. The pixel is covered with 3 poly electrodes, 2 of 5 μm and one thin extended poly-silicon electrode of 17 μm to improve a low energy transmission. The device includes both wide and narrow channels in which the former is used for deep depletion, while the latter is for radiation hardness.

**3. Results and Discussion**

An electron charge distribution extracted on a potential minimum in the channel is shown in Figure 2, where the first (or second) phase electrode with a gate length of 5 μm was applied to 10 V, while the second (or first) and third remained unchanged at 0 V. To transfer the whole signal from one storage region to the next without surface charge trapping, the potential difference between the surface interface and channel minimum point should be > 10 kT/q in order for the mobile charge not to jump the barrier for the duration of the transfer process.

In Figure 3, the potential distributions are shown in the direction normal to the surface as a function of mobile carrier densities, which are extracted at the center of gate 1. In this static simulation an input circuit consisting of an input diffusion contact and input gate was used to control a charge injection. The flat band voltage was assumed to be zero. In curve 1 the potential well is filled with < 50 electrons, resulting in a potential difference of 1.1 V (although it is typically 1 V) between the potential minimum and the surface potential. The potential minimum was reduced by 0.9 V compared with that under no mobile charge which corresponds to 13.5 V. For curve 2 the potential well is filled with 19136 electrons, and then the resulting barrier height is reduced to 0.6 V. In this case the potential minimum is located at 0.38 μm below the surface. A full well of electrons is shown in curve 3, where the potential barrier is dropped to 0.28 V and the location of the minimum is much closer to the surface (0.25 μm away from the $Si/SiO_2$ interface). The potential difference between two channels is then 0.2 V, as shown in Fig. 4, which can ensure good charge confinement in the channel 2. The channel isolation regions located at both end of the channel width are not shown in Fig. 4. The static charge carrying capacity for this full well condition in the supplementary channel 2 then corresponded to 56160 electrons.

In order to estimate the depletion depth of a JET-X CCD, different operating voltage conditions as a function of the substrate bias have been used in the simulation. We have analysed different depletion edges to give some comparisons with the estimated edges from the detection efficiency measurements. They have been estimated based on the number of the pixels for each event due to the splitting of charge during the charge collection process. For this work McCarthy [6] found the corresponding quantum efficiencies, from which different depletion depths have been estimated. For the present work three different depletion edges were classified: strong-field, light-field and zero-field depletion edges. Their definition and extraction method have been presented in Reference [7].

In Table I, the results obtained from the simulation as a function of substrate bias were summarised and compared with those from the measurements, where $x_s$, $x_l$, and $x_0$ are represented as strong, light and zero-field edges, respectively. In this simulation only a wide (phase 3) gate was applied to 10 and 12 V. For the depletion edge with the strong field the simulated results demonstrated that their increment as a function of the gate and substrate bias voltage was approximately linear, resulting in an average error of approximately 5 % compared with the results estimated from X-ray measurements. Also, the zero-field depths simulated provided very good prediction for analysis of the photo-sensitive volume. They involved only approximately 2.3 % as an average error [7]. Also, a comparison of the total depletion depth $x_l$ obtained from 3-D and 1-D analysis as a function of the substrate bias showed that the overestimated channel potential computed in 1-D analysis gave rise to a little higher depletion depth.

A result of the transient simulation for signal charge movement within the potential well in the channel 2 is illustrated in Fig. 5, where Poisson's equation and current-continuity equations have been solved with electron and hole carriers resulting in a very high accuracy but long computation time. A three-phase JET-X CCD with low charge packet was simulated as a function of time, in which a clock

period of 0.5 μs with rise and fall times being 0.1 μs and 0.15 μs, respectively was employed with a clock voltage swing of 8 V. A charge transfer process between phase 1 and phase 2 is shown in Fig. 5. The mobile charge is filled under the gate 1 at 0.4 μs, as shown in Fig. 5a, and is started discharging at 0.5 μs, as illustrated in Fig. 5b, whilst in Fig. 5c, the charge transfer is completed under gate 2 at 0.65 μs. From this transfer process it was seen that the charge packet size transferred under the gate 2 was slightly increased compared to that under the gate 1. This is probably because some of fixed charge impurity into the potential well underneath the phase 2 remained not neutralised and was added into net charge packet. For charge transfer with a large charge packet the effect of the fixed impurity on the leakage contribution can be neglected.

*TABLE I*

| | Depletion Depth (μm) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{g3}$ = 10 V, $V_{g1}$ = $V_{g2}$ = 0 V | | | | | $V_{g3}$ = 12 V, $V_{g1}$ = $V_{g2}$ = 0 V | | | | |
| $V_{ss}$ | Simulated | | | Estimated | | Simulated | | | Estimated | |
| | $x_e$ | $x_l$ | $x_0$ | $x_e$ | $x_0$ | $x_e$ | $x_l$ | $x_0$ | $x_e$ | $x_0$ |
| 0 | 34.9 | | 65.7 | | | 35.7 | | 65.6 | | |
| 1 | 34.3 | 42.9 | 65.8 | 30.9 | 64.6 | 34.9 | 43.2 | 65.6 | 33.8 | 66.3 |
| 2 | 33.4 | 42.1 | 65.1 | 30.6 | 62.8 | 34.3 | 42.8 | 66.0 | 32.3 | 64.4 |
| 3 | 31.3 | 41.1 | 65.0 | 30.7 | 63.4 | 33.5 | 42.1 | 68.2 | 31.4 | 65.0 |
| 4 | 27.8 | 35.8 | 65.0 | | 63.8 | 31.5 | 41.1 | 65.0 | 30.5 | 64.0 |
| 5 | 26.5 | 35.7 | 65.0 | 29.2 | 65.5 | 28.0 | 36.7 | 65.0 | 30.0 | 63.4 |

<Comparisons between different depletion edges simulated and edges estimated>

## 4. Conclusions

Buried channel CCDs with the deep depletion have been analysed to provide an optimised condition for charge storage and transfer, as well as to estimate different depletion edges for the charge detection efficiency in the device. A maximum charge capacity has been found for the narrow channel by considering the potential distribution as a function of mobile charge. Analysis for the depletion depths of JET-X CCDs have been successfully performed, showing good agreement with the depths estimated from X-ray detection efficiency measurements. It is evident that the "EVEREST" simulation package is a very useful tool, which led us to study the optimisation work of BC CCDs.

## 5. Acknowledgements

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**<Figure Captions>**

Figure 1: Cross section of a JET-X CCD structure.

Figure 2: The isometric electron distribution on a potential minimum. The x-direction displays the channel width and y-direction represents the channel length.

Figure 3: Potential minimum variation, as a function of mobile charge, along the direction normal to the surface: curves 1,2 and 3 are described in the text.

Figure 4: Potential difference between channels 1 and 2 under a full well condition along the transverse direction.

Figure 5: The electron charge transfer: (a) charge stored under gate 1 at t= 400 ns; (b) charge transfer from gate 1 to gate 2 at t=500 ns; (c) a complete charge transfer under gate 2 at t=650 ns. The magnitude is shown as LOG scale.

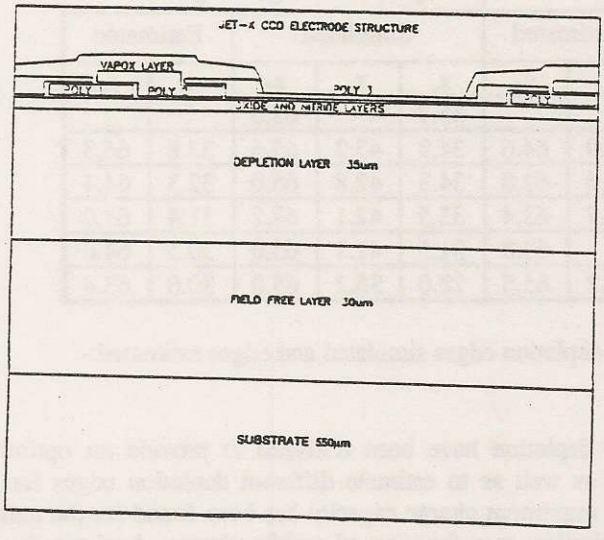


Figure 1

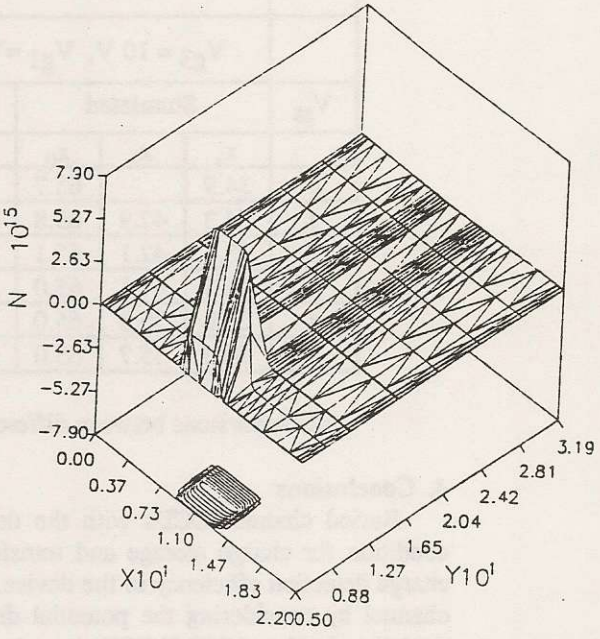


Figure 2

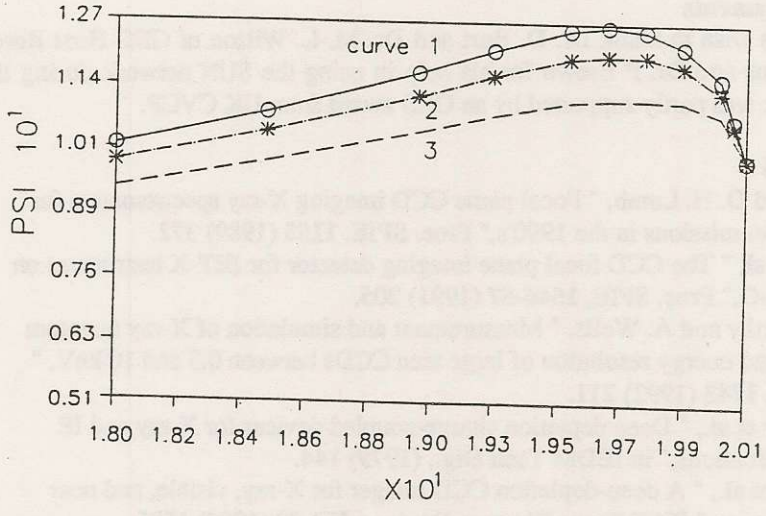


Figure 3

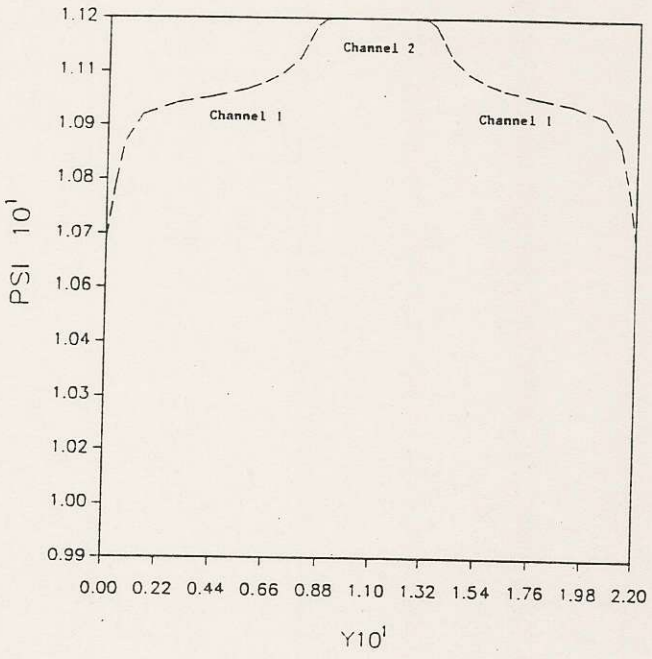


**Figure 4**

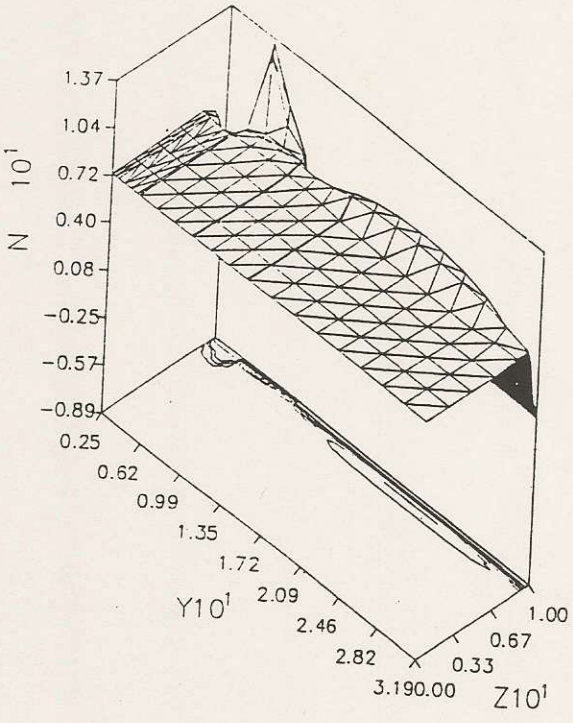


**Figure 5a**

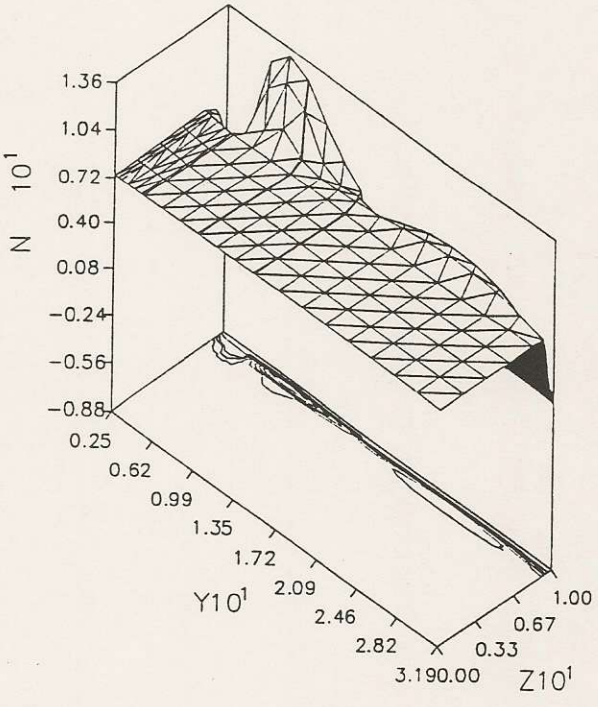


**Figure 5b**

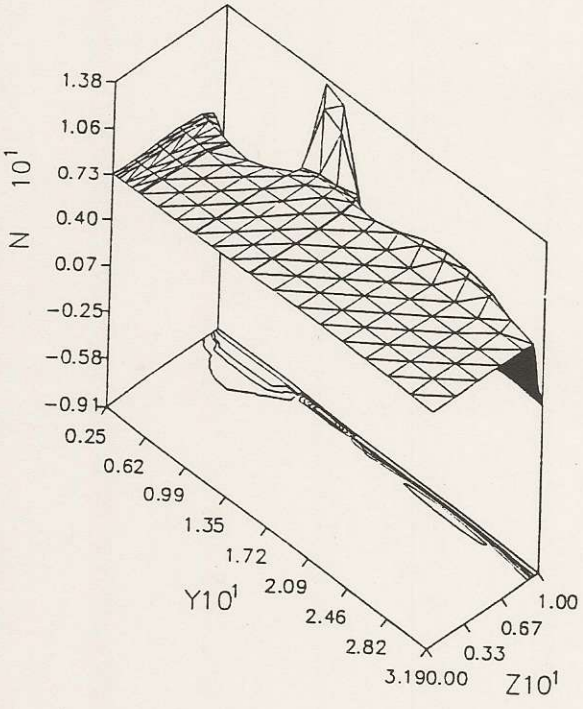


**Figure 5c**