2-D MODELING OF CHARGE COUPLED DEVICES: OPTIMUM DESIGN AND OPERATION FOR MAXIMUM CHARGE HANDLING CAPABILITY

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ABSTRACT

The 2-D process and device modeling programs SUPREM-4 and PISCES have been used to model Charge-Coupled Devices. Together they provide a powerful simulation tool that can model and extract virtually all critical CCD parameters. Charge handling capability is explored in this work and the method is presented to model, design, and operate CCD's for maximum full well . Two basic types and modes of operation are considered:Non-MPP(no boron barrier), and MPP(boron barrier). The architecture is assumed to be 3 phase, but the general method presented here can be applied to CCD's of any size, format, or geometry. The paper is divided into two sections: the first part describes the fundamental principles and methodology of maximum full well design, and the second part shows how several important 2nd order effects fine tune the theory; and how full well, gate voltage, and operational speed are all intimately linked together. All of the following analysis and theory has been derived from modeling and simulation, and has been supported with measurement on many CCD's of varied designs and processes. Due to the limited space available, the scope of this paper will primarily be qualitative in nature.

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ABSTRACT

The 2-D process and device modeling programs SUPREM-4 and PISCES provide a powerful simulation tool that, when used together, can model and extract virtually all critical CCD parameters. Charge handling capability is explored in this work, and the method is presented to model, design, and operate CCD's for maximum full well (FW). Two basic types and modes of operation are considered: Non-MPP(no Boron barrier), and MPP(Boron barrier). The architecture is assumed to be 3 phase, but the general method presented here can be applied to CCD's of any size, format, or geometry.

INTRODUCTION

The paper is divided into two sections. Part (A) describes the fundamental principles and methodology of FW design; part(B) shows how several important 2nd order effects fine tune the theory; and how FW, gate voltage, and operational speed are all intimately linked together. All of the following analysis and theory has been derived from modeling and simulation; and has been supported with measurement on many CCD's of varied designs and processes. However, due to the limited space available, the scope of this paper will primarily be qualitative in nature. Much of the supporting data has been recently presented (1); and a thorough quantitative synthesis of theory and measurement will be forthcoming(2).

A) FIRST ORDER EFFECTS

CASE 1. Non-MPP devices (no boron implanted barrier)

In a Non-MPP device, FW is set by the maximum charge contained under each gate electrode at the point of saturation. There are two basic types of saturation in a buried channel CCD and they are identified and defined as follows:

1. Bloomed Full Well(BFW) - saturation occurs when charge spills laterally into an adjacent pixel resulting in a bloomed condition.
2. Surface Full Well(SFW) - saturation occurs when charge interacts with surface states at the oxide/semiconductor interface resulting in CTE loss.

From the operation standpoint, maximum FW is set by the dynamics of BFW and SFW, and is a direct function of the gate voltage, Vg. BFW and SFW behave quite differently with Vg, and their relationship is plotted is Fig.1. As Vg is raised from the inversion voltage (Vgi) the well depth increases from zero volts and BFW also increases monotonically . SFW is maximum at Vgi, and decreases monotonically with increasing Vg, until it eventually goes to zero at high Vg. Actual FW is the smaller of BFW and SFW and follows the dark line. From the plot, maximum FW is achieved when BFW equals SFW and occurs when Vg is optimized at Vgo.

The potential plot of Fig.2 shows the optimized FW condition where BFW=SFW; the well is filled up to the edge of the barrier phase and to the surface. It is obvious that Vgo (clock high) and Vgi (clock low) are critical to optimum FW operation, and each can be found directly from the plot of channel potential vs. Vg , as shown in Fig.3. The dotted line through Vg=0 is parallel to the potential curve (outside of inversion), and Vgo is found as indicated. The analysis neglects the effects of flatband voltage which shifts the dotted line left of zero, but represents a good 1st order approximation.

From the processing standpoint, FW is a direct function of the phosphorus buried channel (BC) dose. Higher BC doses translate into higher BFW and SFW; therefore FW increases monotonically with dose. However, there are limitations and problems associated with high BC doses, some of which can be overcome and some of which cannot, and these are discussed below.

1. High voltage swings. Fig.4 shows that, everything else being equal, a higher BC dose translates into higher Vgi and higher Vgo. System constraints put a limit on the maximum voltage swing and the BC dose must be set within this range.
2. Reduced charge packet volume. As the BC dose rises the depletion depth increases, which lowers the effective capacitance of the MOS BC structure. This shrinks the effective volume of the charge packet, which diminishes some of the FW increase of the higher BC dose, as shown in Fig.5.
3. High electric fields. For very high doses, the internal fields are so high that impact ionization and dark spikes are a possibility, rendering the CCD useless.

The first two issues can be somewhat mitigated by clever processing. Fig.6 shows that if the BC junction depth , Xj, is decreased (via a shorter drive time or lower temp. or both) , Vgi remains unchanged but Vgo is lowered, decreasing the overall swing. Lowering Xj also decreases depletion depths;charge volumes can approach or surpass that at low BC doses(Fig.5). Nothing can be done about the third issue, as it represents a fundamental limit as to the highest practical BC dose.

CASE 2. MPP devices (boron implanted barrier)

Running MPP necessitates providing a built in barrier under phase 3. This enables integration with all phases inverted which substantially lowers dark current(3). This is accomplished by implanting boron under phase 3 which compensates some of the phosphorus, lowering the net BC dose under this phase. As the boron dose increases, the phase 3 inversion potential decreases and the potential well (phase1-2) during integration deepens, which translates into higher integration FW. Conversely, as the boron dose is increased , FW for phase 3(during readout) is decreased because of the reduced BC dose. Therefore, a plot of FW vs. boron for phases1-2(integration) and phase 3 (readout) is shown in Fig.7. Actual FW is the smaller of the two and follows the dark line. Maximum FW (FWo) occurs when the two entities are equal and happens when the boron dose is optimized at Do.

From Fig.8a we see that adding boron (any dose) under phase 3 lowers BFW and SFW by equal amounts relative to phases 1 and 2. This sets the optimum clock high gate voltage Vgo, for phase 3, equal to that of phases 1 and 2, and is found by looking at Fig.8b which shows the potential vs. Vg curves for all phases. Vgo for all three phases is found via the phase1-2 potential line as explained previously. Vgi for phase 3 is reduced because of its lower net BC dose.

B) 2nd ORDER EFFECTS

1. THERMIONIC EMISSION

Electrons contained within a well possess thermal energy (kT), and therefore acquire random thermal velocities. As a potential well is filled with charge, the barrier (difference in potential between the well and either the lateral or surface potential) becomes smaller and it becomes statistically more probable that an electron will acquire enough thermal velocity to surmount the barrier and cause a BFW or SFW condition. The thermodynamic principle guiding this effect is called thermionic emission, and it defines the barrier, Vb, needed to prevent BFW or SFW. The magnitude of the barrier is a linear function of temperature, and varies as the log of the number of electrons, and the amount of time they sit in potential wells. For typical clocking schemes, and a FW of 500K electrons, Vb assumes of value of about .6V at room temperature(2).

The potential diagram at FW, with thermionic emission included, now looks like Fig.9 (compare to Fig.2). The barrier to the surface, Vb(s), is about half the magnitude (.3V) of the lateral barrier Vb(b) because some of the electrons that escape to the surface and are trapped by interface states, get re-emitted back into the well during the same clock period, and therefore do not contribute to CTE loss (4).

Thermionic emission has several profound effects on the design and operation of CCD's and these are discussed below.

a) Full Well – Vb(b) and Vb(s) cause a reduction in BFW and SFW, respectively, lowering overall FW. FW increases as temperature and time are reduced(1).

b) Optimum clock high voltage, Vgo – The FW vs Vg curve in Fig.10a shows that thermionic emission causes a reduction in Vgo. This is because SFW is actually lowered more than BFW even though Vb(s) is less then Vb(b). This is due to the dynamics of the surface potential and maximum well potential and how they change with Vg and signal charge: as charge is added to a well, Vgo will adjust to maintain the proper magnitudes of Vb(b) and Vb(s). The magnitude of the reduction in Vgo is proportionate to FW, and therefore to the BC dose, and it has a noticeable impact upon MPP devices. Because the BC dose is less under phase 3 , Vgo reduction is also less for phase 3 , ie., the optimum gate voltage for phase 3 is higher than phases 1 and 2, as shown in Fig.10b. For boron doses near the optimum value (Do), the difference in Vgo for phase 3 is typically 1-2 volts. Larger boron doses translate into greater Vgo differences.

c) Optimum Boron Dose for MPP – Due to the same basic fundamentals of the dynamics of BFW and SFW reduction, thermionic emission lowers the optimum boron dose, Do, for MPP devices, as shown in Fig.11.

2. SPEED

All of the preceding analysis assumes operation at slow speeds, ie., all charge has time to transfer to the next gate. Charge transfer, however, requires a finite time and the last remaining electrons are transferred via fringing fields set up by potential differences under adjacent gates. If not enough time is allotted, some charge will be left behind, resulting in CTE loss. Because fringing fields decrease as wells fill, incomplete transfer is most probable when levels of charge are at or near maximum capacity. Enhancing the fringing fields by increasing the clock high gate voltage results in decreased transfer times, as shown in Fig.12

We now identify and define two distinct types of full well.

Static Full Well - FW(S) - – The maximum amount of charge a well can hold before it saturates(as in Fig.1)

Dynamic Full Well - FW(D)— The maximum amount of charge that can transfer from gate to gate in a given time with no CTE loss . FW(D) is a function of time and Vg, as shown in Fig.13.

Actual FW is now the smaller of FW(S) and FW(D) and it is plotted vs. Vg in Fig14. Note that the maximum FW attainable is FW(S), and it occurs at Vg=Vgo, and at transfer times greater than or equal to the critical time, Tc. As transfer times are decreased below Tc, the optimum gate voltage, Vgo, must increase to transfer the charge which in turn lowers FW via SFW effects.

Fig.14 applies to all CCD's and Tc is primarily dependent upon pixel geometries; with shorter gate lengths causing a reduction in Tc, but it can also be a function of processing. The boron implant under phase 3 in MPP devices diffuses laterally under adjacent gates setting up a small potential barrier at the gate edges. The magnitude of the barrier is largest during the final portion of charge transfer(when fringing fields are smallest), and it slows transfer into phase 3. This causes Tc for phase 3 to exceed that of the other phases; up to 10 times larger for boron doses near Do (1). Therefore, when transfer times are less than Tc(phase 3), the preceding FW(D) theory puts Vgo for phase 3 greater than the other phases, the difference being proportional to the speed. When running very fast, this difference can be as much as 10 volts, and the subsequent drop in FW can be greater than 50%.

3. ELECTRODE VOLTAGE DROP ACROSS CHIP

Because of the finite RC value of the polysilicon electrodes, there can be a significant voltage drop from the chip edge to center. This shift from the optimum voltage degrades FW; the magnitude of degradation getting greater as speeds are increased. There is no way to eliminate FW loss at high speeds, but there is an operational means to minimize it. If the voltage drop, Vgd, is calculated from edge to center, then there are basically two different methods to run the chip as shown in Fig.15.

a) The clocks are run at Vg=Vgo. The center is now at Vgo-Vgd and is limiting overall FW(reduced to FW1)

b) The clocks are run at Vg=Vgo+Vgd. The center is at Vgo and the edge is now limiting overall FW(reduced to FW2).

Method (a) is limited by BFW in the center of the chip and method (b) by SFW at the edge. Due to the difference in the slopes of the BFW and SFW lines, SFW shows less FW degradation than BFW for a given Vgd. Therefore, method (b) provides the highest FW.

ACKNOWLEDGMENTS

Many thanks to the Loral Fairchild Tustin group under the direction of Dick Bredthauer for fabrication of many of the high quality CCD's used in this work; and to Steve Hallman of Hughes Aircraft Co., El Segundo, for technical consultation and many enlightening discussions regarding thermionic emission theory.

REFERENCES

1. Janesick,J., Winzenread,R., Pinter,J., Dyck,R., "Sandbox CCD's," SPIE, San Jose, Feb.,1995
2. Janesick,J., Pinter,J., "Modeling and Analysis of CCD's", presented at CCD Workshop, Grand Cayman, Dec.,1995
3. Janesick,J.,et al, "History and Advancement of CCD's,"
4. Chatterjee,P., Taylor,G., "Optimum Scaling of Buried Channel CCD's," IEEE Transactions of Electron Devices, Vol.ED-27, No.3, March, 1980

FIRST ORDER EFFECTS

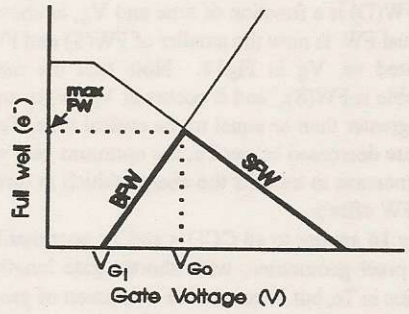


Figure 1. Full well is the smaller of BFW and SFW (Thicker line). Maximum FW occurs when BFW = SFW and Vg=Vgo.

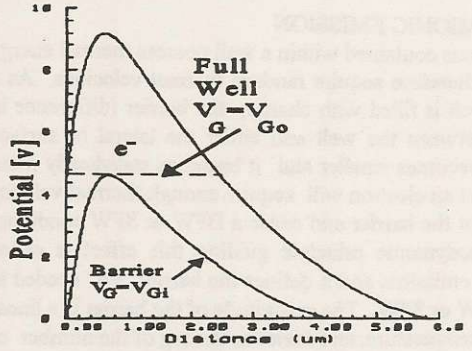


Figure 2. At maximum FW, Vg is optimized at Vgo and the well is filled to the barrier edge and to the surface.

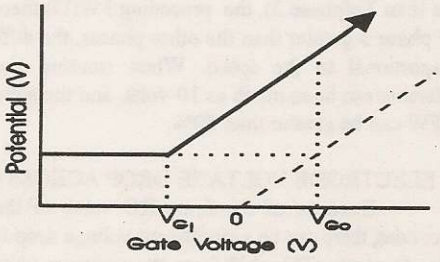


Figure 3. Clock high (Vgo) and clock low (Vgi) can be found from potential vs. gate voltage.

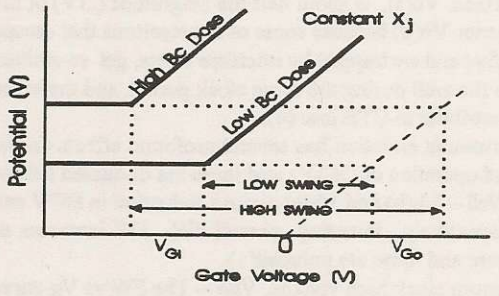


Figure 4. Increasing the buried channel (Bc) dose increases both Vgo and Vgi.

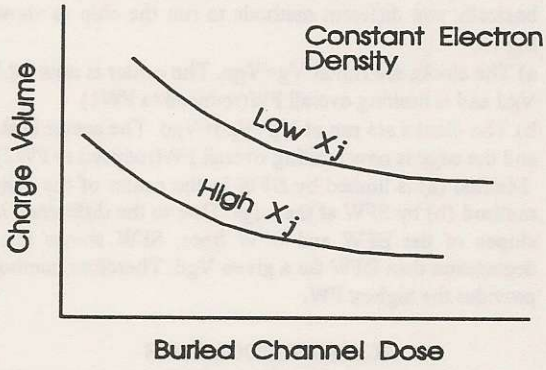


Figure 5. As Bc dose is increased charge volume is decreased. Lowering the Bc junction depth (Xj) raises the volume.

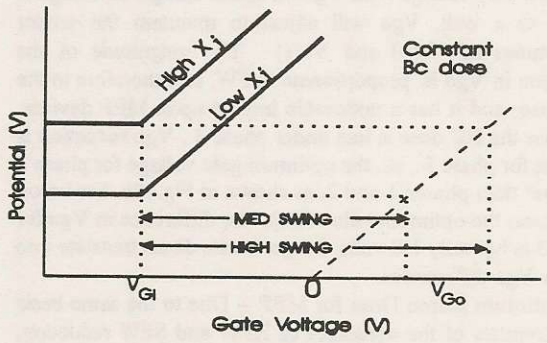
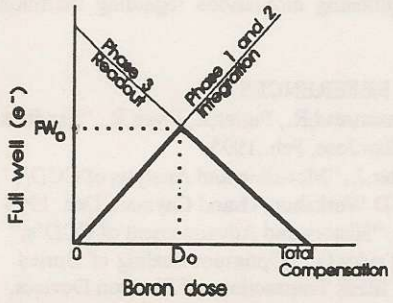
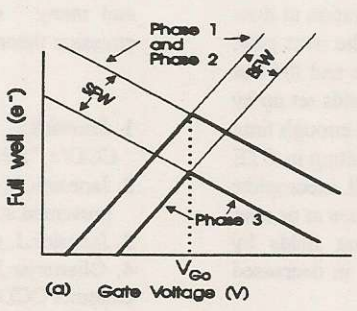


Figure 6. Reducing the Bc junction depth (Xj) lowers Vgo and decreases clock swing.





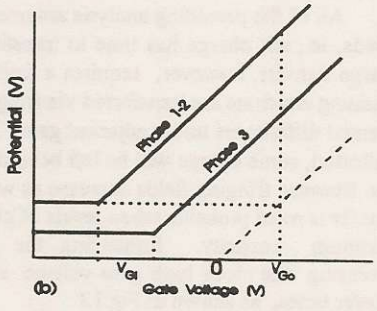


Figure 7. For an MPP device maximum FW is achieved when the boron dose is optimized (Do),i.e. when phase1- 2 integration equals phase 3 readout.

Figure 8. (a) Implanting boron in phase 3 lowers BFW and SFW by equal amounts; Vgo remains constant for all phases. (b) Vgo is found from the phase 1-2 potential vs Vg curve.

2ND ORDER EFFECTS

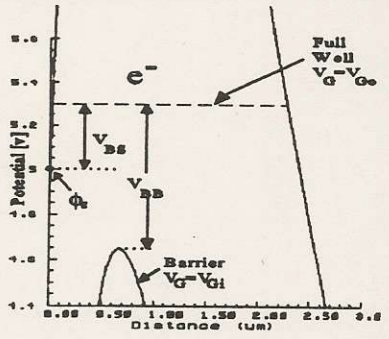


Figure 9. Thermionic emission lowers FW by defining a surface barrier (Vbs) and a lateral barrier (Vbb).

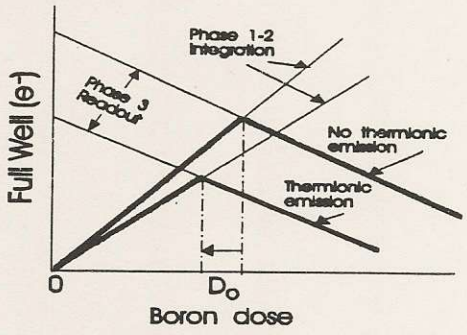
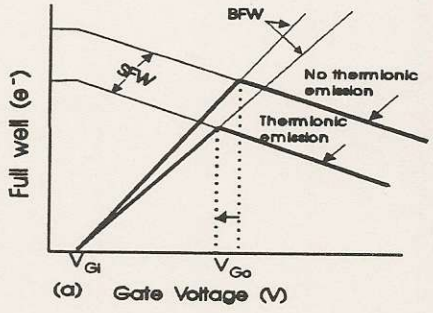


Figure 11. Thermionic emission lowers the optimum boron dose in MPP devices.



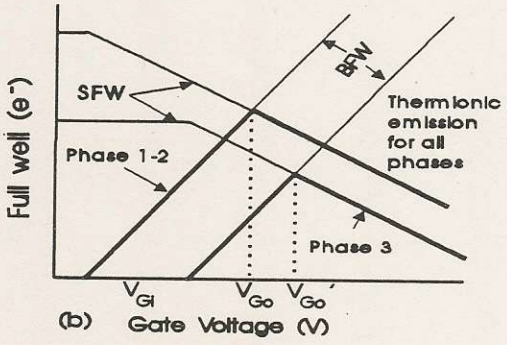


Figure 10. Thermionic emission (a) lowers the optimum gate voltage for all phases and (b) causes the optimum gate voltage for phase 3 (Vgo') to exceed phases 1 and 2 (Vgo) in MPP devices.

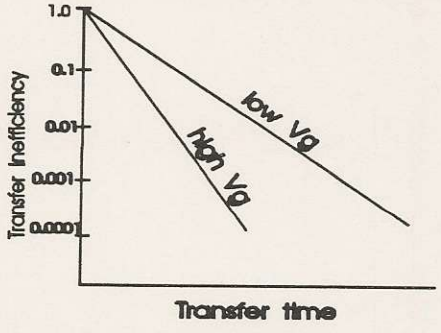


Figure 12. As gate voltage is increased, transfer time is decreased.

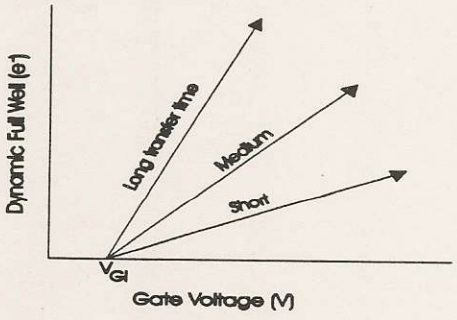


Figure 13. Dynamic full well[FW(D)] increases with gate voltage and decreases as transfer times are reduced.

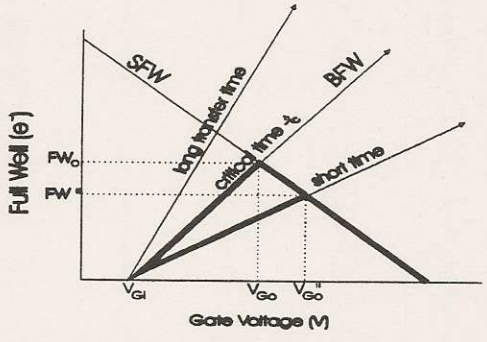


Figure 14. FW is the smaller of FW(S)[Fig.1] and FW(D)[Fig.13]. Largest possible FW (FWo) occurs at transfer times > tc. For time < tc, Vgo is increased(Vgo") and FW is decreased (FW").

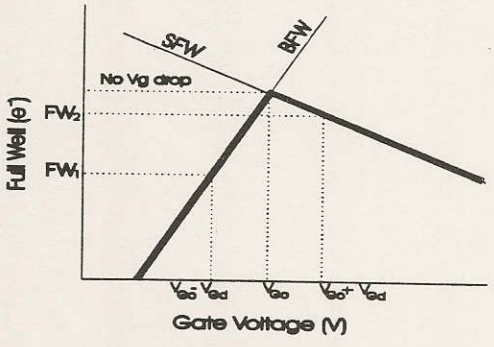


Figure 15. If Vgd is the voltage drop from chip edge to center, then running the clocks at Vgo+Vgd gives a higher FW(FW_2) than running at Vgo (FW_1).