Optimum Design for a 2-Phase CCD

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***Abstract*— 2-phase CCDs used as image sensor horizontal CCDs (HCCDs) have two poly-Si electrodes each, and a boron implanted N^- region. In order to realize low driving voltage at high speed operation, we must take precise care in designing barrier N^- region not to form both potential barriers and pockets under the electrode gaps. In this study, we have used a two-dimensional device simulator to investigate the mechanism by which charge transfer in such CCDs depends on the edge position of the N^- region. Results indicate that certain N^- region edge positions (Xp) result in significant electric potential pockets, while others might be expected to result in barriers. Both of these effects can produce significant charge transfer loss. Therefore, it is important to control Xp for CCD optimum design. In a transit time (τ) analysis for any realistic gap length or taper angle of the 1st poly-Si electrode edge, the most efficient charge transfer appeared to be achieved when the N^- region edge position (Xp) lay within the range of that electrode but no further into the range than 0.1 μm.**

I. Introduction

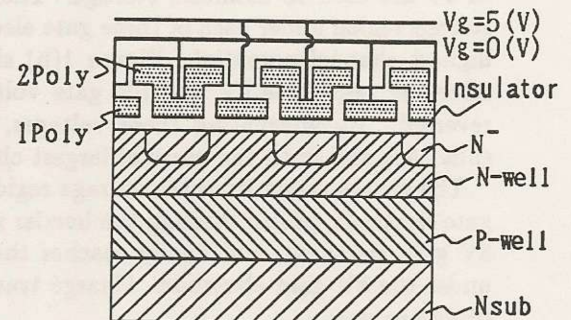
2-phase CCDs are often used as horizontal CCDs (HCCDs) in area image sensor, and their clock frequencies are apt to be higher with increase in pixel numbers.

While power consumption considerations make it important to reduce the clock voltage in HCCDs, significant reduction in this voltage may result pockets of potential under the inter-electrode gaps, pockets which can constitute obstacles to efficient charge transfer. In this regard, Maekawa et al. and Tanaka et al. have managed to suppress potential pocket in a single electrode structure by means of boron implantation self aligned to the inter-electrode gap [1] [2]. Similarly, Toyoda et al. have successfully applied an angled boron implantation technique to the suppression of potential pocket in a double electrode structure [3].

In our study, we have conducted a carrier transit time simulation for a 2-phase CCD with a boron implanted N^- region in an attempt to determine the degree to which gap length (i.e. that of the inter-electrode gap, the gap separating electrodes), in addition to the thickness and shape of electrodes, might effect charge transfer efficiency. We considered the degree to which any resulting deterioration in charge transfer efficiency might be attributed to the creation of potential pockets, and we looked at the effect of the N^- region edge position itself for optimum design that aimed at low voltage and high speed operation.

II. Configuration and Operation of a 2-phase CCD

Figure 1 illustrates the configuration of our simulated 2-phase CCD.



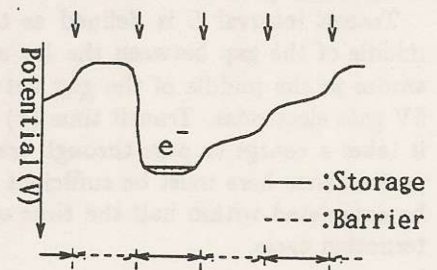
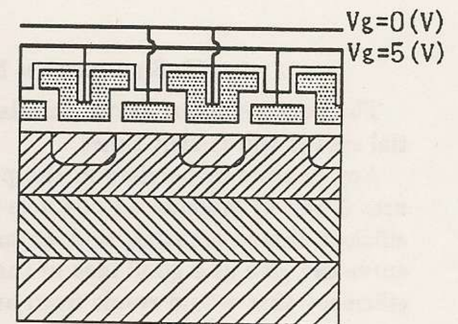


Fig. 1(a)



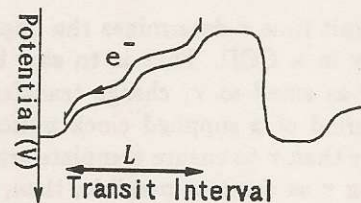


Fig. 1(b)

A P-well layer is formed on an N-substrate, and an N-well layer is formed on the P-well. The N-well layer is covered with a gate insulator layer. Two poly-Si electrodes are deposited on the gate insulator for 2-phase driving. A gate insulator also lies between the 1st and 2nd poly-Si electrodes. A charge storage and a barrier region is formed under each 1st and 2nd poly-Si electrode, respectively.

The barrier regions, for which the N-well becomes partially N^-, are formed by boron implantation. Channel potentials in barrier regions are lower than those in storage regions with the same gate voltage. In this structure, the charges in the barrier regions are transferred to the storage regions.

As may be seen in Figure 1(a), clock voltages assumed as 5V are used to maintain storage. The portions of the storage region under each of these gate electrodes have the highest channel potential. Figure 1(b) shows conditions after the respective 5V and 0V gate voltages have been reversed. By alternating these voltages, we are able to shift back and forth the areas of largest channel potential.

The charge starts from the storage region under the 0V gate electrode, passes through the barrier region under the 5V gate electrode, and finally reaches the storage region under the 5V gate electrode. Charge transfer here is entirely one way.

Transit interval L is defined as the distance from the middle of the gap between the 1st and 2nd 0V gate electrodes to the middle of the gap between the 1st and 2nd 5V gate electrodes. Transit time (τ) is defined as the time it takes a charge to pass through transit interval L. CCD performance here must be sufficient for charge transfer to be completed within half the time of the gate voltage alternation cycle.

III. Simulation Model

The purpose of our device simulation is to obtain potential curves and transit times.

Any pockets or barriers in the potential curve (see Figures 3 and 4) indicate an obstacle that will interfere with efficient charge transfer, and an analysis of the potential curve can give us a good idea of the overall charge transfer efficiency that would result from any given set of parameters.

Transit time τ determines the upper limit for drive frequency in a CCD. That is to say, if the clock period is nearly as small as τ, charge transfer will be incomplete; the period of a supplied clock pulse must be sufficiently greater than τ to ensure complete transfer. Conversely, by making τ as short as possible, then, we extend the range to which drive frequency may be increased and extend the range to which drive voltage may be reduced, while we still maintain efficient transfer.

In our device simulation, we assume there is no free charge in the CCD (i.e. all regions are depleted; charge current is zero), and we are able first of all to obtain two values: channel potential V (the potential curves) and electric field E. From these, we can calculate transit time (τ) as

$$\tau = \int_0^L \frac{dl}{v} = \int_0^L \frac{dl}{\mu E}$$

wherein charge velocity v is replaced by the product of charge mobility μ and electric field E. This method of obtaining a simulated value for τ has the advantage of requiring much less calculation time than simulation methods which are based on the presence of a charge current.

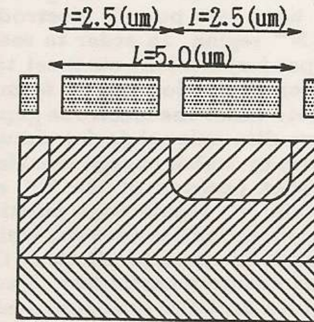


Fig. 2(a)

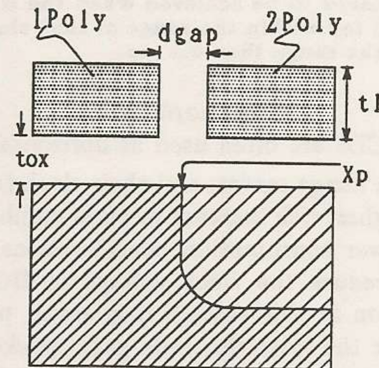


Fig. 2(b)

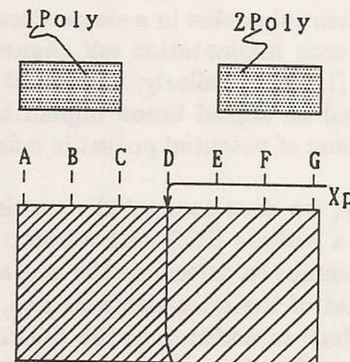


Fig. 2(c)

The major parameters used in our two-dimensional device simulation are inter-electrode gap length (dgap), electrode layer thickness (tl) and the edge position of boron implanted N^- region (Xp). (See Figure 2(b)). We used values for dgap of 0.2, 0.25 and 0.3 μm, and values for tl of

0.1, 0.2, 0.3 and 0.4 μm. We simulated for seven possible combination among 1st and 2nd poly-Si electrode edge positions and the position of the boron implanted N^- region edge (Xp). (See Figure 2(c)). Specifically:

A: Xp protrudes $0.2\mu m$ into the 1st poly-Si.
B: Xp protrudes $0.1\mu m$ into the 1st poly-Si.
C: Xp just reaches the inner edge of the 1st poly-Si.
D: Xp is extends to the middle of the gap.
E: Xp just reaches the inner edge of the 2nd poly-Si.
F: Xp extends to $0.1\mu m$ from the inner edge of the 2nd poly-Si.
G: Xp extends to $0.2\mu m$ from the inner edge of the 2nd poly-Si.

The other parameters are fixed as follows: transit interval L is $5\mu m$; $l = L/2$ is $2.5\mu m$ (See Figure 2); clock voltage on the gate electrode is 5 V; insulator layer is made of silicon oxide and its thickness (tox) is $0.07\mu m$.

The same simulations were also conducted for various 1st poly-Si electrode taper shapes (i.e. for various values of taper angle ta); in these case tl was held constant at 0.4 μm. The structure illustrated in Figure 2, in which the 2nd poly-Si electrode sits side by side with the 1st, is much simpler than that illustrated in Figure 1, in which the 2nd overlaps the 1st, but this does not effect the outcome of our simulation because transit time is independent of the effects of overlap.

IV. Results

1) The relationship between Xp and the transit time.

Our simulation results are shown in Figures 3 and 4. The horizontal axes indicate position (or distance). The origin of the axis is the middle of the gap between the 1st and 2nd 5V gate electrodes. (in case D, Xp coincides with the origin). Axis direction is the opposite of charge transfer direction. The vertical axis indicates channel potential. The electrode layer thickness (tl) is $0.4\mu m$. Potential profile is independent of the tl between $0.1\mu m$ and $0.4\mu m$. As may be seen in Figures 3 and 4, for both gap values, 0.2 and 0.3 μm, variations in potential between A and G are most significantly pronounced at three general positions: $2.3\mu m$, $2.8\mu m$, and $4.9\mu m$.

Potential pockets are apt to appear at positions under inter-electrode gaps. They are seen near $2.3\mu m$ and $4.9\mu m$ in the potential curves of F and G in Figure 3, and E, F and G curves of Figure 4. Looking at this from another angle, we may think of the N^- region as "filling" a pocket as its edge position moves from G to A.

On the other hand, at $2.8\mu m$ we can observe gradual movement toward the formation of a "barrier" as the edge position moves from G to A. We can surmise that if the edge position were to protrude even further beyond the 1st poly-Si (i.e. more than 0.2 μm; beyond position A), a more dramatic barrier would appear, one which would result in significant charge transfer loss.

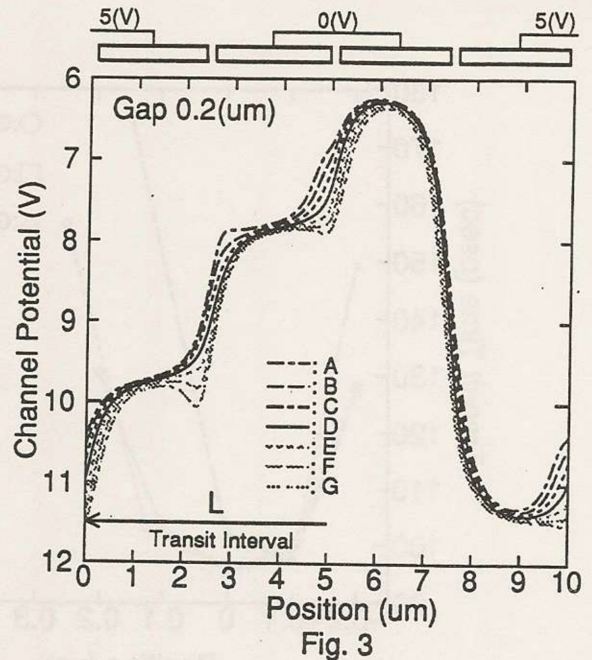


Fig. 3

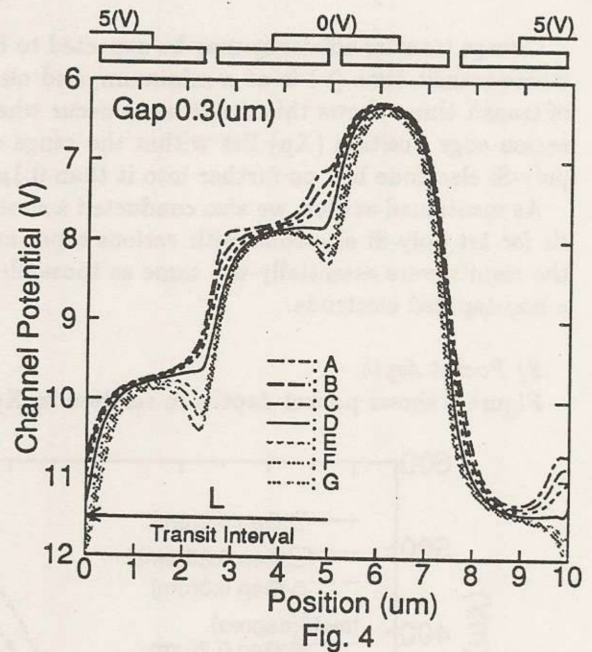


Fig. 4

The best Xp for efficient charge transfer would then appear to lie somewhere in the range between the occurrence of pockets and the possible occurrence of a barrier. In order to determine more precisely what might be the optimal value for Xp, we analyzed transit times, shown in Figure 5. The horizontal axis indicates distance from the 1st poly-Si edge (Xp in case C coincides with the origin). The vertical axis indicates transit time. (Note that where the potential pockets occur transit times have no meaning, and the graph does not include them.)

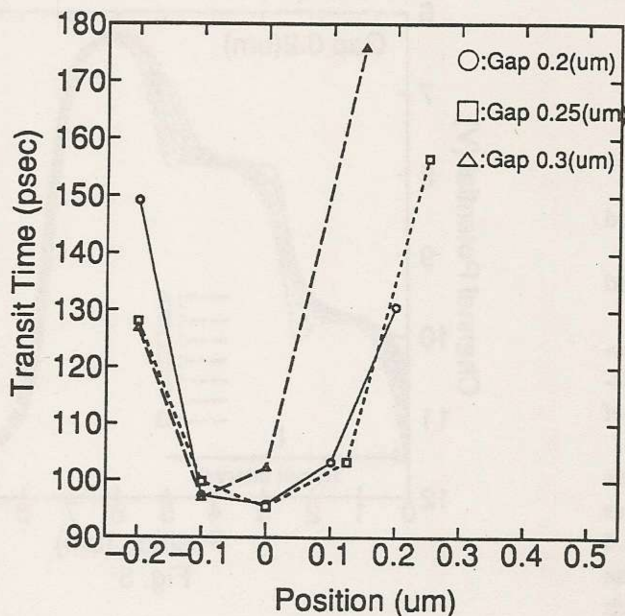


Fig. 5

Charge transfer efficiency may be expected to be highest where transit time (τ) is at a minimum, and our analysis of transit times shows this situation to occur when the N^- region edge position (Xp) lies within the range of the 1st poly-Si electrode but no further into it than $0.1\mu m$.

As mentioned earlier, we also conducted a similar analysis for 1st poly-Si electrode with various taper angles, but the results were essentially the same as those obtained for a non-tapered electrode.

2) Pocket depth.
Figure 6 shows pocket depths in relation to Xp.

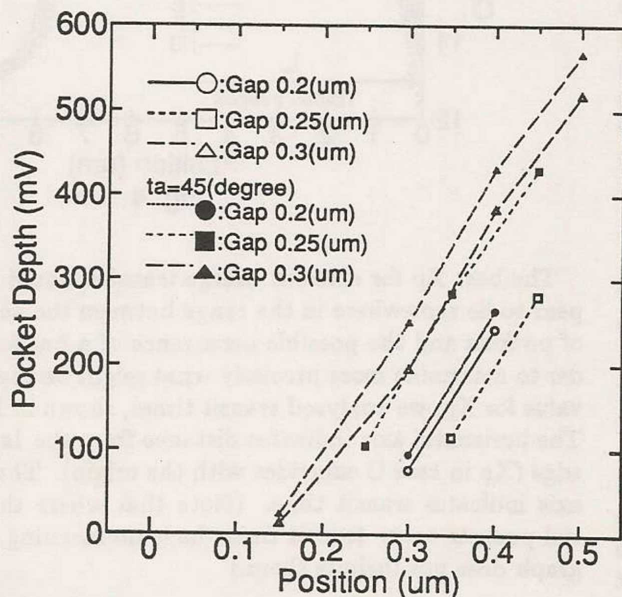


Fig. 6

Figures 3 and 4 have already shown us something of the relationship between pocket depth an Xp; with Figure 6 we are also able to see that:

a) Bigger inter-electrode gaps produce greater pocket depths. (The enlarging of inter-electrode gaps weakens the lines of electric force that come from the sides of the electrode, and this results in deeper.)

b) Higher taper angles produce greater pocket depths (for the same reason as above).

V. Conclusion

In our study, we have simulated a two-dimensional device containing no free charge to investigate the mechanism by which charge transfer in CCDs depends on the edge position of the boron implanted N^- region. Results indicate that certain N^- region edge positions (Xp) result in significant electric potential pockets, the depth of which depends on the size of inter-electrode gap and the degree of electrode taper angle, while other Xp values might be expected to result in a barrier. Both of these effects can produce charge transfer loss. In a transit time analysis for any realistic gap length or taper angle of the 1st poly-Si electrode edge, the most efficient charge transfer appeared to be achieved when the N^- region edge position (Xp) lay within the range of that electrode but no further into that range than $0.1\ \mu m$.

It is important to control Xp for CCD optimum design. Due to optimizations of Xp and impurity profiles in of N-well and P-well, low voltage driving (less than 3V) at high speed (more than 37MHz frequency) can be realized.

Acknowledgment

The authors are very grateful to H. Watanabe and K. Higuchi for their encouragement, and would like to thank the staffs of the System Micro Division and of the ULSI Device Development Laboratories for their valuable help and advice.

References

[1] Maekawa et al., "Single-Level Polycide Gates CCD," Technical Report of IEICE, ED-89-163, pp. 1-6,(1989). (in Japanese)

[2] N. Tanaka et al.,"A Low Driving voltage CCD with Single Layer Electrode Structure for Area Image Sensor", IEDM Technical Digest, pp. 705-708, 1994

[3] Y. Toyoda et al., "A 2/3-inch 2.0M-Pixel M-FIT CCD with a Single Channel HCCD for HDTV Camera", ISSCC Digest of Technical Papers, pp. 220-221,/SLIDE SUPPLEMENT, pp. 176-177, Feb., 1992.