MEGA PIXEL CCD IMAGE SENSOR TECHNOLOGY

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ABSTRACT

In this paper, we concentrate on large format CCD Image Sensors of a million or more pixels. We review the state of the art of mega sensors and also highlight the present challenges and technical issues. The second part of our paper deals with our development of a 25.4 Mega pixel CCD image sensor with forward motion compensation. We describe the architecture, deal with yield issues and also give experimental results on images with forward motion compensation.

MEGA PIXEL CCD IMAGE SENSORS

CCD image sensors and electronic digital video CCD cameras are widely used in numerous applications. These include surveillance, corporate television, broadcast television, manufacturing, remote inspection, medical, military, and by research laboratories.

ILT mega sensors are predominantly aimed for HDTV. As a result, the effort is toward smaller image format sizes through finer line lithography, novel vertical CCD interconnect schemes and extensive vertical integration. Significant issues which are presently addressed are reduction of smear, efficient antiblooming, low readout noise at high video output rates, and reduction in fabrication cost which translates to smaller pixel size. All of these image sensor arrays use 2:1 interlacing to increase resolution. Sony reported a 1920 x 1036 HDTV frame interline transfer CCD based on a 5.0 mm x 5.2 mm pixel pitch [1]. The device has a dual readout shift register. NEC outlined a 1920 x 1080 interline transfer CCD based on a 5.0 mm x 5.0 mm pixel pitch[2]. The device has dual outputs each operating at 37 MHz. Separate p-wells are used in the vertical and horizontal CCD to simultaneously maximize the full well charge and output register transfer efficiency. A 1920 x 1036 frame interline transfer CCD based on a 5.0 mm x 5.2 mm pixel pitch that offers either interlaced or progressive scanned operation for HDTV applications was reported by Matsushita[3]. Toshiba reported a frame interline transfer CCD based on a 5.0 mm x 5.2 mm pixel pitch with an overlaid amorphous silicon photoconversion layer yielding large dynamic range and -140 dB smear[4]. Image lag may still be a problem with this approach. Eastman Kodak reported a 1920 x 1080 interlaced interline transfer device with a pixel pitch of 7.3 mm x 7.3 mm intended for HDTV applications with a special vertical electrode strapping in order to reduce RC delays [5]. Philips has a 1920 x 1152 interlaced frame transfer image sensor array with vertical antiblooming and 7.25 mm x 13.6 mm pixels intended for HDTV applications [6]. This device has dual outputs capable of 36 MHz each. Thomson CSF reported a 1260 x 1152 interlaced (576 vertical CCD stages) frame transfer device based on 11 mm x 13.6 mm pitch with lateral antiblooming and exposure control.

Frame type architectures are also widely used and manufactured. These devices are typically used in non-consumer based applications and,

more commonly, for low speed scientific applications. In these cases specifications such as dark current, fill factor, full well capacity, dynamic range, sensitivity and MTF are optimized. In many cases the effort to optimize these specifications along with resolution result in wafer scale image formats. In addition, many of these devices rely on the application to interrupt the incident illumination for device readout using either an external shutter or pulsed illumination.

DALSA developed, designed and manufactures a family of large format silicon CCD imagers which can operate in the visible and near infrared spectrum [7-13]. These image sensors include 1024 X 1024, 2048 X 2048, 4096 X 4096 pixel and most recently we produced the new 25.4 mega pixel sensor which is the largest CCD imager presently reported and is made up of 5040 X 5040 pixels. Tektronics reported a 2048 x 2048 based on a 21 mm x 21 mm pixel 4 inch wafer scale device. Due to the low speed single output, the device is intended for low speed scientific applications. Loral Fairchild offers a 4096 x 4096 based on a 7.5 mm x 7.5 mm pitch. EG&G Reticon offers a 2048 x 2048 device based on a 13.5 mm x 13.5 mm pitch with four outputs. This device is intended for scientific and spectroscopy applications.

FOCAL PLANE 5040 X 5040 IMAGER WITH FORWARD MOTION COMPENSATION

The concept of electronic image motion compensation for use with large frame transfer CCD image sensors has been described by Lareau et.al [14-15]. The minimization of image blur for a frame transfer image sensor used in a side oblique reconnaissance image mode is vital where the velocities of scene segments across the array are not uniform. This is shown in Fig.1.

We developed a unique CCD architecture which provides implementation of forward motion compensation (FMC) [14-15]. The architecture of this CCD implementation is described in Fig.2.

Compensation for the nonuniform scene velocity can be accomplished by segmenting the image sensor into several independently variable speed vertical clocking segments, and operating the device in a partial TDI mode to match scene and pixel velocities. In this way high MTF can be maintained throughout the imaged scene while achieving minimized "pop up" mission time exposure profile.

We first tested the motion compensation concept on a 2048 x 2048 element full frame sensor [7, 10]. FMC blocks are isolated from each other by breaking the polysilicon bus lines at specified intervals.

Figure 2 shows our full frame transfer device, 5040 X 5040 pixels with 16 FMC sections, each with 315(H) x 5040(V) photoelements, that has 8 outputs. The pixel pitch is 12 mm x 12 mm and uses two metal and three layer polysilicon buried channel CCD technology. It employees a two micron design rule, a profiled buried channel and metal strapping of polysilicon clock lines.

The charge storage capacity of each photosite is approximately 200,000 electrons. The minimum detectable charge is 50 electrons when correlated double sampling is used. Reduced dark leakage operation of 60 pA/cm^2, when operated in the hole accumulation mode, has been demonstrated. Multitap output structures are utilized to facilitate frame rates between 2 frames and 10 frames per second. Experimental results of forward motion compensation of a reconnaissance scene is shown in Fig.3. This scene was captured by our CCD image sensor with forward motion compensation. The velocity of the carrier of the

sensor was 208.5 KN at an altitude of 400 feet [16].

YIELD OF WAFER SCALE CCD IMAGE SENSORS

Yield for the wafer scale 5040 X 5040 pixel sensor is fundamentally different from that for smaller dies. The defect distribution was examined across many wafers and found to be essentially random. The yield of sensors susceptible to these defects was in excellent agreement with the yield law: $Y = C \exp(-AD)$.

A is the sensor area, D is the defect density, and C is a constant to account for other yield loss mechanisms. For metal strapped devices, D is the net defect density over all 4 critical layers (poly-2, poly-3, contact, and metal-1). Figure 4 is a plot of sensor yield versus area. Current 4" wafer clean room technology limit the net defect density to about 1 defect/sq.in. These curves predict that yielding metal strapped sensors requires a significantly lower defect density.

The gross shorts/opens yield is generally dominant for the wafer scale sensors. Functional yield for image quality is relatively high if the sensors survive the shorts/opens tests.

By using optimized CCD lay out practices and improved process layers and sequences, the systematic yield loss mechanisms can be minimized. With an innovative design approach we overcame the 4" wafer clean room limiting factor on the yield for our 25.4 Mpixel sensor.

We successfully demonstrated the feasibility and fabrication of a 25.4 million pixel (61.4mm x 61.4mm) full frame transfer CCD image sensor with finite and acceptable yield.

CONCLUSION

We developed a wafer scale CCD image sensor technology. This technology was used successfully to develop and fabricate a 5040 X 5040 image sensor with acceptable yield. A brief review of recent mega sensor developments is also given.

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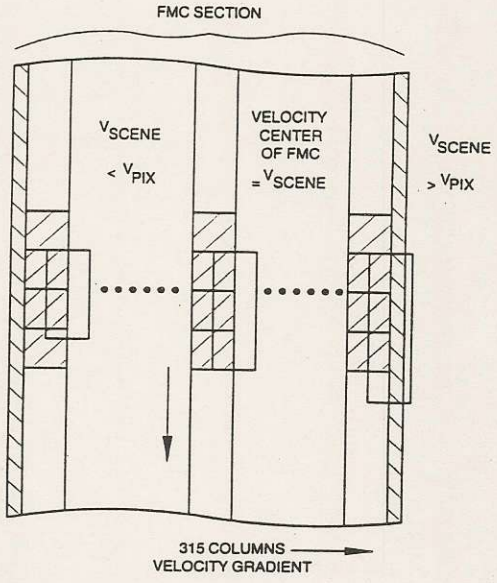

FIG.1 VELOCITY MISMATCH SCHEMATIC

SENSOR WITH SECTIONED IMAGING AREA FOR MOTION COMPENSATION

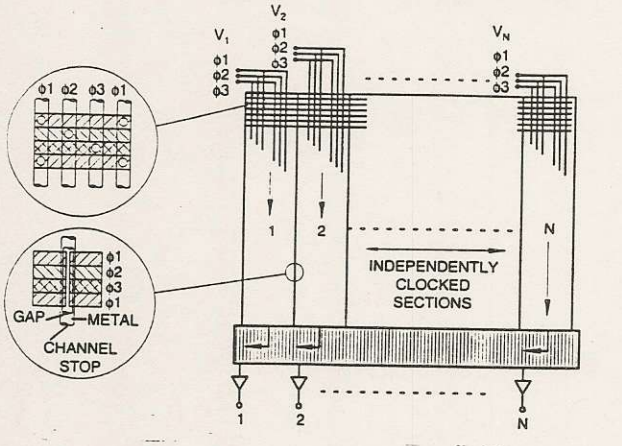

FIG.2 HIGH SPEED SENSOR ARCHITECTURE FOR FORWARD MOTION COMPENSATION

FIG.3 SCENE CAPTURED BY THE CCD IMAGE SENSOR WITH FORWARD MOTION COMPENSATION. VELOCITY IS 208.5KN.

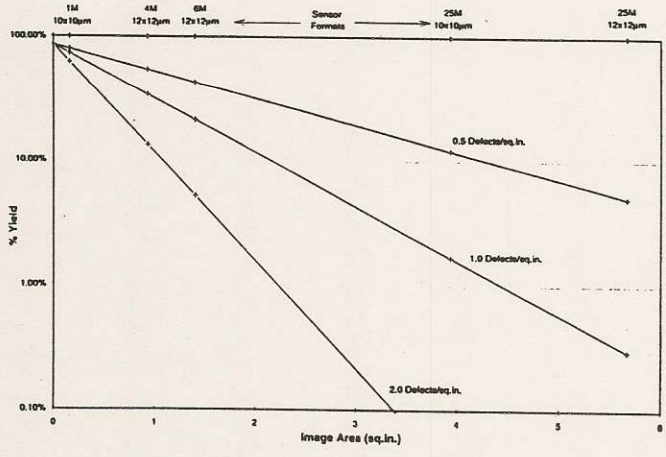

FIG.4 WAFER SCALE SENSOR YIELD AT VARIOUS DEFECT DENSITIES