A 1/3-inch 330k Square-Pixel Progressive-Scan IT-CCD

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ABSTRACT

We developed a 1/3-inch 330k square pixel progressive-scan IT-CCD image sensor with 640(H) X480(V) pixels for VGA compatibility. All pixel signals can be read independently via the four-phase vertical CCD and dual-channel horizontal CCD constructed under a three-level polysilicon process. This structure enables high vertical resolution of 480 TV lines, making the device suitable for a wide range of applications such as video capturing, teleconference systems and industrial uses.

1. Introduction

Recently, video cameras have become more compact while their picture quality has been improved. Image sensors today demand high resolution and small size. High resolution is usually achieved by increasing the number of horizontal pixels in the conventional interline transfer CCD (IT-CCD). Maximum vertical resolution, however, is limited to 350 TV lines by the fact that IT-CCD adds signal charges for neighboring lines, thereby processing the total 480 lines in line pairs. A progressive-scan IT-CCD developed recently has achieved vertical resolution of 480 TV lines where each line is read independently, but these CCDs are generally larger due to the complicated vertical and horizontal CCD structures required.[1],[2] The 1/2-inch format, the smallest for the progressive-scan IT-CCD, increases the costs associated with chips.

We have developed a 1/3-inch progressive-scan IT-CCD image sensor. This device employs a four-phase vertical CCD (V-CCD) and a simplified dual channel horizontal CCD (H-CCD) structure using a three-level polysilicon process.

2. Device structure

The schematic diagram of the device is shown in Figure 1. The device has 659(H)x494(V) effective pixels which include 640(H)x480(V) pixels corresponding to the Video Graphics Array (VGA) format. All photodiode signals are transferred to the V-CCD independently using the four-phase vertical electrodes. The signals of two rows of photodiodes are read out simultaneously by the dual channel horizontal CCD (H-CCD1 and H-CCD2). The pixel size is 7.4(H)x 7.4(V)μm^2 , and the pixels are arranged in a square. The progressive-scan IT-CCD is suitable for video capturing, teleconference systems and industrial uses.

3. Key Technologies

This device has two technological features which are discussed below.

A. Four-Phase V-CCD

The first feature is the four-phase V-CCD. The unit pixel (see Figure 2) is divided into three parts : the V-CCD, the photodiode, and the wiring area which is located between vertical photodiodes. In the conventional pixel, the V-CCD is comprised of three-phase electrodes which are fabricated in a three-level polysilicon process. In the proposed pixel structure, however, the V-CCD has four-phase electrodes to increase the V-CCDs charge handling capacity and photodiode sensitivity.

Figure 3 shows the transfer potential profiles of the V-CCD. The storage area capacity of the four-phase V-CCD is one-half of the unit pixels, 50% more (1.5 times) than the maximum one-third of conventional V-CCDs. Therefore, the V-CCD channel width as seen in Figure 2 can be narrowed, and the photodiode area is made larger than in a conventional CCD. As a result, the sensitivity of this device is improved.

The design difficulty of the four-phase V-CCD lies in the wiring of electrodes. Figure 4 shows a cross section of the wiring areas previously shown in Figure 2. In a conventional three-phase V-CCD, the electrodes are formed of three-level polysilicon and arranged on top of each other. The electrode structure in this device differs from conventional structures in that the four phase electrodes are formed through a three-level polysilicon process. The first

electrode (V1) is narrower and vertically thicker with electrical resistance as low as conventional electrodes. The second and third electrodes (V2 and V3), made of a second polysilicon level, are configured in parallel formation above the first electrode to minimize the separation distance as shown in Figure 4. The fourth electrode (V4) is made of the third polysilicon level. By using this wiring structure, the wiring space between photodiode A and photodiode B can be as narrow as the wiring space in a conventional CCD, even with the inclusion of the four-phase electrodes. Moreover, the sensitivity of the photodiode does not decline using this structure. Thus, charge-handling capacity of the V-CCD and sensitivity of the photodiode area are optimized. This enables a 30% improvement (1.3 times) in V-CCD capacity and photodiode sensitivity over conventional structures.

B. Simplified Dual Channel H-CCD

The second feature of the proposed CCD is the simplified dual channel horizontal CCD. The design problem with the H-CCD concerns how to split within the dual channel H-CCD the two signals sent from the V-CCD.

Figure 5 shows the conventional dual channel H-CCD. The shift gate (SG) and the last gate of the V-CCD (abbreviated VL) are made of the first polysilicon level , and horizontal gates (H1) and (H2) are made of the second and the third polysilicon levels. Signal charges from two horizontal adjacent lines are transferred independently from the V-CCD to the dual channel H-CCD which is discussed below. A signal charge packet of a line (○) is directly transferred under the H1 gate of the H-CCD1. Another signal charge packet from the neighboring line (●) is transferred to the H2 gate of the H-CCD2 through the H1 gate of H-CCD1 and the SG. The signal charge (●) is transferred through the three gates (H1, SG, and H2). Because the shape of the gates through which the signal charge travel are not straight, the structures of the H1 gate, the H2 gate, and the isolation region under the SG are complicated.[1] It is difficult therefore, to narrow the H-CCD pitch with this structure.

To resolve these problems, and achieve a 1/3-inch progressive-scan IT-CCD, we have adopted a structurally simplified dual-channel H-CCD. The dual-channel H-CCD has an improved H-CCD structure and better transfer clock timing for signal sent from the V-CCD to the H-CCD.

In Figure 6, the H-CCD structure of the device is illustrated. The signal charge (●) is transferred straight through the H1 gate and the SG from the H-CCD1 to the H-CCD2. Furthermore, the signal charge (●) is transferred under the same gate(H1), so the structures of the H1 gate and isolation region can be straightened. The simplified gate structures make the isolation region width as narrow as 0.6μm, and enables the channel width to be wider along the direction from the H-CCD1 to the SG. This results in high transfer efficiency and high charge-handling capacity of the SG.

Figure 7 and Figure 8 show the transfer clock timing diagram of the H-CCD and the corresponding potential profiles of the H-CCD, respectively during the horizontal blanking period.

The potential differences are formed at the H1 gate of the H-CCD1 and at the SG. The potential difference at the H1 gate ensures that the signal is transferred in its entirety from the H-CCD1 to the SG, while the potential difference at the SG stores the signal charge from the H-CCD1 and prevents it from flowing back to the H-CCD1. Signal charge is thus transferred efficiently to the H-CCD2 by the H1 and the SG without need for the H2 gate.

The transfer process underlying this device works as follows. At time T1, the VL gate, the H1 gate and the SG have low potential, and signal charge accumulates under the gate V4 of the V-CCD. Between T2 and T3, the charge is transferred from the V-CCD to the H1 gate of the H-CCD1. At T4, the charge flows into the SG. At T5, the potential under the H1 gate goes to high and the signal charge at the SG starts to flow into H-CCD2. At the same time, the next charge of the adjacent line is transferred to the gate V4 by clocking the V-CCD. At T6, the potential of the SG turns low while the H1 potential keeps a high level, and the charge is transferred from the SG to the H-CCD2. Between T7 and T8, the next charge is transferred from the V-CCD to the H-CCD1. Then, the charge transfer from the V-CCD to the dual channel H-CCD is concluded. In this timing scheme, the H1 pulse goes to a high level between T4 and T6, in order to make the potential differences maximum between the H-CCD1 and the SG at T4, and between the SG and the H-CCD2 at T6. As a result, the charge transfer efficiency becomes

maximum at T4 and T6, and the driving voltage amplitude of the SG is declined.

This ensures maximum efficiency of the simplified dual-channel H-CCD. The driving voltage amplitude of the SG is reduced to 5.0V where the high level is 2.5V and the low level is -2.5V because of the simple gate structure and the optimized clock timing.

4. Characteristics

The main characteristics of this device are summarized in Table 1. A sensitivity of 110 mV/lx, and a saturation voltage of 700mV were obtained. Smear is as low as -85dB. The horizontal and the vertical resolution are each 480 TV lines.

5. Conclusion

A 1/3-inch 330k square-pixel progressive-scan IT-CCD has been successfully developed. This device employs the four-phase V-CCD and the simplified dual channel H-CCD. High vertical resolution of 480 TV lines, high sensitivity and high saturation voltage have been achieved in a 1/3-inch sized CCD.

6. Acknowledgment

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7. References

[1] T.Ishigami et al. : " A 1/2-in 380k-pixel Progressive Scan CCD Image Sensor ", ITE Technical Report Vol.17, No.16, pp.39-44 (Mar. 1993)

[2] K.Nakasima et al. : " A 1/2-in 330K Progressive-Scan Image Sensor with Square-Pixel ", ITE Technical Report Vol.18, No.67, PP.7-12 (Nov. 1994)

Optical format	1/3 inch
Effective pixels	659(H)X494(V)
Pixel size	7.4(H)X7.4(V)μm^2
Horizontal resolution	480TV line
Vertical resolution	480TV line
Sensitivity	110mV/lx
Saturation voltage	700mV
Smear	-85dB

Table 1 Characteristics

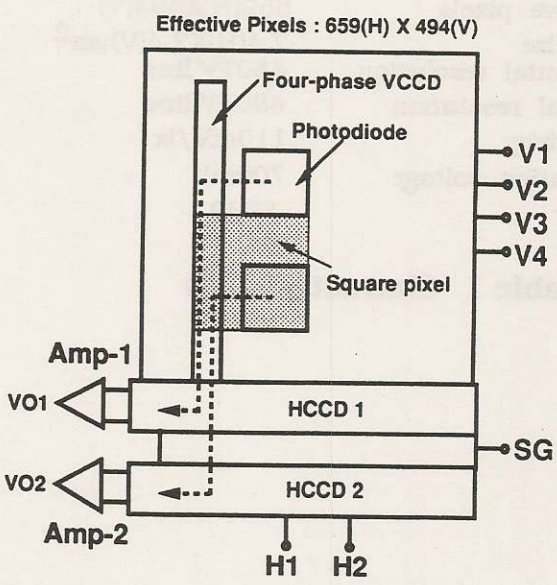
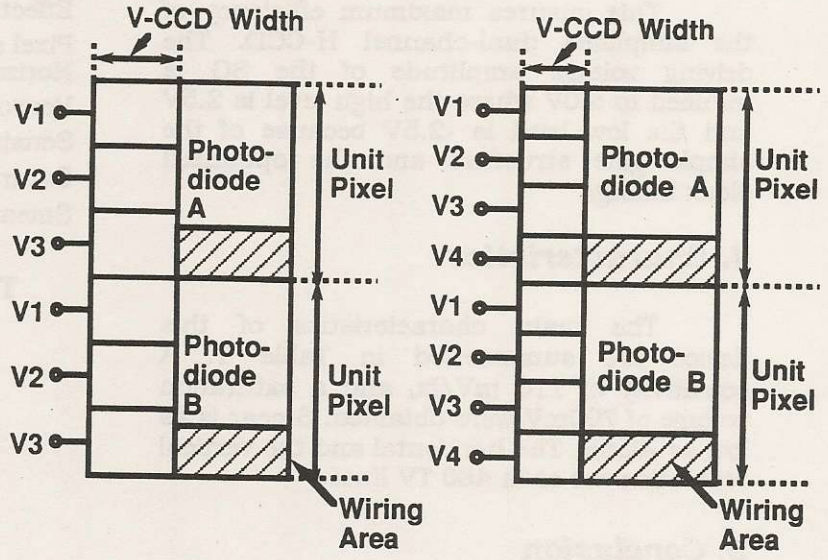
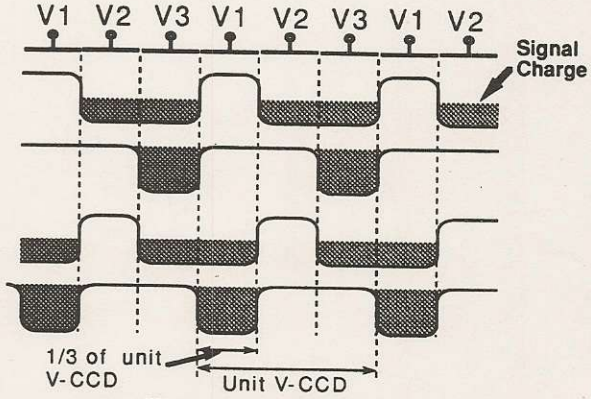


Figure 1 Schematic Diagram of The Device

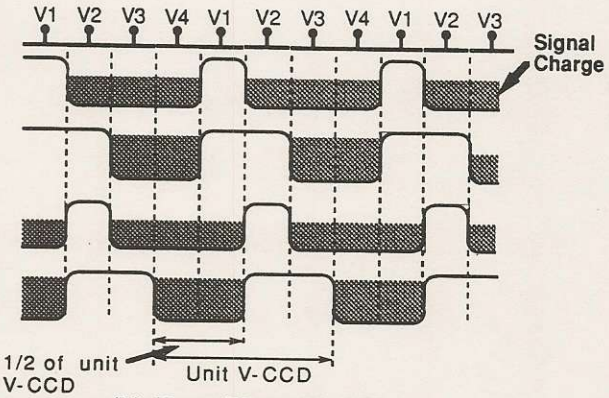


(a) Conventional Pixel Structure (b) Proposed Pixel Structure

Figure 2 Unit Pixels

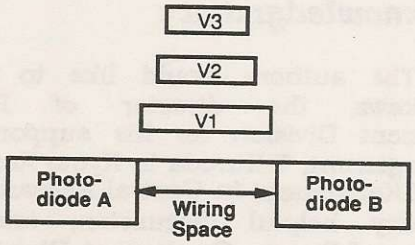


(a) Three-Phase V-CCD

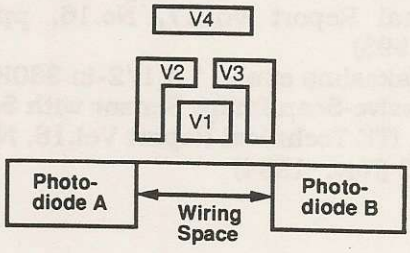


(b) Four-Phase V-CCD

Figure 3 The Transfer Potential Profiles of V-CCD



(a) Conventional device



(b) This device

Figure 4 The Cross Section of Wiring Area

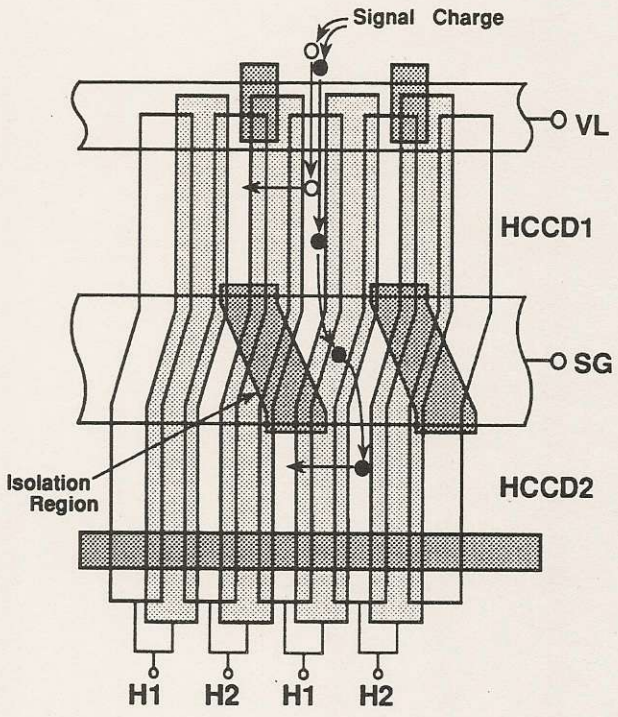


Figure 5 Conventional Dual Channel H-CCD

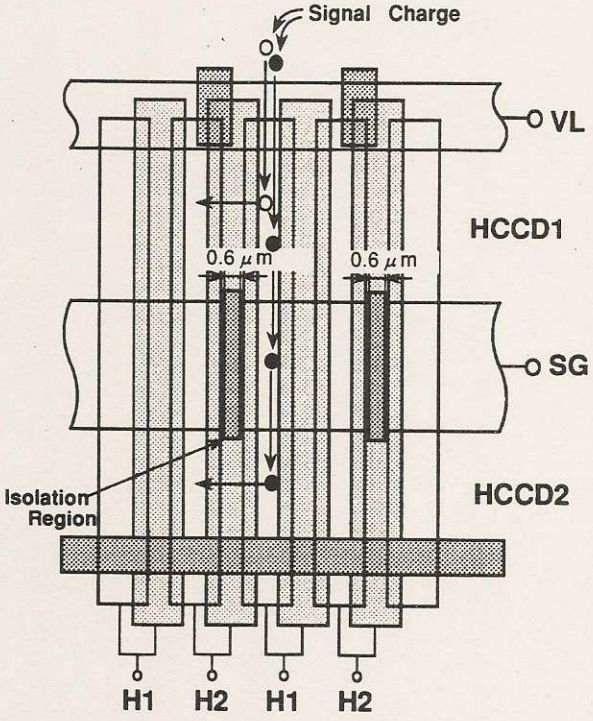


Figure 6 Proposed Dual Channel H-CCD in This Device

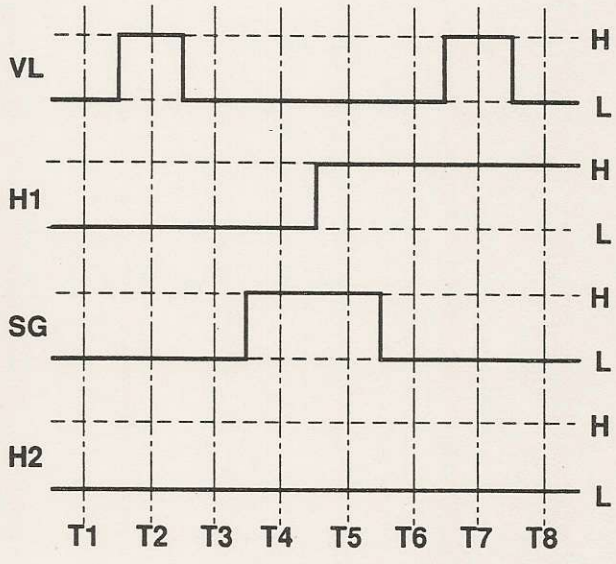


Figure 7 Transfer Timing Diagram of The H-CCD

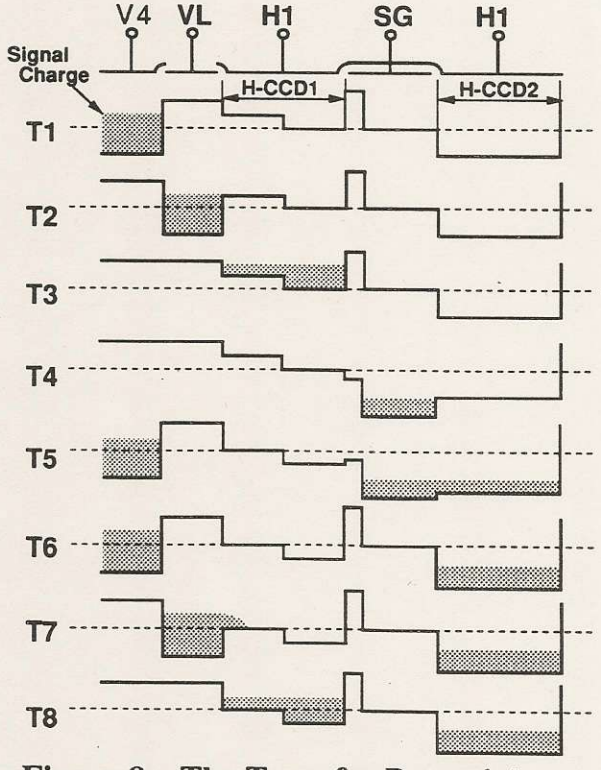


Figure 8 The Transfer Potential of The H-CCD