A modular, high performance, 2 μm CCD-BiCMOS process technology and linear CCD sensor with on-chip electronics

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ABSTRACT

A 2 μm BiCMOS process module has been developed for incorporation into existing high performance 2-phase CCD processes, to enable integration of digital and analog circuits on-chip with the CCD image sensor. The modular process architecture allows integration of CMOS, NPN, or BiCMOS circuits without affecting the baseline CCD characteristics. A trilinear CCD image sensor with on-chip timing generation and Correlated Double Sample was designed and demonstrated.

INTRODUCTION

As previously reported, a 2 μm BiCMOS process module has been developed for insertion into existing linear and full-frame CCD image sensor processes to enable integration of desired analog and digital circuit functions on-chip with the CCD sensor, without affecting the characteristics of baseline CCD [1,2]. A design of experiments approach was used with process and device simulation tools and selected physical experiments, to optimize BiCMOS device performance and process latitude. A summary of the CMOS and NPN device characteristics are provided in Table I. A comparison of the CCD process and device characterisitics is provided in Table II.

Table I - CMOS Device Summary

Device	V_T (V)	V_{dmax} (V)	L_{min} (μm)
P1 N-ch enh	0.94	7.0	2
P1 N-ch dep	-2.3 or -6.3	7.0	2
P2 N-ch enh	0.75	7.0	2
P2 N-ch dep	-2.3 or -6.3	7.0	2
N-ch LDD's	As above	15.0	3
P1 P-ch enh	-0.98	-12.0	2
P2 P-ch enh	-0.75	-12.0	2

Table II - CCD Sensor Characteristics Summary

Group	Storage Region Channel Potential	CCD Transfer Barrier	CCD Transfer Well
Std. CCD	6.50 V (0.12)	0.172 V	0.058 V
CCD + CMOS	6.50 V (0.11)	0.176 V	0.063 V
CCD + BiCMOS	6.45 V (0.13)	0.167 V	0.049 V

Group	Dark Current (nA @ 75C)	Output Noise (mV rms)	Response Uniformity (% peak-peak)	Sensitivity (uV/electron)	CTE (per transfer)	Normalized Yield (Defect Free)
Std. CCD	2.00	0.21	< 5%	> 12.0	> 0.999999	0.80 - 1.0
CCD + CMOS	1.44	0.23	< 5%	> 12.0	> 0.999999	0.80 - 1.0
CCD + BiCMOS	2.25	0.25	< 5%	> 12.0	> 0.999999	0.80 - 1.0

INTEGRATED CCD SENSOR AND ELECTRONICS

After the completion of process development and SPICE parameter extraction, design of a CCD sensor with on-chip electronics was undertaken. This demonstration device consisted of a timing generation circuit, and a Correlated Double Sample, (CDS), circuit integrated onto a standard production trilinear sensor. The basic block diagram is shown in Fig. 1. With the new device, only a master clock, exposure time control signals, and a supply voltage are required to be externally provided. The CCD transfer clocks, and reset clock as well as the CDS clamp and sample clocks are all generated on-chip. The first iteration sensor was designed with one CDS per channel to maintain parallel output capability. A version was also designed with a 3 to 1 multiplexer to provide a single output pin.

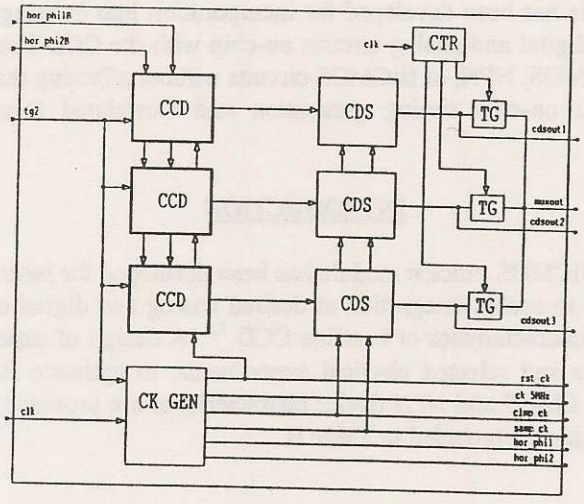

Fig. 1. - Integrated CCD sensor block diagram; each CCD block refers to one channel.

The clock generation circuit was designed with existing 2 μm CMOS standard cells. This circuit contains approximately 400 transistors, and is designed to provide properly aligned clock edges and clock pulse widths that scale with the master clock frequency. The aspect ratio of the layout was designed to facilitate simple placement and wiring into the CCD sensor. The clock generation layout can be seen Fig. 3. Output waveforms from the timing circuit are shown in Fig. 2. In each case a master clock and exposure control signal are the only inputs provided. All output signals appear as expected and scale properly with the frequency of the master clock.

The CDS circuit was a custom design and layout taken from a previous 2 μm CMOS product. It incorporates LDD N-channel devices to allow up to 15 V supply voltages. The CDS portion of the layout can also be seen in Fig. 3. The CDS and timing circuit use an analog ground, that is isolated from the chip substrate, already provided for the production sensor. Measured CDS output signals are provided in Fig. 4. More detailed measured circuit performance data is provided in Table III, (for 2V input swing).

Table III - CDS Circuit Performance Data

Parameter	2μm CMOS Process	CCD-CMOS Process
Gain	0.80 - 0.82	0.70 - 0.72
Linearity	9 - 10 bits	9 -10 bits
Acquisition Time	20 - 25 nS	20 - 25 nS
Sampling Rate	up to 15MHz	up to 12 MHz
Feed Through	10 - 14 mV	12 mV
Input Signal Range	up to 3V p-p	up to 3V p-p
Power Dissipation	70 - 90 mW	70 - 90 mW
Hold Time	10 mS	10mS

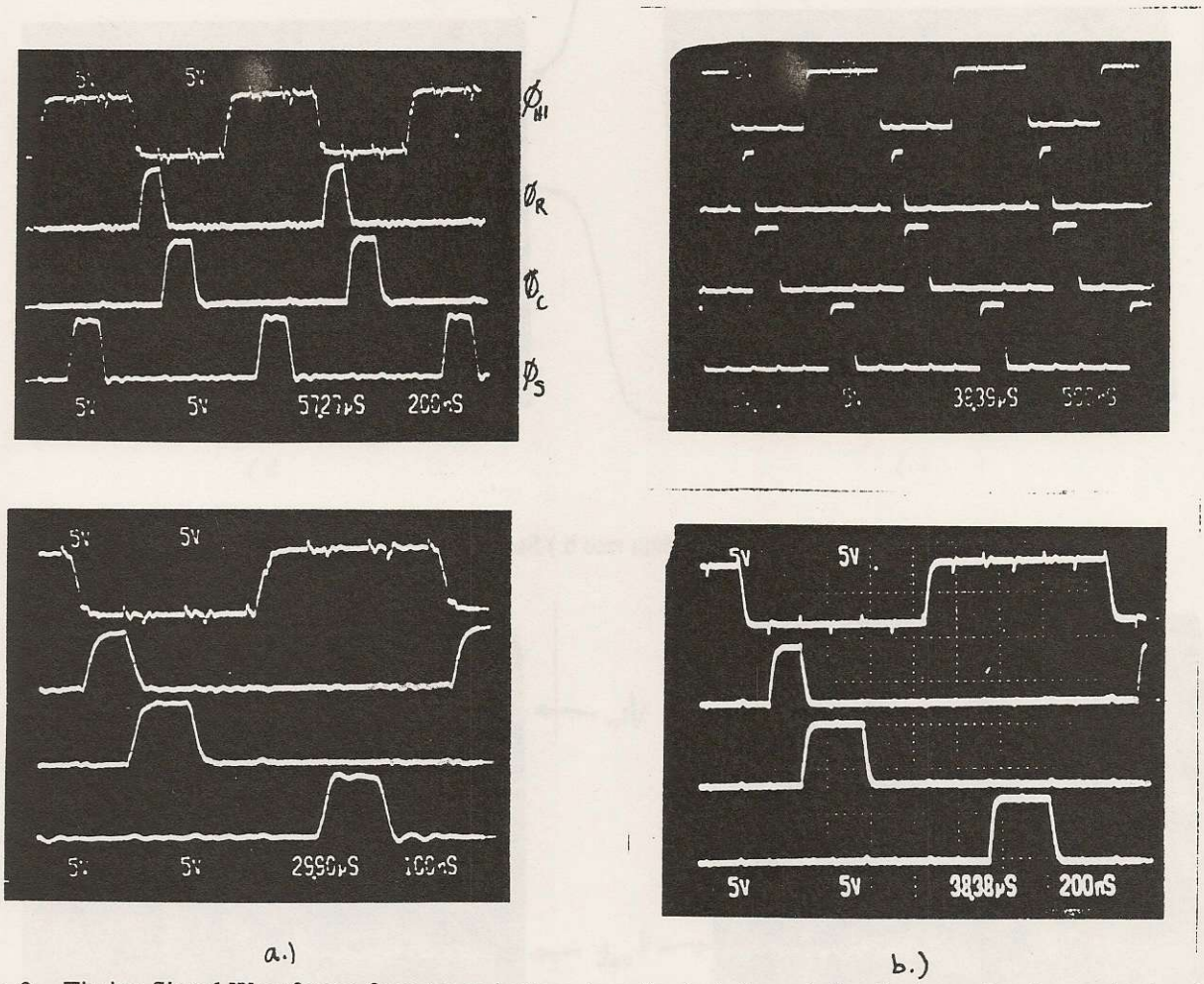

Fig. 2. - Timing Signal Waveforms; from top to bottom, transfer clock 1, reset signal, clamp signal, sample signal; a.) 1.25 MHz data rate b.) 0.75 MHz data rate

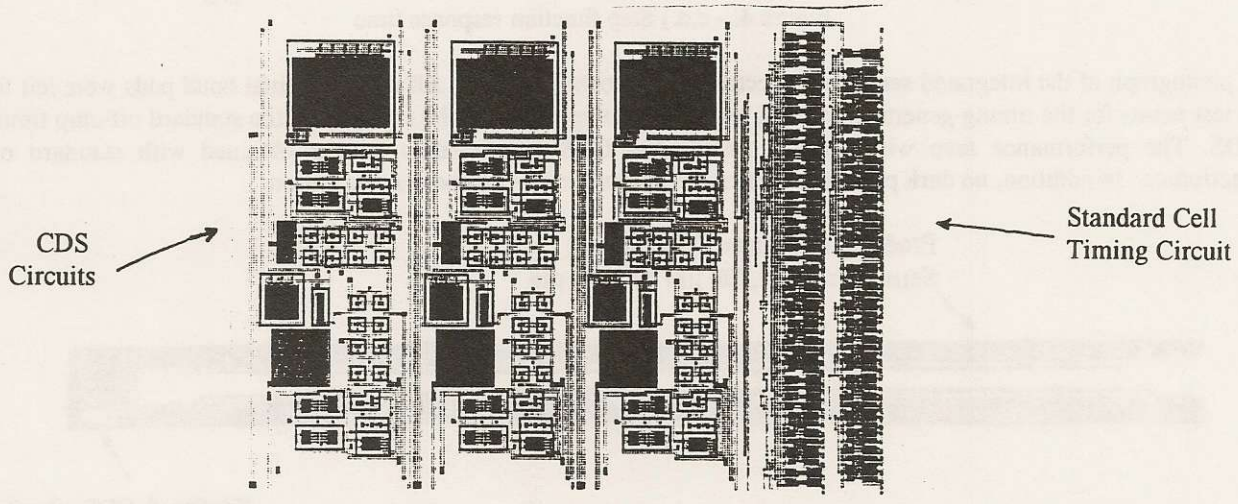

Fig. 3. - CDS and timing circuit layout; dimensions are 1300 μm by 1800 μm.

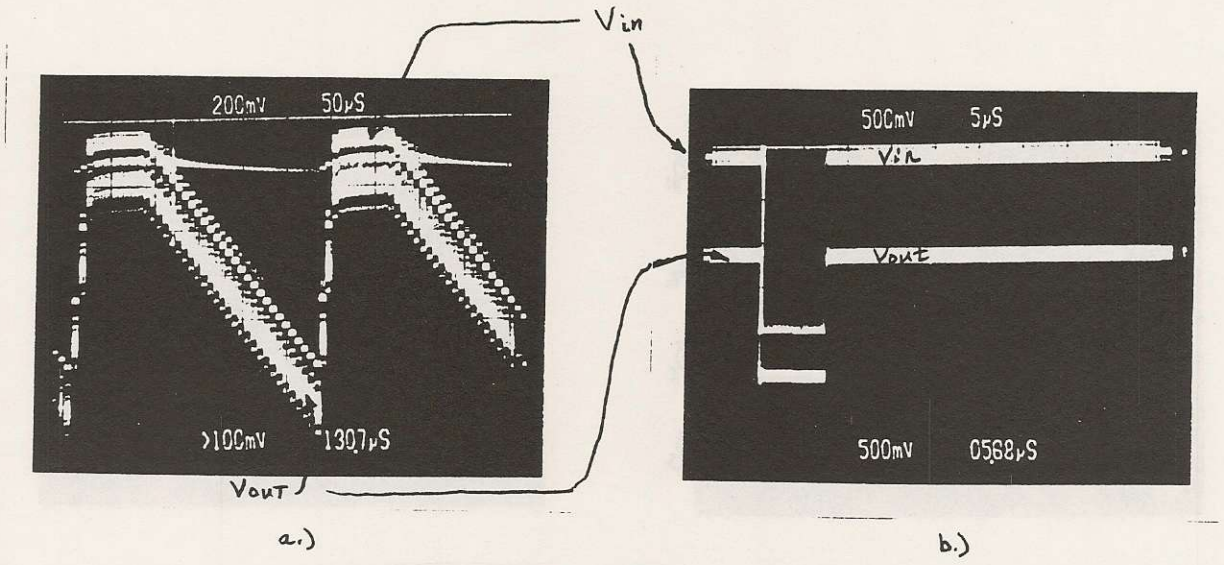

Fig. 4. - a.) Ramped V_{in} vs. V_{out}, ; 10 MHz data rate b.) Step function V_{in} vs. V_{out} ; 10 MHz data rate

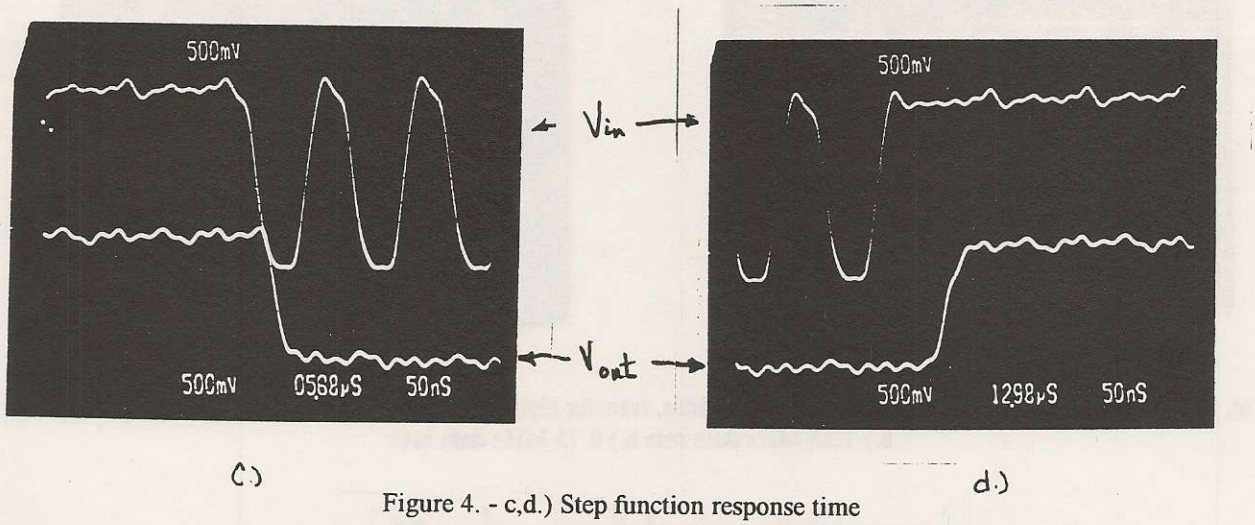

Figure 4. - c,d.) Step function response time

A photograph of the integrated sensor and electronics is shown in Fig. 5. All of the original bond pads were left to serve as test points for the timing generation circuit, and to enable operation of the sensor with the standard off-chip timing and CDS. The performance seen with on-chip timing and CDS is equivalent to that obtained with standard off-chip electronics. In addition, no dark pattern is seen as a result of the on-chip power dissipation.

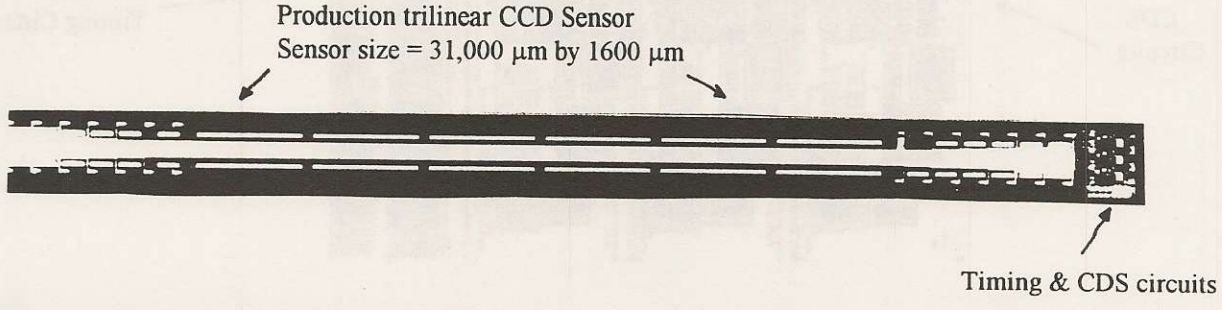

Fig. 5. - Completed integrated sensor; 2098 element per channel; 3-channel linear CCD; Size is 32,500 µm by 2000 µm.

CONCLUSION

A 2 μm BiCMOS process module has been developed for an existing family of CCD image sensor process technologies. The module integration was achieved without altering the baseline CCD process or device characteristics. A linear CCD sensor with on-chip timing generation and CDS was designed and demonstrated. The resulting modular process provides the capability to integrate selected analog and digital circuit functions on-chip with new or existing CCD image sensors. This will enable more effective application specific sensors, and provide the capability to create image sensor systems on a chip.

ACKNOWLEDGMENTS

The authors wish to thank the members of the fabrication department of the Microelectronics Technology Division for their work in fabricating these devices.

REFERENCES

[1] R. M. Guidash et al., "A modular, high performance, 2 μm CCD-BiCMOS process technology for application specific image sensors and image sensor systems on a chip", IS&T/SPIE Electronic Imaging Symposium Tech. Dig., Feb. 1995.

[2] E.G. Stevens, et al., "A 1.4-million element CCD image sensor", ISSCC Tech. Dig., pp. 114-115, Feb. 1987.