TRANSIENT ANALYSIS OF SIGNAL CHARGE TRANSFER IN LONG DIFFUSED REGIONS OF SPECTROSCOPIC IMAGE SENSORS

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ABSTRACT

This paper presents the results of a study of charge transfer time in long doped semiconductor regions. These regions are used to collect and store charge in high performance image sensors. The effect of dopant concentration on charge transfer time was studied using a novel two dimensional device simulation tool. It was found that the delay associated with the long storage region only becomes significant for doping concentrations that are not degenerate. The effect of storage diffusion length on charge transfer time was also studied for degenerately doped structures. For these structures, it was found that the delay is much less than the conventional belief that the delay is proportional to the square of the diffusion dimension the electrons traverse. It was also found that the diffusion dimension affects the charge transfer time indirectly through the back biasing of the transfer MOSFET. Shorter diffusions initially cause a larger back biasing of the transfer MOSFET, decreasing the maximum current flow through the device. To validate these conclusions, experimental image sensor devices were designed that incorporate some of the results discussed above. After being fabricated, these image sensor structures were analyzed to study charge transfer time and the results compared favourably with the computer simulations.

I. Introduction

Spectroscopic applications require a detector that is sensitive over a range of radiation frequencies (usually confined to the visible spectrum) and sensitive to large range of intensities. An array of photodiodes coupled to a CCD shift register can be a sensitive spectroscopic image sensor [1]. In order to maximize active area and preserve spatial resolution, the individual photodiodes of these array sensors (photodiodes) are designed such that the photodiode area is very long and narrow

The spatial geometry of these photodiode detectors can cause an appreciable delay associated with the movement of charge from one end of the photodiode region to the other. It is the magnitude of this delay, the sources of delay, and comparison with other delays in the structure that is the subject of this study. No such study has been reported in the literature.

II. Charge Transfer Theory

In this section, the first order theory of signal charge transfer and the delay of total signal charge transfer from the photodiode diffusion to the CCD read-out shift register is discussed [2, 3].

Figure 1 shows a typical configuration of an integrated photodiode detector with a transfer MOSFET located at one end of the device. For practical reasons, this structure is the most common way to transfer signal charge from the photodiode storage diffusion. Inherent in this design is the delay associated with the movement of charge from one end of the diffused region to the channel of the transfer MOSFET.

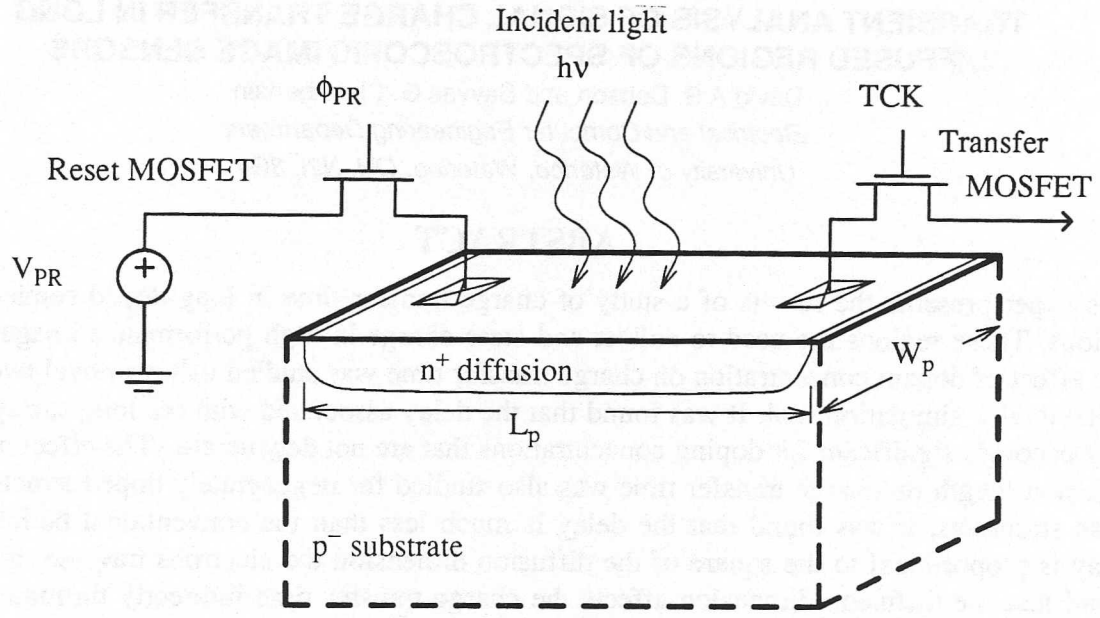

Figure 1: A simple photodiode configuration.

It can be assumed that the majority charge carriers (electrons, in the case of an n^+ diffusion) move through the photodiode storage diffusion by drift due to an electric field. Therefore, the long storage diffusion can be considered as a distributed RC transmission line. The equation for the delay of the line is

$$\tau_{RC} = \frac{rc \cdot L_p^2}{2}, \tag{1}$$

where r is resistance per unit length, c is capacitance per unit length, and L_p is the length of the diffusion. This formula can be used to approximate the storage diffusion transfer delay based on doping changes.

The transfer MOSFET delay can be estimated by using Burns' expression [4]:

$$\tau_{FET} = \frac{4}{3} \frac{L_{eff}}{\mu_n (V_{GS} - V_{TH})}, \tag{2}$$

where L_{eff} is the effective gate length of the MOSFET, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage of the MOSFET, and μ_n is the mobility of the electrons. This expression applies to MOSFETs operating in saturation.

III. Two Dimensional Device Simulations

The photodiode structure of Figure 1 was simulated under steady state and time-varying conditions using the CHORD 3.0 two dimensional device simulator [5]. The simulations were carried out using the drift-diffusion transport model. Six devices were simulated, each with a photodiode structure 200μm long (L_p) and 10μm wide (W_p), and composed of an n^+ diffusion in a p-type ($N_A = 2.5 \times 10^{15}$ cm^{-3}) substrate. The TCK n-channel MOSFET has a drawn gate length of 6μm and an actual gate length of approximately 5μm.

Steady state simulations were carried out on each device to characterize it and to bias the device for transient simulation. A fixed amount of charge (the signal charge) was placed in the photodiode storage diffusion by placing an external bias on the diffused region. A transient simulation was performed using the results of the steady-state simulation as initial conditions. During the transient simulation, the voltage on the transfer MOSFET gate was swept to a constant value, V_{GBmax}, above the threshold voltage of the MOSFET. The surface potential of the channel centre in steady state conditions with the maximum simulation voltage on the gate was used as a reference for the signal charge transfer time. The signal charge was considered to be transferred when the potential of the storage diffusion reached this reference.

III.1. Effect of photodiode doping on charge transfer time

The doping profile of the n^+ diffused region was modified during simulation in order to study the effect of dopant density on charge transfer time. Four devices were simulated with decreasing doses of implanted donor atoms. The surface concentration of donor impurities was such that one device was degenerately doped (Device 1), one device was highly doped (Device 2), one device was moderately doped (Device 3), and one device had low doping (Device 4).

After completing the simulations, the surface potential and electron concentration at various locations in the structures were extracted from the solutions and analyzed. The degenerately doped device stores the most charge and consequently had the highest amount of current flow out of the storage region.

The charge transfer time for each device is summarized in Table 1.

Device	N_D (cm^{-3})	FET L_{eff} (μm)	t_{THEORY}	t_{SCT}
1	3.5×10^{20}	5.22	0.55ns	10ns
2	7.5×10^{18}	5.20	0.65ns	22ns
3	3.5×10^{17}	5.16	4.1ns	70ns
4	3.5×10^{16}	5.00	40ns	600ns

Table 1: Comparison of theoretical signal charge transfer delay ($t_{diff} + t_{FET}$) to simulated results for Devices 1 to 4. t_{THEORY} is the theoretical delay time, and t_{SCT} is the delay extracted from simulation results.

The theoretically calculated delay according to Equation (1) is given in the table as t_{THEORY}, which is at least an order of magnitude smaller than the extracted transfer time t_{SCT}. However, it can be noted that t_{SCT} follows the trend of t_{diff}. Therefore, first order theory indicates the trend in increasing signal charge transfer time t_{SCT} for decreasing impurity doping, but does not give accurate individual results.

III.2. Effect of photodiode length on signal charge transfer time

In addition to these simulations, two other devices were analyzed, one (Device 5) having a 100μm long photodiode region and the second (Device 6) having a 400μm long photodiode region. The photodiode regions of Devices 5 and 6 were degenerately doped (the same doping as Device 1). Both devices were simulated using exactly the same procedure as was used for Devices 1 to 4. The charge transfer delay was expected to have a quadratic dependence on photodiode length, L_p, according to Equation (1). However, simulation results showed that this was not the case. Table 2 summarizes the the charge transfer time t_{SCT} as extracted from the simulation results. The relationship of photodiode region length to transfer delay suggested by this data

is a linear one, rather than quadratic, since t_{SCT} for L_p = 200μm is about twice that for L_p = 100μm and t_{SCT} for L_p = 400μm is about four times that for L_p = 100μm.

Device	Length (μm)	t_{SCT}
1	200	10ns
5	100	4.5ns
6	400	17ns

Table 2: Signal charge transfer time t_{SCT} as a function of photodiode storage region length.

The current through the longer device (Device 6) was always greater than the current in Devices 1 and 5. The reason for this is related to the size of the charge packet to be transferred. As the transfer MOSFET turns on, a specific amount of charge flows from the source of the MOSFET (the photodiode storage region) to form the inversion layer in the channel. This amount of charge is the same size for Devices 1, 5 and 6 since the MOSFET is the same size. However, this channel charge is a much larger percentage of the total signal charge packet in Device 5 than in Devices 1 and 6. Consequently, the surface potential of the storage region in Device 5 goes to a more positive level and the MOSFET sees a larger source to substrate bias, reducing the current through the device due to the back-bias effect. Hence, the delay of the transfer MOSFET depends inversely on the length of the photodiode storage region. This relationship combined with the quadratic relationship of Equation (1) leads to an overall linear relationship.

IV. Experimental Results

Experimental devices were fabricated in two different processes and subsequently tested. This structure is slightly different than the device structure simulated using CHORD: the reset MOSFET is integrated and the charge from the photodiode is transferred to a floating diffusion rather than a reverse-biased drain. The voltage change of the floating diffusion as a result of signal charge entering it is sensed by a buried-channel MOSFET. This MOSFET was connected in an source-follower configuration for testing.

The mask layout for a photodiode structure was designed and fabricated on a CMOS fabrication process using the Mitel Semiconductor foundry.

In addition to these experimental structures, devices were donated by DALSA Inc., a CCD image sensor company. These devices have the same structure as Mitel devices, but slightly different dimensions, and were fabricated on a specifically tailored CCD fabrication process.

The delay time measured using this procedure includes the response time of the buried-channel MOSFET, and hence the delay time was expected to be greater than simulated results. 3.

Device	L_p (μm)	BCFET W/L	t_r	t_{SCT}
DALSA	325	70/6	100ns	20ns
Mitel A	200	90/6	20ns	15ns

Table 3:

Signal charge transfer time t_{SCT} as observed from experimental device tests. L_p is the length of the photodiode storage region, the aspect ratio of the output buried-channel MOSFET is listed under 'BCFET', and t_r is the rise time of the output signal voltage.

These results represent the average values of the tested devices; the deviation between devices was very small. The observed delay time difference (5ns) compares favourably to that between the 400μm and 200μm simulated device results (7ns), recorded in Table 2.

V. Conclusions

The signal charge transfer time for long and narrow photodiode diffusions was studied using computer simulations and experimental devices. The dependence of this transfer time or delay on photodiode doping profile was investigated and is shown in Figure 2. As the doping of the photodiode diffusion increases, the signal charge transfer time decreases and becomes limited by the response time of the transfer MOSFET.

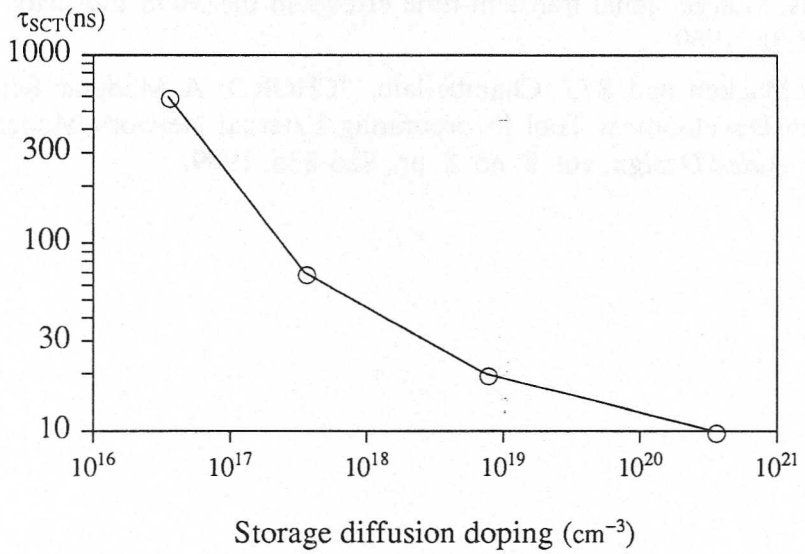

Figure 2: Signal charge transfer time t_{SCT} as a function of photodiode doping (N_D) from simulation results. Photodiode length is 200μm and width is 10μm.

The length of the photodiode region also affects the charge transfer time, but in a linear relationship, not a quadratic one as is predicted with first order theory. It was found that the length affects the bias conditions of the transfer MOSFET during charge transfer. Part of the signal charge in the photodiode region becomes inversion charge in the MOSFET and the percentage of this charge to the total charge packet determines the resulting potential of the photodiode diffusion and hence the back bias on the transfer MOSFET. The results of the computer simulations are supported by measurements of experimental test devices.

VI. Acknowledgements

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VII. References

[1] P.M. Epperson, J.V. Sweedler, R.B. Bilhorn, G.R. Sims, and M.B. Denton, "Applications of Charge Transfer Devices in Spectroscopy", *Analytical Chemistry*, vol. 60, no. 5, pp. 327A-335A, 1988.

[2] S.G. Chamberlain and B.Y. Woo, "Transient Analysis of Electrical Charge Injection into Charge-Coupled Devices", *Int. J. Electronics*, vol. 40, pp. 569-586, 1976.

[3] M.H. Elsaid, S.G. Chamberlain, and L.A.K. Watt, "Computer Model and Charge Transport Studies in Short Gate Charge-Coupled Devices", *Solid-State Electronics*, vol. 20, pp. 61-69, 1977.

[4] J.R. Burns, "Large-signal transient-time effects in the MOS transistor", *RCA Review*, vol. 30, pp. 15-35, 1969.

[5] J.R.F. McMacken and S.G. Chamberlain, "CHORD: A Modular Semiconductor Device Simulation Development Tool Incorporating External Network Models", *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 8, pp. 826-836, 1989.