Frame-Transfer CCD's with All-Gates Pinning: Device Modelling and Dark Current Evaluation

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Abstract

A Frame-Transfer CCD for consumer applications was developped with drastically reduced dark current by using hole accumulation at the entire Si-SiO_2 interface of the image pixel during integration, called *All-Gates Pinning*, or *AGP*. Vertical anti-blooming and electronic shutter was not compromised.
This presentation will focus first on the device modelling of the imager, and then on dark current and fixed-pattern measurement results obtained on the device. It will be shown that process modelling combined with 3-D device modelling provides accurate predictions of sensor performance. Measurements at 80°C show a 30 times lower dark current, and 6 times lower FPN with AGP compared to conventional mode.

Introduction

At the 1992 IEDM, we presented a 1/3" FT-CCD imager which incorporates *All-Gates Pinning* (**AGP**) operation to drastically reduce the dark current and fixed-pattern noise by shielding the Si-SiO_2 interface with a layer of holes [1]. The two-phase, two-poly image pixel is illustrated in Fig.1. A DN n-channel implant on a profiled DP p-well is used for VAB. Channel stops are made with the SP implant. A maskless shallow SPM implant controls the potential in the window areas. The present paper deals with two aspects of the introduction of AGP in a consumer FT CCD: *device modelling* and *dark current evaluation*.

Device Simulations

Available simulation tools
Four types of device simulations are currently used in the design of our CCD's:

- *RC network simulations* e.g. to check the maximum frame shift frequency,
- *1-D and 2-D process simulations* e.g. to estimate the dopant profiles,
- *2-D and 3-D electrostatic device simulations* e.g to optimize the npn structure for anti-blooming,
- *2-D and 3-D transient device simulations* e.g. to characterize the transport from serial register to the floating diffusion [2].

This presentation will focus on *3-D electrostatic device simulations* using *PADDY*, since this is the most efficient device simulator for image pixel optimisation.

Conditions for efficient anti-blooming and all-gates pinning
Previous CCD imagers developed at Philips Imaging Technology already used extensive device simulation to optimize the vertical anti-blooming structure and output gate area [2,3]. We have expanded this technique to optimize the sensor performance in AGP mode. Fig.2 shows the requirements for efficient anti-blooming [3] and for all-gates pinning for an empty pixel next to a full pixel.
A full well (maximum charge packet) is found during integration when

- the barrier to the substrate for the full well Δ VAB = 0.4V,
- the lateral barrier between neighboring pixels Δ VLB > 0.6V
- the barrier of the charge packet to the surface Δ VSB > 0.25V
- the whole surface is in deep inversion, both for the empty and for the full pixel

Inputs for 3-D electrostatic simulations
For the 3-D electrostatic simulation program PADDY [4], the silicon and the gate structure are defined (thickness, dielectric constant, etc.) The dopant profiles resulting from the process simulations performed with SUPREM3 [5] are included in the silicon definition, e.g. by means of a Gaussean fit function. Lateral outdiffusion is modelled with an error function. Voltages are applied to the gates and the Fermi-levels of holes and electrons are defined for different regions in the semiconductor material.

Simulation runs
Adjustable parameters are gate voltages (integration voltage, low and high transport voltages); dopant profiles and the Fermi-level of electrons and holes. The Fermi-level in the top layer of silicon can be adjusted to represent a certain amount of charge in the potential well associated to the image pixel.

- Integration: A solution is found when
  - the above-mentioned conditions for VAB and AGP are satisfied (Δ VAB = 0.4V, Δ VLB > 0.6V, Δ VSB > 0.25V, deep inversion at the surface)
  - sufficient charge can be stored
  - the charge collection volume extends sufficiently wide and deep to obtain good quantum efficiency
- Transport: No potential barrier should be present in the CCD channel in transport direction with 10V clockswing. These simulations essentially determine the maximum implant dose for the two-phase implant.
- Variable Integration Time: With this sensor, electronic shuttering is obtained by flushing the already collected electrons in the image pixel from the CCD-well to the n-substrate. This should be obtained with the image gates at pinning voltages and the storage gates at transport voltages when a pulse is given to Nsub. No significant potential barrier towards Nsub should be present in the image pixel (2-D transient simulations with CURRY show a potential barrier < 0.1V allows full electronic shutter within 10 μs); a sufficient barrier (> 0.6V) should be maintained in the storage section to hold maximum charge packets.
- Tolerancing : Variations in geometry and dopant profile within the process tolerances should not degrade the above-mentioned requirements.

Results:
Since the cell is symmetrical, only half the width was simulated. Fig.3 shows the input structure for the PADDY simulations. Starting from a conventional npn structure, a combination of XA gate length and DN2 implanted dose is calculated that fulfils the requirements of good integration (Fig.4) and transport (Fig.5). The pinning condition under the gates is reached by adjusting the offset between gate voltage and the p-well voltage (i.e. Fermi-level of holes). Then the implant SPM is adjusted to achieve pinning also in the windows (Fig.6). With a profiled p-well (implanted through stripes) in the image section and a blanket p-well implant in the storage section, the conditions for electronic shutter by a pulse on Nsub are checked (Fig.7).
A typical run with 50 000 mesh points will run approximately 10 minutes on a HP 9750.
Good agreements were found between measurements and simulations, e.g. for maximum charge capacity, operating voltages for pinning, and required Nsub-voltage for electronic shutter.

Dark Current Evaluation

The dark current of the image pixel at 80°C is reduced from 4 nA/cm^2 to about 0.15nA/cm^2 by going from conventional to pinned operation.
The fixed-pattern noise (FPN) of the device was measured using an 8-bit digital image processor Series 151 from Imaging Technology. Fig.8 shows a histogram of the FPN obtained at 80°C by averaging 8 images for the device operating in conventional non-AGP mode ('AGP off') and in AGP mode ('AGP on'). A reduction in FPN (σ-value) with a factor of six is measured. Fig.9 shows the histogram of FPN for 'AGP on' for different temperatures. More detailed results will be presented at the workshop.

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References
[1].J. Bosiers et al., "A S-VHS compatible 1/3" 720(H) * 588(V) FT-CCD with low dark current by surface pinning", Proc. IEDM'93 pp.97-100.
[2].A. Theuwissen et al., " A 2.2 Mpixel FT-CCD imager according to the Eureka HDTV standard", Proc. IEDM'92 pp.167-170.
[3]. J. Bosiers et al.," A 2/3 in 1187(H) * 581(V) S-VHS compatible Frame-transfer CCD for ESP and Movie Mode", T-ED vol.38 no.5, pp 1059-1068, 1991.
[4]. S.J. Polak et al., " Semiconductor device modelling from the numerical point of view", Int. Jnl. Numerical Methods in Engineering, vol. 24 pp-763-838, 1987.
[5]. SUPREM3 is a 1-D process analysis program by Technology Modeling Associates, Inc.

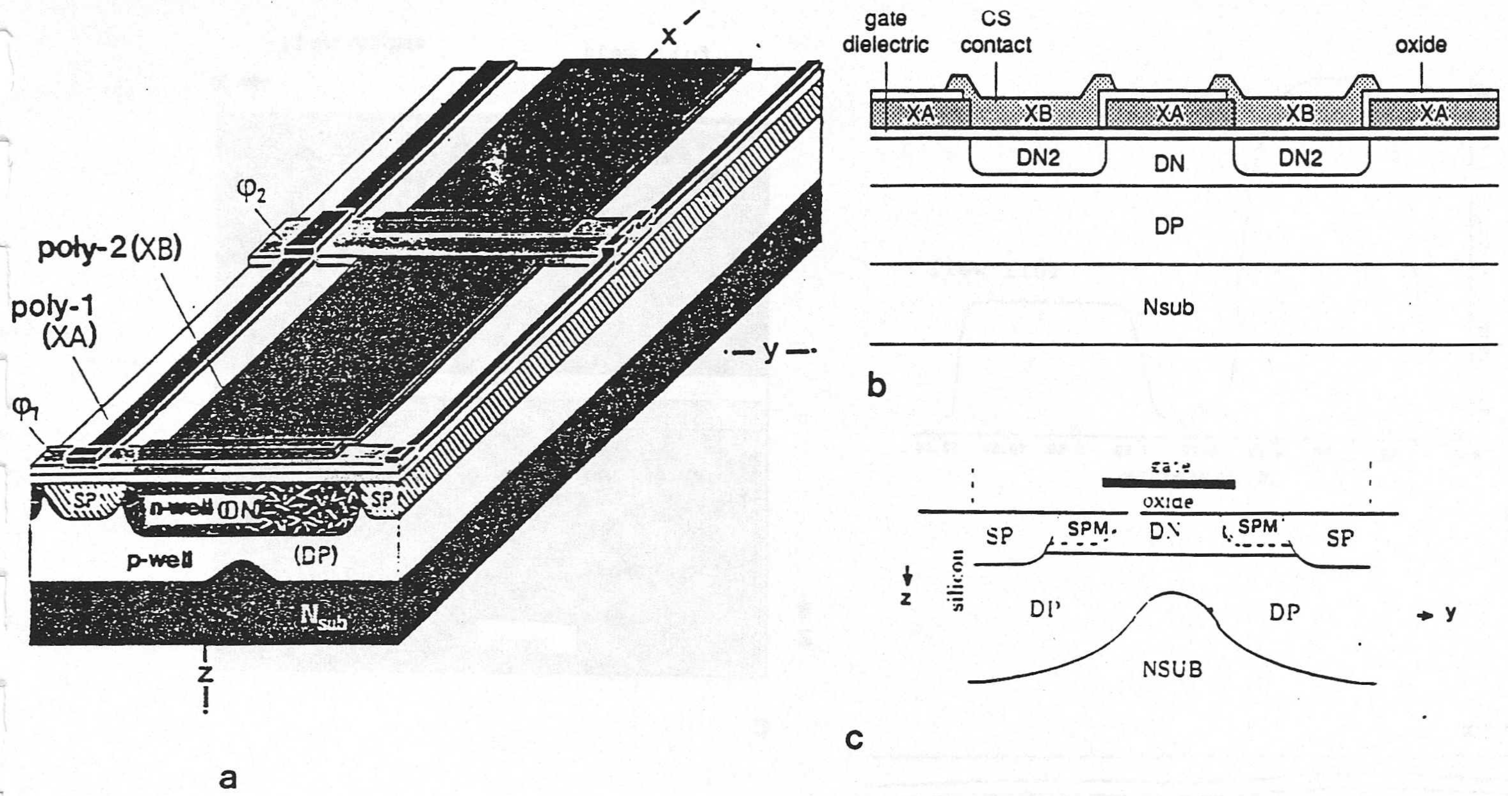


Fig.1. The image pixel of the AGP FT-CCD.
a. perspective view of image cell
b. Cross section along transport direction (x-x)
c. Cross section across the columns (y-y)

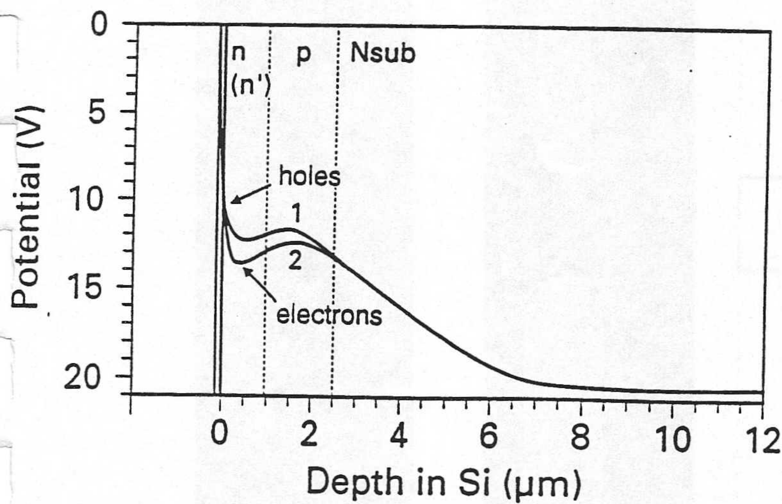


Fig.2. Required potential profiles for VAB operation with AGP under poly-1 (curve 1) and poly-2 (curve 2)

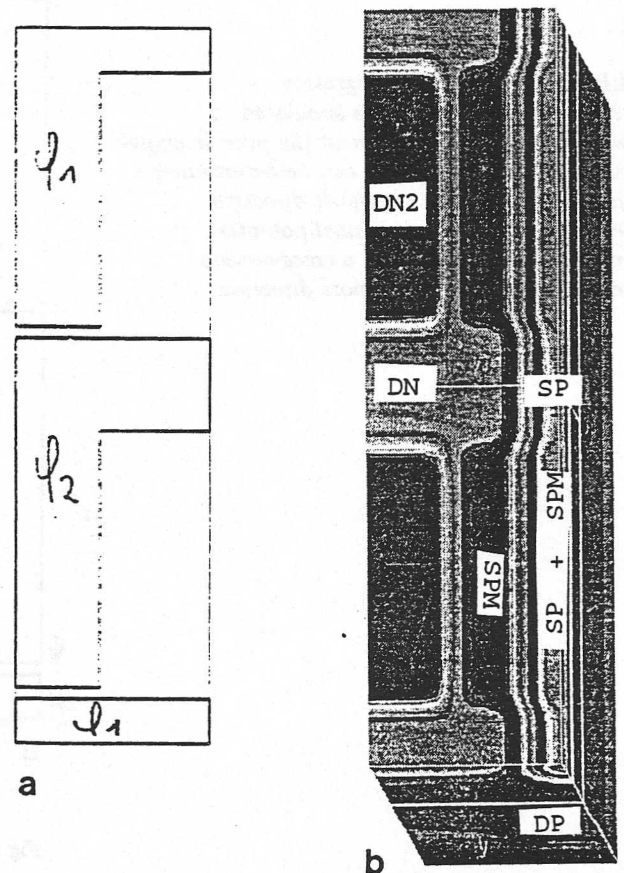
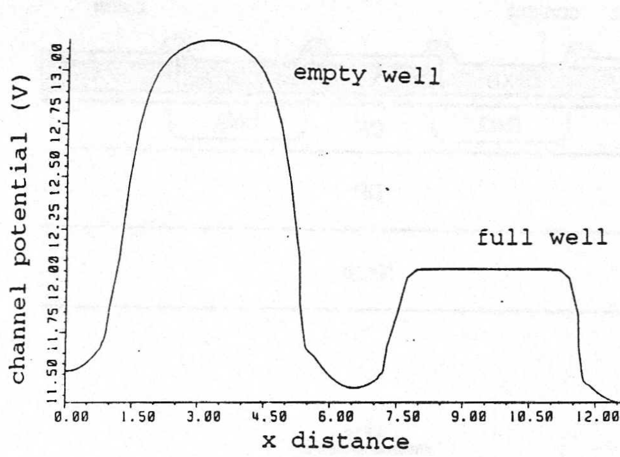
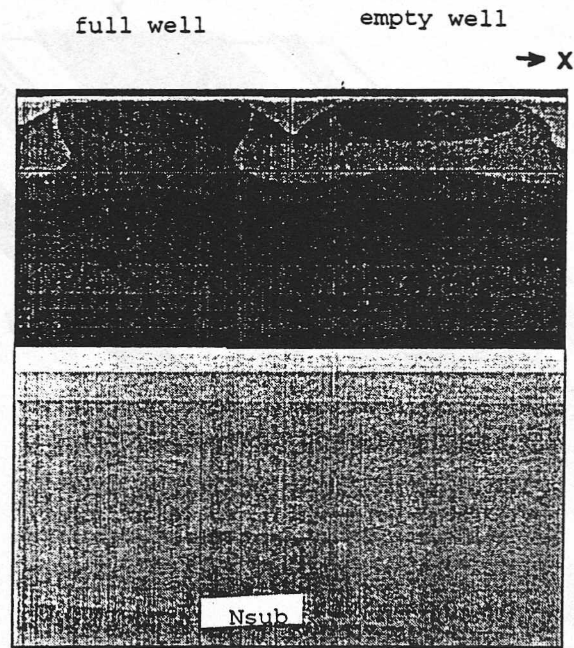


Fig.3. PADDY input structure for 3-D simulations
a. Electrode structure
b. Lines of equal doping concentration





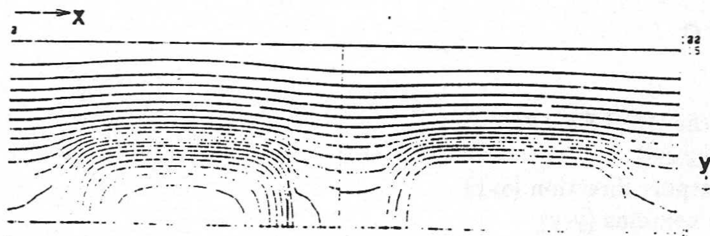


Fig.4.PADDY output for integration.
The right halve of the pixel is simulated to full well capcity, the left halve of the pixel is empty
Δ VAB, Δ VLB and Δ VSB can be determined.
a. *Channel potential in transport direction*
b. *Contour lines of equal channel potential.*
c. *Lines of equal potential in a cross-section in the middle of cell in transport direction*

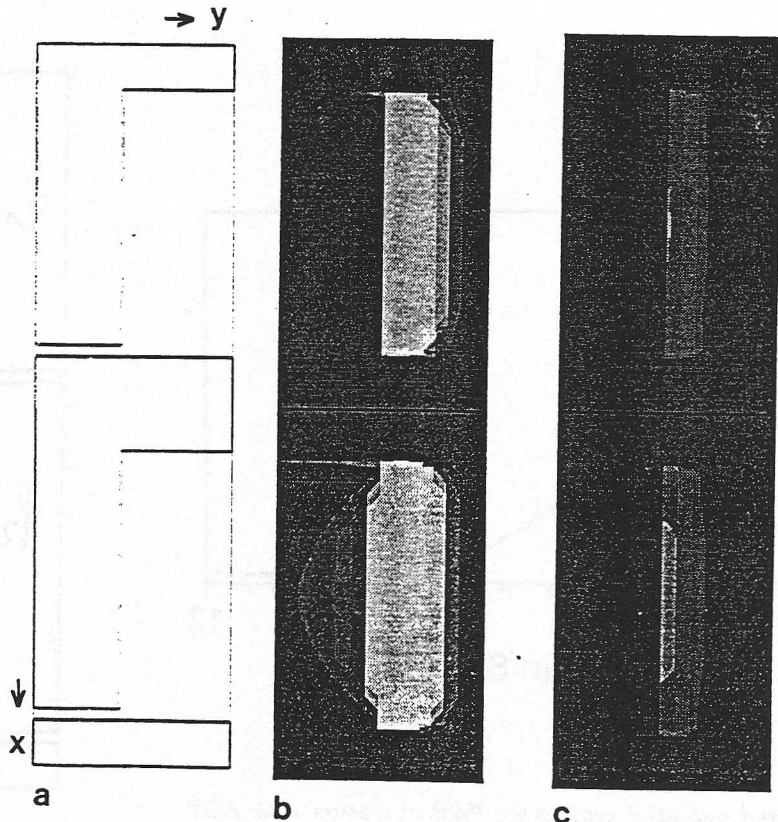


Fig.5. PADDY output for integration adjusted for pinning.
a. gate and window geometry
b. Hole concentration at the surface with conventional SPM implant
c. Hole concentration at the surface with adjusted SPM implant

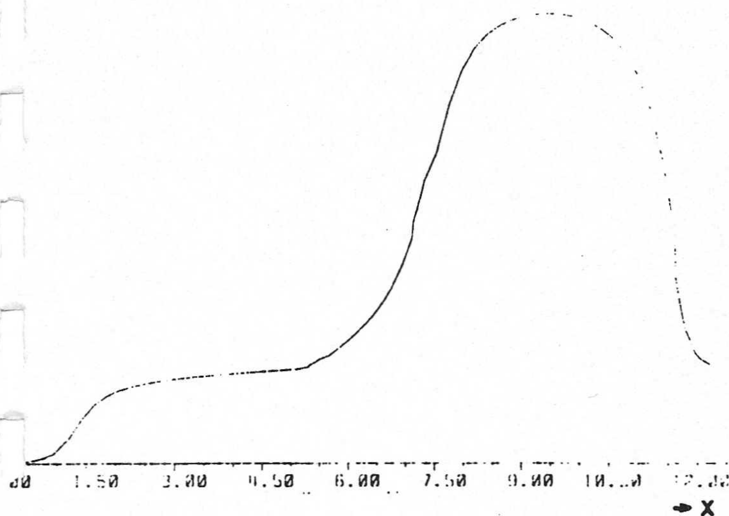


Fig.6. PADDY output for transport: Channel potential in transport direction

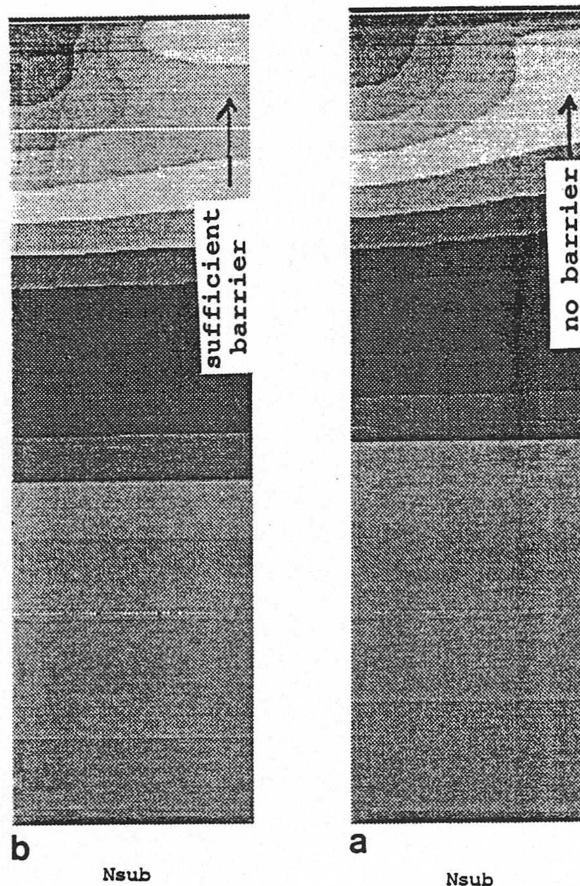


Fig.7. PADDY output for charge reset
Cross-section perpendicular to the transport direction, in the middle of the charge collection gate.

a. for the image pixel
b. for the storage cell

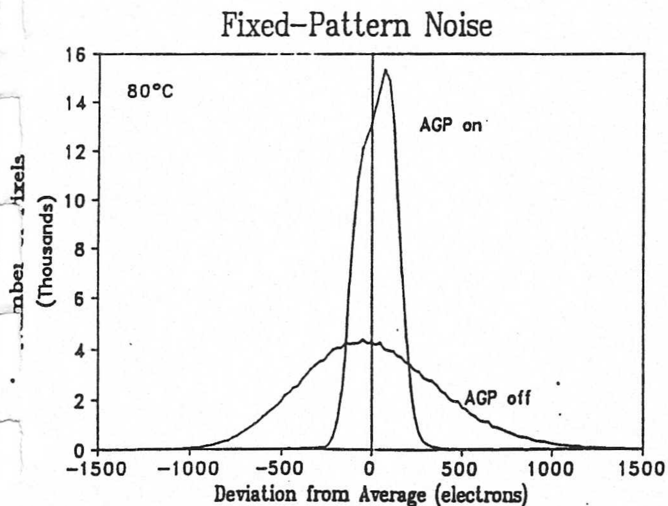


Fig.8. FPN for 'AGP on' and 'AGP off'

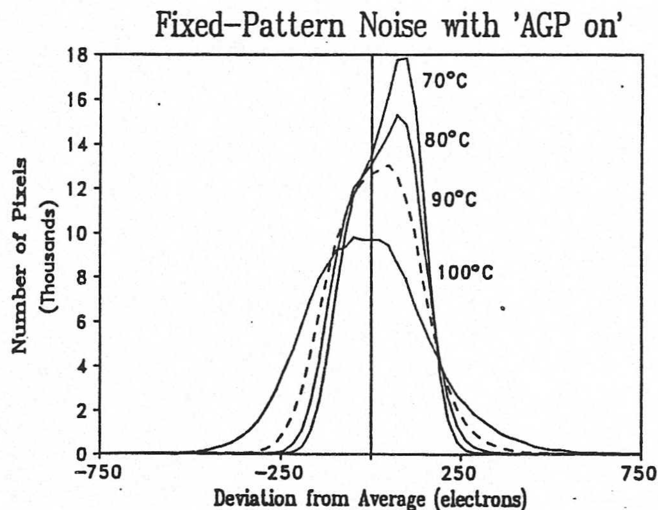


Fig.9. FPN as a function of temperature for 'AGP on'