INVESTIGATING THE UNIPHASE OPERATION OF A GaAs RESISTIVE GATE CHARGE-COUPLED DEVICE USING TIME DOMAIN TECHNIQUES

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Abstract: The ability to operate a GaAs resistive gate charge-coupled device (RGCCD) in the UHF band using a uniphase clock provides electronic circuit advantages over multiphase clocking methods. The requirement for multiple clocks having phase correlation is unnecessary resulting in a considerable reduction in the complexity of the electronic circuits required to operate the RGCCD. This is especially important for the 500 MHz multi-channel GaAs RGCCD transient digitizer system currently being developed at TRIUMF. In order to achieve further insight into the high speed uniphase operation of a GaAs RGCCD, an investigation using time domain techniques was undertaken. Two results were obtained from this investigation. The first result, was the indirect observation of charge transfer within the RGCCD. This provides information regarding the quantity of signal charge that can be supported within the RGCCD channel and gives details as to the maximum frequency the device can be expected to operate at. Our experimental observations indicate a maximum worst case operating frequency of approximately 1 GHz, for a 128-pixel GaAs RGCCD operating in a quiescent state with each pixel containing a "full" well of charge of approximately 20 fC per pixel. The second result was the development of an equivalent circuit for modelling the parasitics of the RGCCD transport region. This model is an appropriate design aid for devising wide bandwidth clock circuits for operating a GaAs RGCCD.

Introduction

The GaAs "resistive gate" charge-coupled device (RGCCD) was developed in 1982 by Higgins et al.[1] for UHF applications[2,3]. Devices were operated at frequencies approaching 1 GHz with $\eta \rightarrow 0.999$[4]. It has been predicted that the GaAs RGCCD should be capable of operating at frequencies up to 6 GHz[5]. Although this is theoretically possible, it proves to be quite challenging to attain reasonable performance at clock frequencies beyond 1 GHz. This partially stems from the difficulties encountered with operating the RGCCD using a traditional multiphase clock, as it is necessary to maintain a consistent phase relationship over a wide bandwidth. To overcome this limitation, a novel uniphase mode for operating the RGCCD was developed at TRIUMF[6]. This method of operation takes advantage of the surface potential control offered by the resistive gates; permitting an externally applied d.c. electric field to direct the motion of charge along the channel. Since the motion of charge along the channel is governed externally, there is no need to employ a "built-in" electric field mechanism, resulting in reduced device fabrication complexity. Furthermore, the electronic circuits required to operate the RGCCD using a uniphase clock are considerably simpler than those used in multiphase clocking schemes, providing cost benefits for electronic systems employing significant quantities of these devices.

In this work, we describe two results obtained from time domain measurements taken from a RGCCD clocked using the uniphase clock technique. The first, considers the indirect observation of charge transfer within the device, confirming the principle of uniphase operation. It also provides quantitative information regarding the amount of charge that can be supported within the channel and an indication of the maximum frequency the device can be expected to operate at. The second, is the presentation of an equivalent

circuit for modelling the parasitics of the RGCCD transport region in the "empty well" mode and its associated packaging. A brief description of the 500 MHz multi-channel GaAs RGCCD transient digitizer currently being developed at TRIUMF will also be given.

Principle of Operation

A review of the uniphase mode of operating the GaAs RGCCD is given below. The motion of a packet of charge along the RGCCD channel is shown in Fig. 1. Four transport electrodes labelled: $\phi 1$, $\phi 1a$, $\phi 2$ and $\phi 2a$ comprise a pixel. The electrodes are d.c. biassed using voltages: V_1, V_{1a}, V_2, and V_{2a} that are adjusted so that

$$V_2+v_{c,max} > V_{1a}+v_{c,max} > V_1 > V_{2a} > V_2+v_{c,min} \quad (1)$$

where $v_{c,min}$ and $v_{c,max}$ correspond to the minimum and maximum clock voltage levels of the clock waveform $v_c(t)$ applied to the $\phi 1a$ and $\phi 2$ electrodes. The electron potential energy, E, within the channel below the electrodes varies as the negative of the applied voltage when negligible charge exists in the channel and (1) yields

$$E_1 < E_{1a} > E_2 > E_{2a} > E_1 \quad (2)$$

for $v_c(t)=v_{c,min}$ and

$$E_1 > E_{1a} > E_2 < E_{2a} > E_1 \quad (3)$$

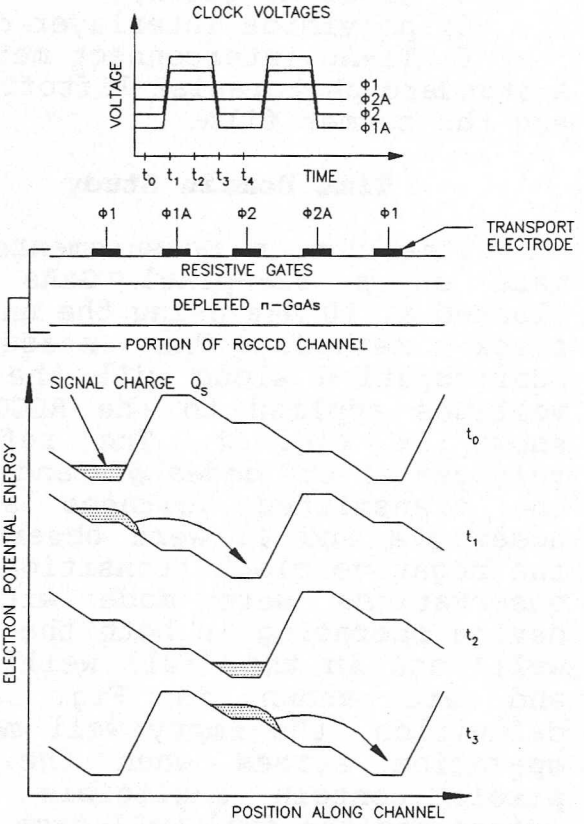

Fig. 1 Uniphase operation of a GaAs RGCCD.

for $v_c(t)=v_{c,max}$. The implication of (2) and (3) is that a potential well is formed under the $\phi 1$ or $\phi 2$ electrode on the negative or positive levels of the applied clock waveform. Referring to Fig. 1; at $t=t_0$, the clock is at its minimum and (2) is true. Assume that a small quantity of electrons, with signal charge magnitude $Q_S \approx 0$, is introduced into the channel (Q_S is small so as to negligibly perturb the local potential energy). This charge will be drawn towards the energy minima below the $\phi 1$ electrode . On the positive clock transition occurring at $t=t_1$ through to $t=t_2$ a potential well forms below the $\phi 2$ electrode as (3) becomes true, resulting in the motion of the signal charge Q_S along the channel from $\phi 1$ through $\phi 1a$ to $\phi 2$. The channel potential varies monotonically between the transmitting and receiving potential wells during the transfer period as a consequence of the surface potential control offered by the resistive gates[7,8]. This transfer process similarly occurs on the negative clock transition from $\phi 2$ through $\phi 2a$ to $\phi 1$ at $t=t_3$ resulting in the charge packet being shifted along one pixel of the RGCCD at $t=t_4$.

Fabrication

The GaAs RGCCDs investigated in this work were fabricated at TRIUMF on 3 inch GaAs epi-wafers. A 0.28 μm thick uniformly doped $N_D=5 \cdot 10^{16}$ cm^{-3} n-GaAs film comprised the device active layer. A nominal 1.5 μm thick p^--GaAs film unintentionally doped $N_A \leq 2 \cdot 10^{14}$ cm^{-3} acted as a buffer between the undoped LEC

GaAs substrate and the active layer. The epitaxial films were grown using MOCVD. Device fabrication employed conventional 1 μm contact photolithography to define the patterns for the following:

1) Au/Ge-Ni-Au ohmic contacts,
2) 35 keV and 200 keV H^+ bombarded isolation implants,
3) 500 kΩ/□ Cr:SiO cermet resistive gates,
4) Cr-Pt-Au gates,
5) polyimide interlayer dielectric film,
6) Ti-Au interconnect metallization.

A standard photoresist liftoff method was used to pattern the metallizations and the cermet film.

Time Domain Study

Time domain measurements were made on a 128-pixel GaAs RGCCD clocked at 10 MHz using the uniphase clock method. The measurement configuration along with the clock voltages applied to the RGCCD are shown in Fig. 2. The reflected voltages at the nodes **ϕ**1a and **ϕ**2 and the transmitted voltages at the nodes **ϕ**2a and **ϕ**1 were observed on the negative clock transitions. The observations were made with the device operating in both the "empty well" and in the "full well" modes and are shown in Fig. 3. By definition, the empty well mode of operation arises when the RGCCD pixels contain negligible signal charge and the full well case occurs when each pixel contains the maximum signal charge. The influence of the signal charge is demonstrated by the observed difference between the empty well and the full well voltage responses.

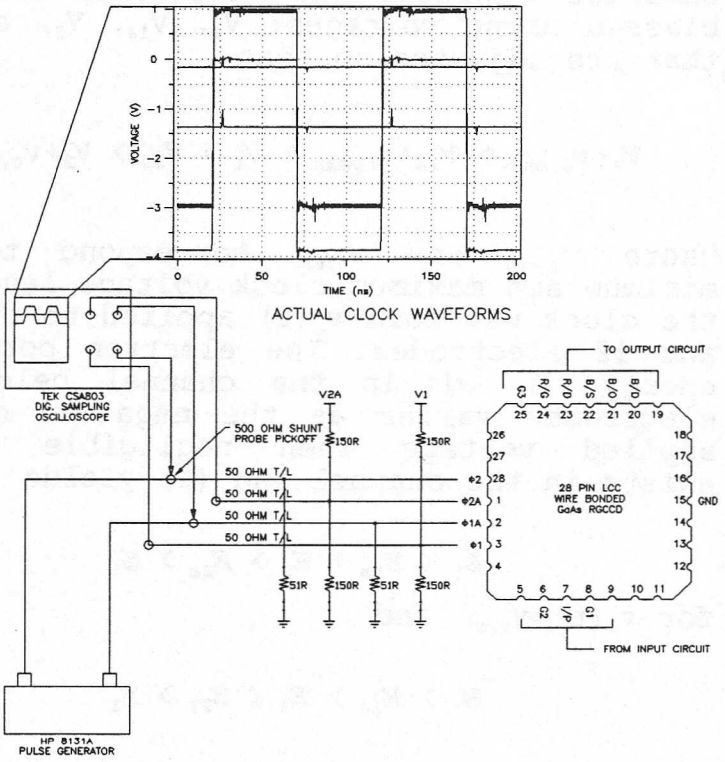

Fig. 2 RGCCD test circuit.

The signal charge contained in the RGCCD channel below the **ϕ**1, **ϕ**1a, **ϕ**2, and **ϕ**2a electrodes is also shown in Fig. 3. The signal charge was calculated by integrating, with respect to time, the current in each of the terminating resistances attached to the transport electrode terminals that would result from the potential difference between the observed full and empty well voltage responses. The signal charge contained under the **ϕ**2 electrodes is about 3 pC prior to the negative clock transition, corresponding to a full well charge magnitude per pixel of approximately 23 fC ($\approx 1.5 \cdot 10^5$ electrons). During the negative transition of the clock the signal

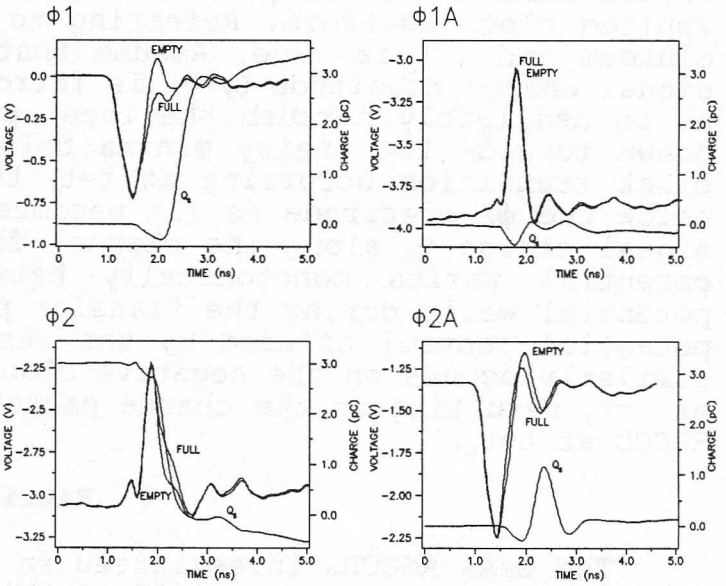

Fig. 3 Voltage responses and calculated charge on the negative clock transition.

charge diminishes below the $\phi 2$ electrodes and is seen to increase below the $\phi 1$ electrodes, as expected. While the signal charge is in transit, it passes directly through the region under the $\phi 2A$ electrodes, causing the subnanosecond charge pulse to occur. The signal charge does not present itself to the region below the $\phi 1A$ electrodes during the negative clock transition as indicated. The maximum frequency of operation for the 128-pixel RGCCD under test is just beyond 1 GHz as determined by the duration of the charge pulse below the $\phi 2A$ electrodes.

A lumped element equivalent circuit for modelling the empty well circuit parasitics associated with the GaAs RGCCD transport region is shown in Fig. 4. The proposed model was derived from a SPICE simulation of the test circuit contained in Fig. 2. The simulation included the uniphase drive, the d.c. bias networks, and the proposed equivalent circuit in Fig. 4. The SPICE simulation focussed on the transient response occurring on the negative clock transition. It was determined that the package and metallization inductance, L, was about 5 nH, the interdigital cermet resistance, R, was nearly 1 kΩ and the interdigital capacitance $C+C_S$ was approximately 2.5 pF. The calculated and the observed transient responses are shown in Fig. 5.

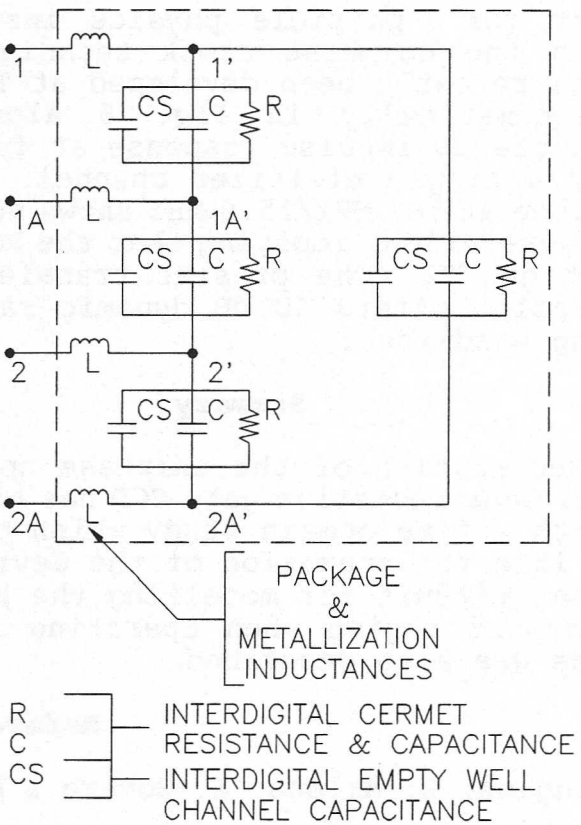

Fig. 4 Equivalent circuit of the transport region for the empty well mode of operation.

In principle, it is possible to use the equivalent circuit in Fig. 4 to estimate the applied tangential electric field term between adjacent transport electrodes on the RGCCD surface, providing guidance for determining if appropriate values are being achieved during device operation. For device operation using a predetermined uniphase drive circuit the potential difference between adjacent "primed" nodes can be computed. Dividing the computed values by the transport electrode separation provides an estimate of the surface electric field which is assumed uniform, by the very nature of the resistive gates. Our experience has shown us that the surface electric field term should be > 2-3 kV/cm for the uniphase operation of the device. For our 128 pixel RGCCD, a clock driver delivering 4 V_{p-p} with ±100 mA current drive is required. This condition is satisfied using conventional GaAs MESFET circuits.

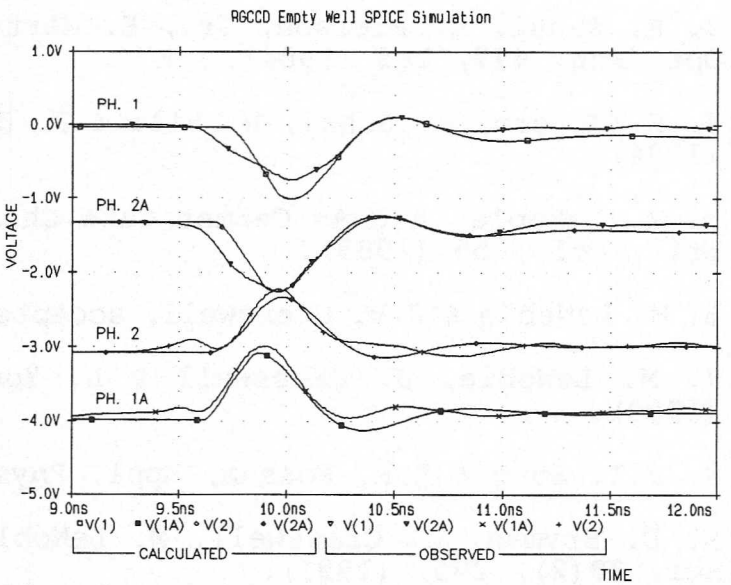

Fig. 5 Calculated and observed transient responses at the RGCCD transport electrodes.

Operation

The GaAs RGCCDs fabricated at TRIUMF were evaluated for uniphase operation at frequencies up to 500 MHz. Charge transfer efficiencies (CTEs) in excess of 0.999 have been obtained, and are the highest reported for the uniphase operation of a GaAs CCD[6]. A prototype implementation of a 500 MHz/15.6 MHz GaAs RGCCD multi-channel transient digitizer for particle physics instrumentation[9] employing the uniphase clock technique described above has recently been developed at TRIUMF and is shown schematically in Fig. 6 along with the observed pseudo-impulse response at full operating speed of a single digitizer channel. The observed performance at 500 MHz/15.6 MHz shows no significant signal degradation, implying that the RGCCD operates with a high CTE. The present transient digitizer configuration offers 40 dB dynamic range over its operating bandwidth.

Summary

A description of the uniphase operation of a 128 pixel GaAs resistive gate CCD has been presented along with a time domain study which provides some insight into the operation of the device. A simple equivalent circuit for modelling the parasitics of the transport region when operating in the empty well mode was also described.

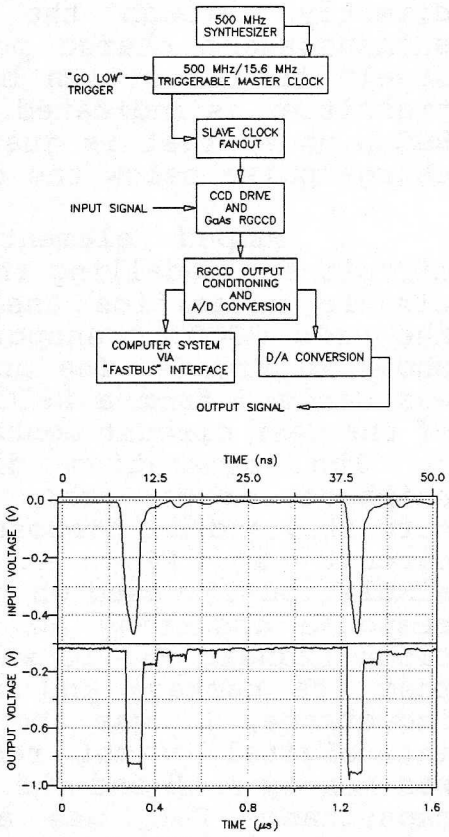

Fig. 6 500 MHz RGCCD transient digitizer.

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