Analysis and Results of a Random Access Charge Injection Device

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Abstract

High Speed tracking applications require high video frame rates that can overload the camera and computer system with unnecessary video information and attendant signal processing. The use of a random access imager to read only the desired group of pixels eliminates unnecessary video processing and increases frame rate in a ratio of the total number of pixels in the array to the number of pixels read per frame.

Reported herein is the design, analysis and results of a 10 MHz Charge Injection Device (CID) with 520 Correlated Double Sampled (CDS) amplifiers that operate in parallel at line rate. Direct addressing of the 520 rows and 520 columns is accomplished with two latched ten bit decoders.

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2. Introduction-Application Needs
3. Design Approach
4. Subsystem Implementation
5. RACID Layout
6. RACID Results
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Design Approach

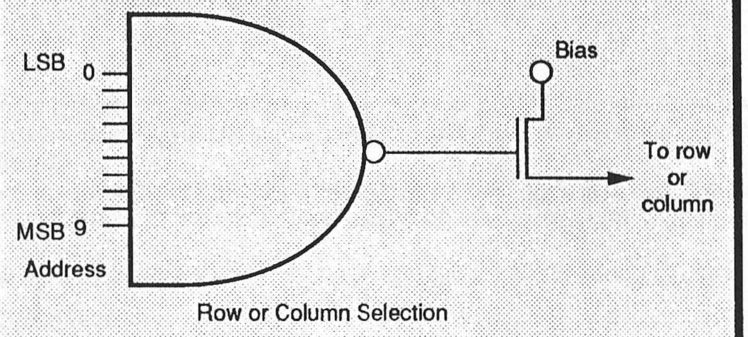
Architecture Issues

While the pixel structure lends itself to satisfy the requirements of 500 frames per second, variable integration, variable frame size, the conventional CID imager architecture did not.

- The system element rate clock operating at 10 MHz for a 512 x 512 pixel array generates at maximum 38 Hz frames per second.
- A sub array of 16 x 16 pixels at the same 10 MHz element rate will generate at maximum 39,062 frame per second.
- In practice, necessary timing overhead due to integration, blanking and addressing lowers the frame rate significantly.
- Conventional CID architecture sequentially scanned each pixel in a row and each row in sequence for the entire array.

Direct horizontal and vertical (x and Y) addressing and control of each pixel at 10MHz was necessary.

A ten bit CMOS Nand decoder was selected for all addressing needs.



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Design Approach

The CID 's unique pixel structure can satisfy the 500 frames per second, variable integration time, variable frame sizes, anti-blooming and sub-pixel interpolation requirements

CID Features	CID Benefits	CID Weakness
• X-Y Addressable	Allows for sub-array or individual pixel addressing	Interconnected pixel structure has high associated capacitance and therefore noise
• Non Destructive Read-Out (NDRO)	Variable integration or noise reduction	
• Extreme Anti-Blooming due to buried collector	Allows for high image overloads without distortion of nearby objects	
• Simple pixel structure-high fill factor	Allows high degree of subpixel interpolation	

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Introduction-Application Needs

D2 Seeker Missle Goal

D2 is a strategic defense, ground launched, hit to kill projectile with an end-game in the lower atmosphere. The terminal homing seeker is used during end-game for final Guidance and Control homing maneuvers on strategic re-entry vehicles to obtain hit-to-kill accuracy.[4]

D2 Seeker Focal Plane Array Requirements

- High Speed Tracking- 500 Frames Per Second (Mach 14 to 20)
- Withstand 100,000 Gs Launch
- 512 x 512 Pixel Arrangement
- 1/14 Subpixel Interpolation
- Variable Integration Time
- 60 dB Dynamic Range
- Extreme Anti-Blooming
- Variable Frame Size
- Pixel Element Rate of 10MHz.
- Freeze Frame (eliminate image blur)
- 20 micron square pixels

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Architecture Issues

The pixel structure and CMOS decoders will take care of all but the freeze frame and 60 dB signal to noise.

- A 20 X20 Micron pixel structure can be designed to collect 1,000,000 carriers. The low light level read noise needs to be less than 1000 carriers. A goal of 400 electrons dark back ground noise was set.
- Conventional CID architecture used current sensing along the row for reading pixel information. This sensing technique would have 1000 to 1500 electrons noise per read.

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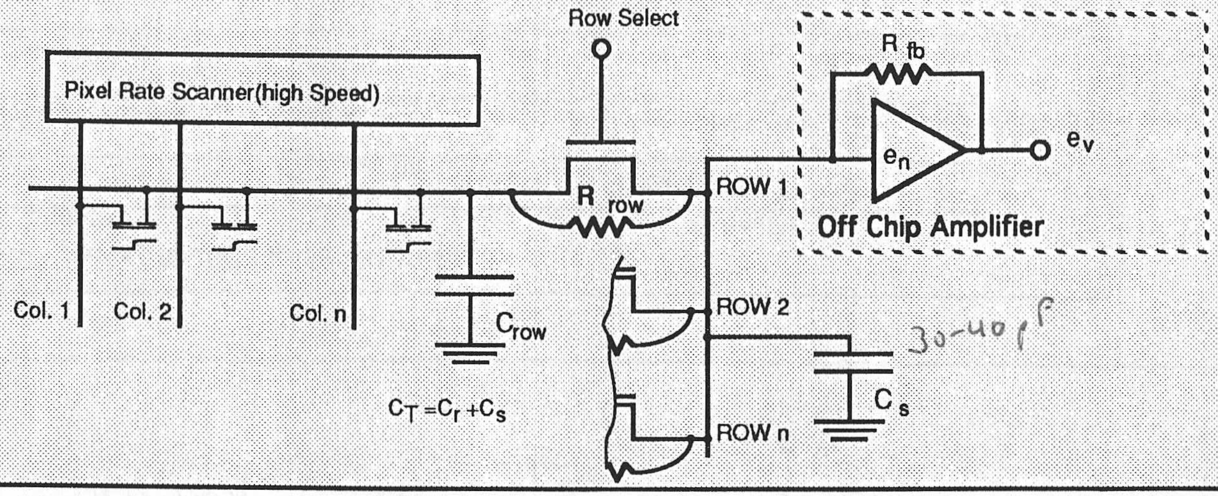
Design Approach

Architecture Issues- Sense Noise

Conventional Row Sense With Off Chip Preamplifier



Dark Background Noise Sources

Source	Type	Behavior
R_{row}	KTC*, Johnson	$\alpha\, C_{row}, R_{row}^{1/2}, (\text{pixel rate})^{3/2}$
R_{fb}	Johnson	$\alpha\, R_{fb}^{-1/2}, (\text{pixel rate})^{1/2}$
e_n	Johnson, 1/f	$\alpha\, C_t, e_n, (\text{pixel rate})^{3/2}$

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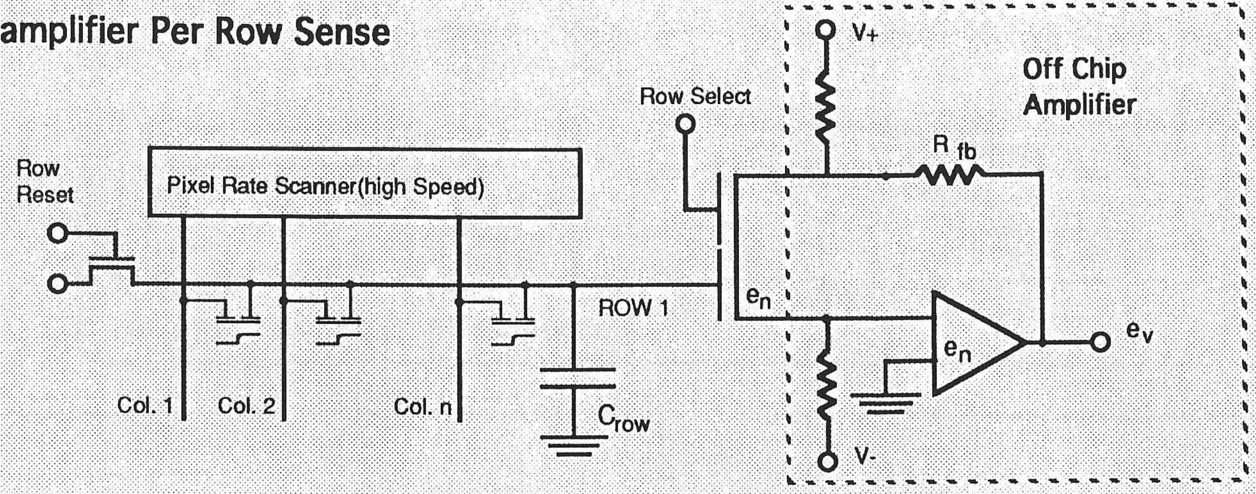
Architecture Issues- Sense Noise

Preamplifier Per Row Sense



Dark Background Noise Sources

Source	Type	Behavior
R	KTC*, Johnson	αC_{row}
e_n	Johnson, 1/f	αe_n, (pixel rate)$^{1/2}$

Note: eliminated via off-chip CDS

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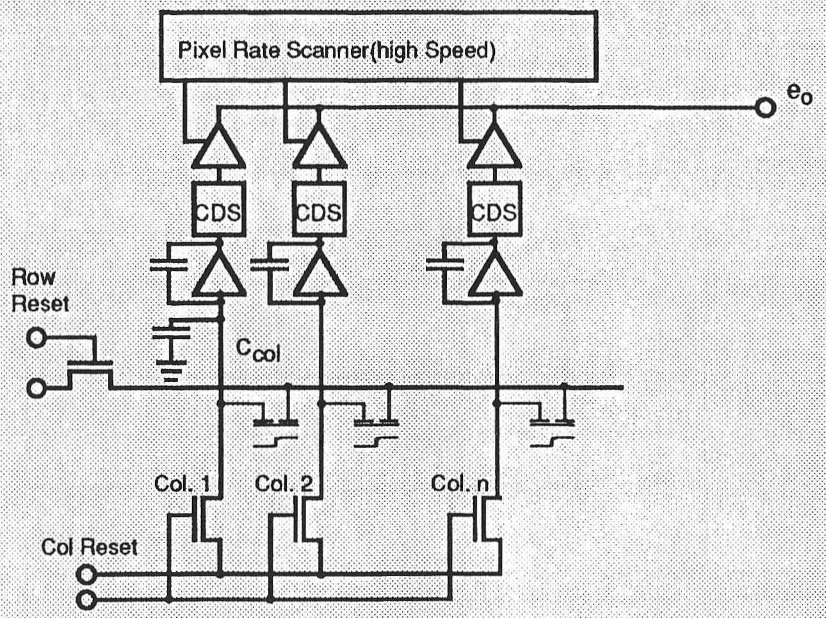
Architecture Issues- Sense Noise

Preamplifier Per Column Sense



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Architecture Issues- Sense Noise

Dark Background Noise Sources

Conventional Row Sense[1]

Source	Type	Behavior
R_{row}	KTC*, Johnson	$\alpha\, C_{row}, R_{row}^{1/2}, (\text{pixel rate})^{3/2}$
R_{fb}	Johnson	$\alpha\, R_{fb}^{-1/2}, (\text{pixel rate})^{1/2}$
e_n	Johnson, 1/f	$\alpha\, Ct, e_n, (\text{pixel rate})^{3/2}$

Preamp Per Row Sense

Source	Type	Behavior
R	KTC*, Johnson	$\alpha\, C_{row}$
e_n	Johnson, 1/f	$\alpha\, e_n, (\text{pixel rate})^{1/2}$

Preamp Per Column Sense[2,3]

Source	Type	Behavior
R	KTC**, Johnson	$\alpha\, C_{col}$
e_n	Johnson, 1/f	$\alpha\, e_n, (\text{Line rate})^{3/2}$

Notes: *eliminated via off-chip CDS
**eliminated via on-chip CDS
reference [1,2,3] for previous papers regarding noise analysis.

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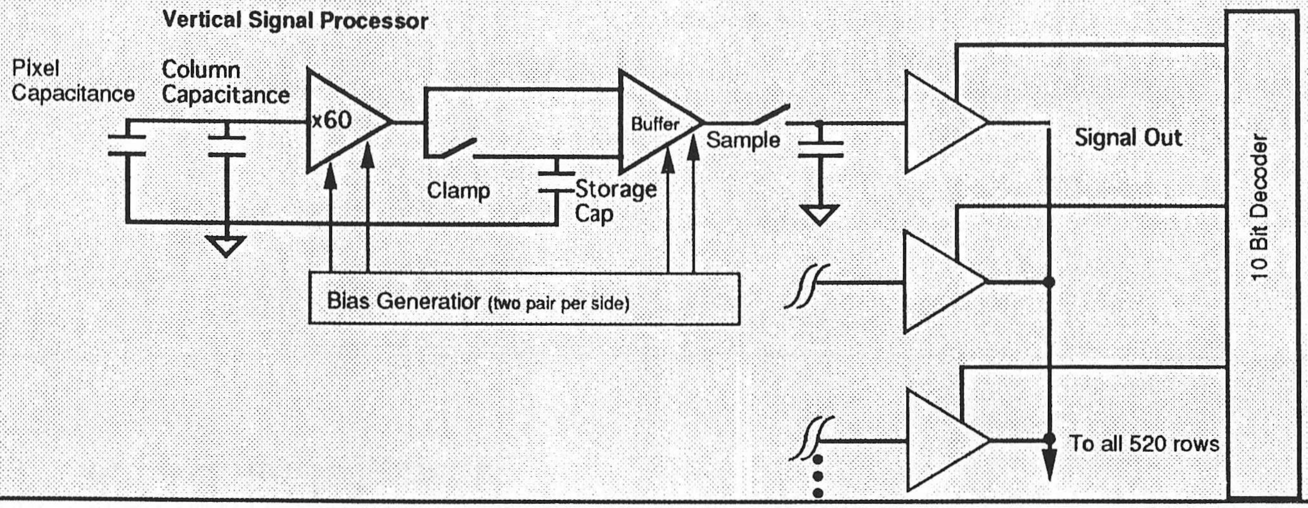
Subsystem Implementation



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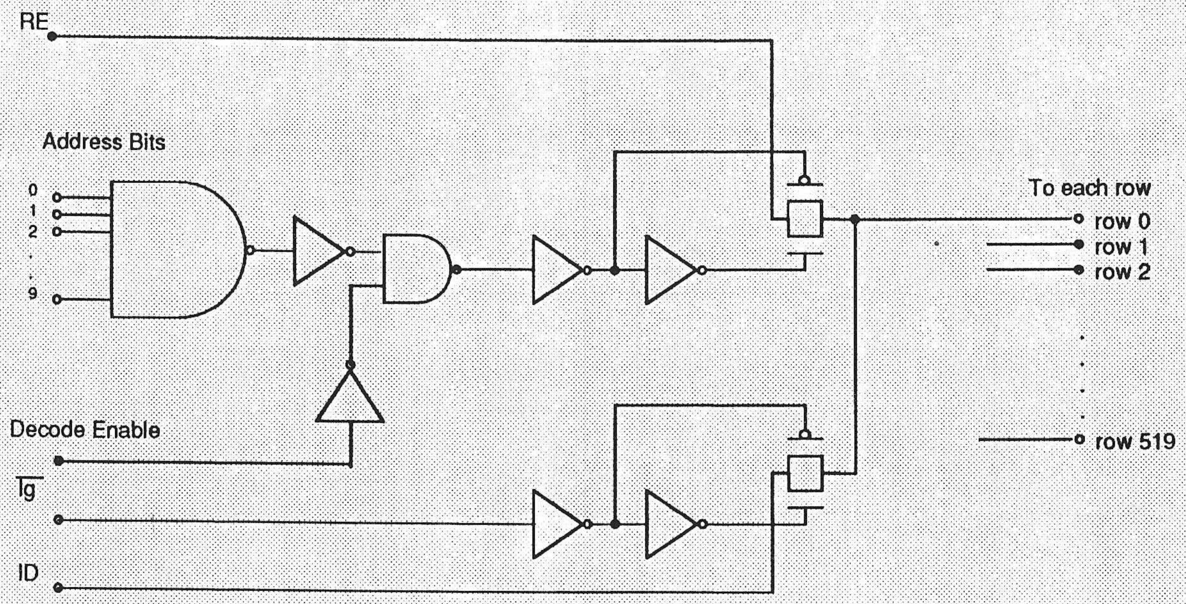
Subsystem Implementation

RACID 35 ROW DECODER and MULTIPLEXOR - FUNCTIONAL SCHEMATIC



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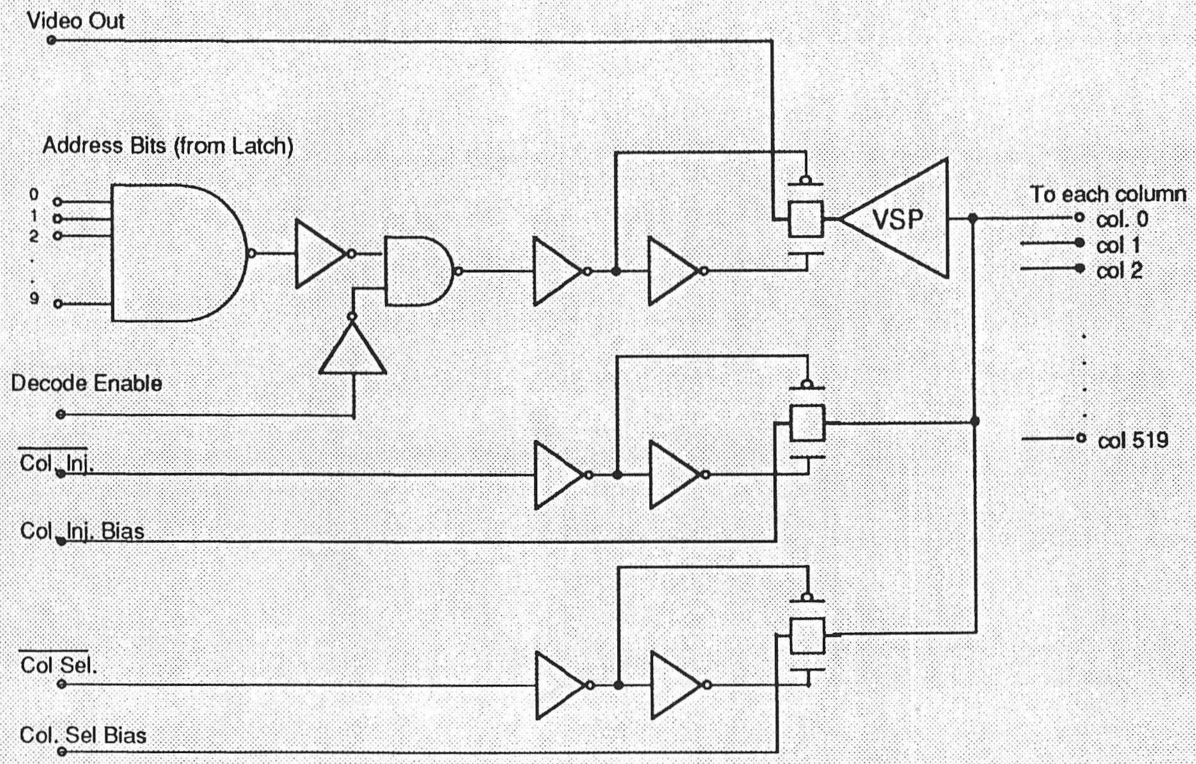
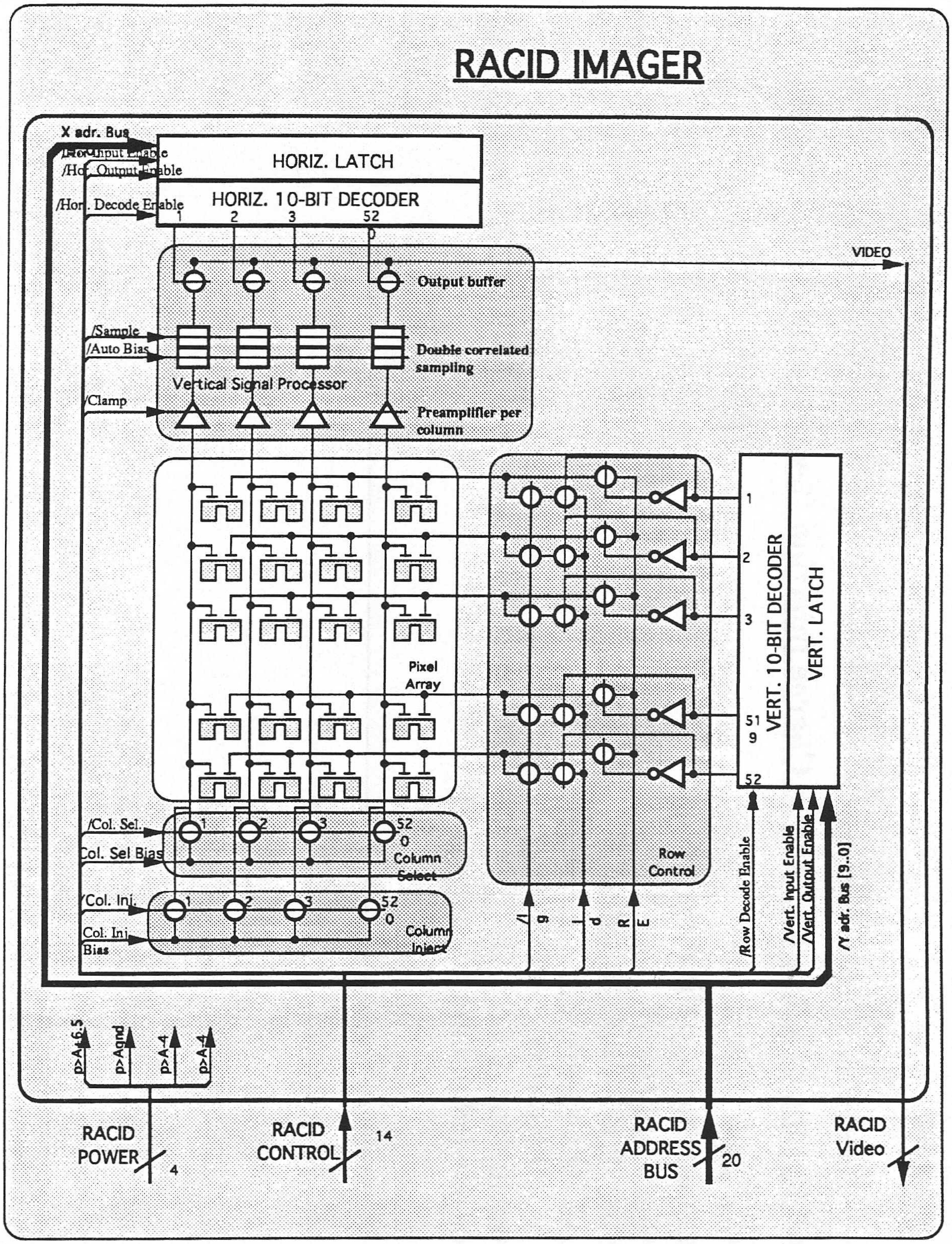
Subsystem Implementation

RACID 35 COLUMN DECODER and MULTIPLEXOR - FUNCTIONAL SCHEMATIC




RACID IMAGER
X adr. Bus
/Hor. Input Enable
/Hor. Output Enable
/Hor. Decode Enable
HORIZ. LATCH
HORIZ. 10-BIT DECODER
1
2
3
520
VIDEO
Output buffer
/Sample
/Auto Bias
Double correlated sampling
Vertical Signal Processor
/Clamp
Preamplifier per column
Pixel Array
1
2
3
519
520
VERT. 10-BIT DECODER
VERT. LATCH
/Col. Sel.
Col. Sel Bias
1
2
3
520
Column Select
/Col. Inj.
Col. Inj. Bias
1
2
3
520
Column Inject
Row Control
/I
g
I
d
R
E
/Row Decode Enable
/Vert. Input Enable
/Vert. Output Enable
/Y adr. Bus [9..0]
p>A+6.5
p>Agnd
p>A-4
p>A-4
RACID POWER
4
RACID CONTROL
14
RACID ADDRESS BUS
20
RACID Video

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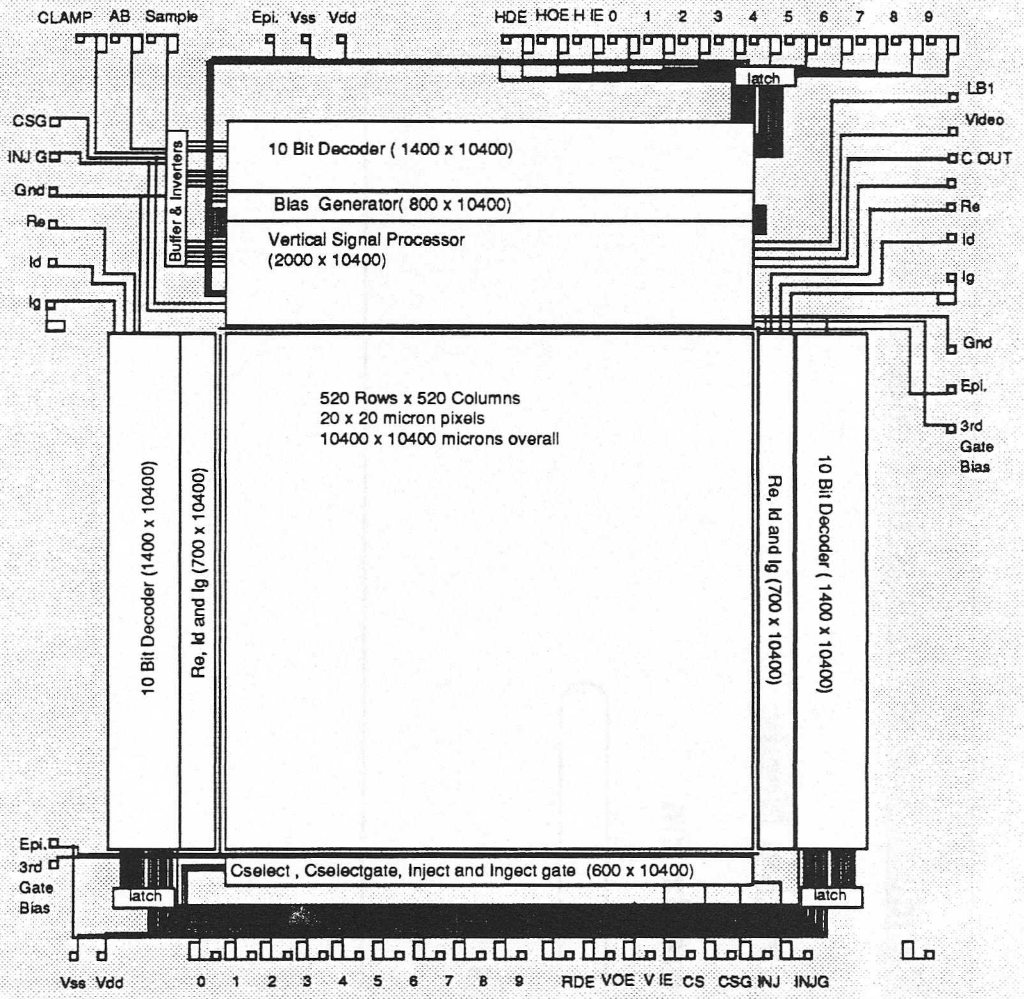
RACID 35 Layout



Die size = 15037.5 x 17460.0 microns

Notes: (Units in microns)

Preliminary Info. only

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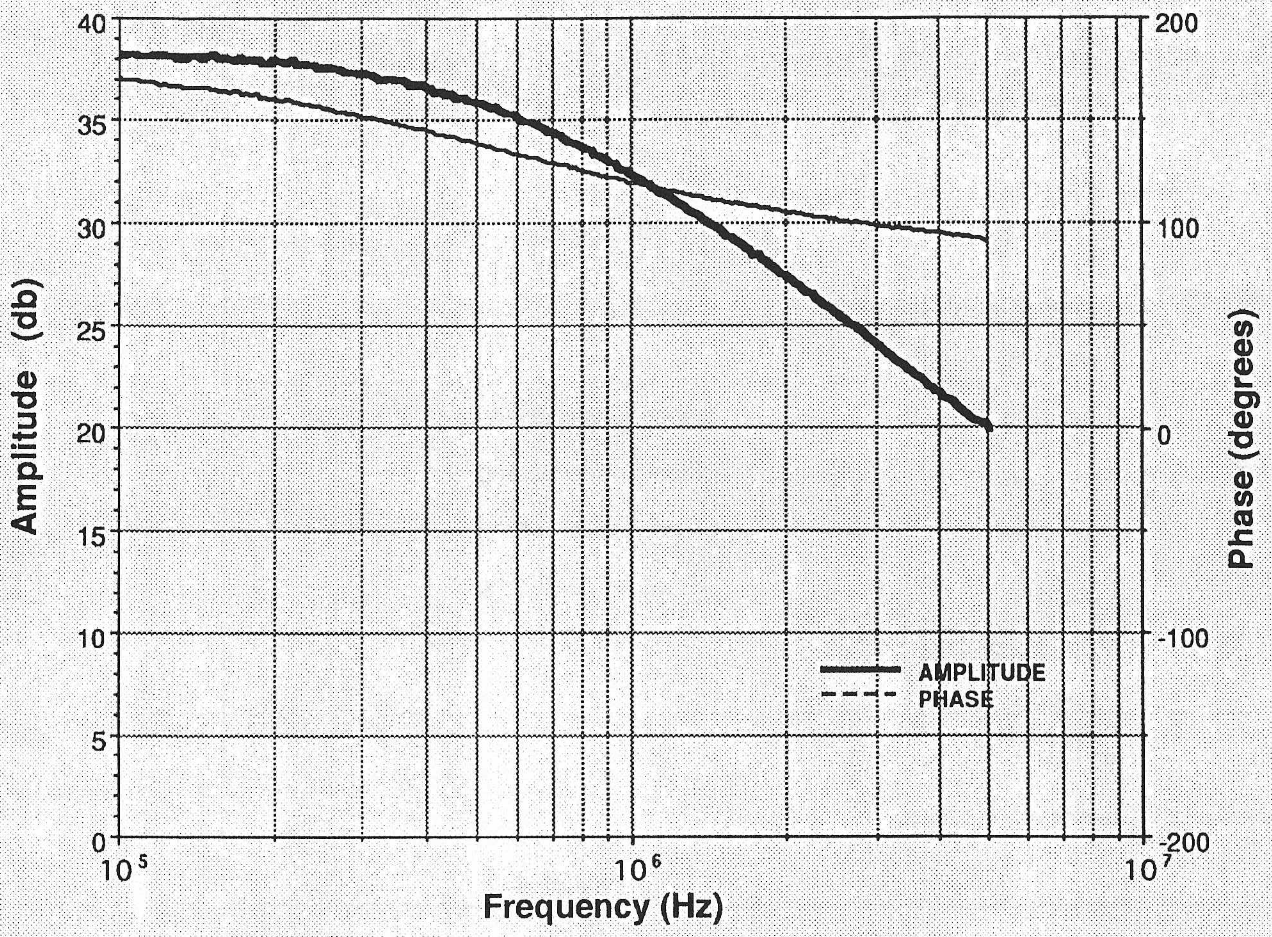
Preamplifier Response (with load)



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RACID Results

Sub-Cell	Results	Comments
Decoders (Horz & Vertical)	Tested to 25 MHz	
Muxers	Functions	
VSP-PreAmp	Measured $A_{cl} = 60$	Needs further testing
VSP-Sample and Hold	Functions	Needs further testing
VSP-Buffer	Functions	Needs further testing
Bias Generater	Functions	Needs further testing
Latches	Tested to 25 MHz	
Inverters/Buffers	Tested to 25 MHz	
Power Consumption	90 mW	

Note: unless otherwise noted RACID testing was at 1.0 MHz.

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Conclusions

The RACID imager achieved a new level of on-chip integration at the same time a new process was developed.

- All subcircuits functioned on first silicon. Some routing errors inhibited a fully functional device.
- Routing errors were corrected and fully functioning devicess were successfully tested.
- Project funding on hold.
- Carrier for RACID imager under development.
- Full device characterization will resume.

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Acknowledgments

Funding has been provided by Martin Marietta Co. Astro-Space, King of Prussia, PA 19101.
Special thanks going to D. Peters of Martin Marietta Co. who assisted in the conceptualization of the RACID imager.

The authors appreciate the hard work and efforts put forth by other RACID team menbers that include, J. Hutton, E. Eid, and F.Arnold .

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