2048*2048 CCD, 3 SIDE BUTTABLE DESIGNED FOR LARGE FOCAL PLANES

J.A. CORTIULA, V. NGUYEN THOMSON Semiconducteurs Spécifiques, France

I - INTRODUCTION.

Five years ago, THOMSON developed a sensor that was considered to be a large detector, with 1024^2 pixels of a 19µm by 19µm size. Today, the technology improvement in silicon, particularly the lithography resolution, allow to manufacture larger sensors of the same type. 1.5µm design rules now give the 2048^2 sensor structure an advantage. Considering its applications towards the astronomic field, this device, running in Multi Pinned Phase (MPP), is designed to obtain three buttable sides in order to form a sensor matrix with, for example four 2048^2 devices.

The sensitive area is then 36 cm^2 with a minimum dead zone.

Technical considerations, and device architecture are presented.

II - DESIGN AND TECHNOLOGY

II.1 - DESIGN

The frame transfer organization based on four phases clocking sheme with two polysilicon gate process, allows the best performance in terms of integrated electrical charges. In order to improve this electron handling capacity, a specific software was developed to automaticaly modelise the electronic structure of such a sensor, easily implemented for computer-aided analysis of circuits. Consequently, a particular attention was paid for the polysilicon gate dimensions that form the pixels of 15µm by 15µm size and also for minimum dimension of the internal drive connections in aluminium in order to get the minimum blind area between two buttable 2048^2 devices. Other problems for this large sensor, were stemmed from the results of these simulations : the parasitic capacitors between two adjacent polysilicon gates. Through these simulations and in result for the user, it is possible to define precisely the different transfer clocks (in time and in magnitude) applied to this device in order to obtain the best features of this large sensor in term of integrated but also tranferred charges.

In pratice, these simulated electronic behaviors allow to define perfectly the type of architecture of this device according to the user specification.

The MPP mode specially required for a very low dark current generation, is obtained during the process by implementing Boron between two polysilicon gates of the same level, keeping therefore an auto-alignment for this buried channel. The generated holes near the oxyde-silicon interface, during the photonic creation of an electron-hole pair, are drained in a P+ channel allowing also to insulate two adjacent pixels and to clamp in this way the oxyde-silicon interface near to a nul potential (in this case given by the substrate connected to the ground). This MPP mode decreases naturally the maximum charge capacity of a pixel during the integration period compared with the non MPP mode. This is due to the fact that the internal electrostatic potential is lower than the non MPP mode one.

The spectral responsivity in the case of front side illumination, depends strongly on the thickness of the poly-silicon gates. Therefore, the responsivity near the "blue" wavelength is degraded since the absorption of this one occurs in the first thickness micron. The choise of the 1.5µm design rules allow to improve a bit this responsivity, by minimizing the overlap of polysilicon gates of two different levels.

The readout register is designed in order to obtain a full MPP device. It is made of three polysilicon gates and is optimised to get a minimun of parasitic capacitors with the last polysilicon gate that ends the image zone. Therefore, the timing is well defined to avoid different problems due to these capacitors. This point concerns particularly the rise and fall time of the readout register timing scheme. Moreover the readout register offers the possibility of summing four pixels in order to obtain a 1024^2 array with a pixel size which is then 30µm x 30µm size.

The output amplifier is designed to obtain a very low noise that can be improved by a double correlated sampling stage. Two MOS transistors are integrated in order to get an internal current source that is externally driven. This current source can be connected or not in order to load the first MOS transistor by an external resistor.

butting ⇒ 400µm dead zone

15 x 2K = 30mm

150,000 full well
15x15µm²
4e⁻ noise
0.2e⁻/s/pix dark 20°C.
CTI 5x10⁻⁶
non unif ±5% !
50kps
full frame

20pA/cm²

II.2 - TECHNOLOGY.

The substrate resistivity of this device is in the range of 4-6 Ohm.cm, and <100> oriented P-type. The epitaxial layer of 15µm thickness optimises the density of integrable charges in the buried channel, which is necessary in the required MPP mode.

The pixel insulation is obtained in the vertical direction (tranfer direction in the image zone) by electrical fields and a compensated channel. For the horizontal direction this insulation is obtained by an oxyde field on the P+ implant.

Globally three polysilicon levels are used to manufacture this device. The first level is principally used to minimise the noise of the output amplifier.
Through several technological considerations, it was studied that at the beginning of manufacturing process, the interface silicon -oxyde quality under the gate driving the MOS transistor, has a strong effect on the output noise. In this way, for scientific applications of such a sensor, where the signal to noise ratio is a first order parameter, it is mandatory to include one specific polysilicon level.

III - DEVICE ORGANIZATION AND FEATURES.

III.1 - IMAGE ZONE.

As explained before, the two polysilicon gate levels driving the frame transfer, are organized in four phases. Since this device runs in the MPP mode, during the integration period all voltages applied to these are negative

10 dark reference pixels are added at the beginning of the image zone for specific calibration needs. These non sensitive pixels also allow to separate optically this image zone from the readout registers. In this way, the total image zone including the dark reference is now defined by 2058 lines and 2048 columns in order to keep the three sides buttable configuration.
The sensitive zone is perfectly masked all around its periphery and at its edges the optical mask is optimised in order to achieve the best uniformity of response.

Through the simulation results and taking into account the intrinsic technology parameters, it was defined that the optimum horizontal frequency is 20kHz in full specification in term of charge handling capacity. Typically, 150ke- are available in integration as in transfer.

A specific clocking applied to this image zone was carefully calculated in rise, fall and setting time, in duration, in negative and positive voltage, and also in sequence to minimise the capacitive crosstalks between two neighboring polysilicon levels. As it was seen during the simulation, the timing defined in the terms above, is critical when it is necessary to obtain the best performances of this sensor. Consequently, specific drivers were developed with using analogic circuits. The command of phases is made of two steps, the first one being a controlled current source driver and in the second step a voltage follower driver. These both drive modes can only be obtained with analogic components.

The front side illumination allows nevertheless an acceptable spectral responsivity spreading from 400nm up to 1000nm. The maximum quantum efficiency is 35% at 700nm.

III.2 - READOUT REGISTER.

Four identical readout registers end the image zone. Three polysilicon levels were therefore used in order to transfer in a four phase mode the charges stemmed from the last stage of the image zone that gives the possibility to sum, if desired, two lines. The charge handling capacity of the registers is twice the full well capacity of the pixel.
Morever in order to get the possibility to sum two pixels, a summation stage was defined at the extremity of each readout register. In this way, the design allows to get the summation of four pixels. Thus, this device can become a 1024^2 array device with an equivalent square pixel of 30µm x30µm.

In order to minimise the capacitive crosstalk usually seen on the signal in a four phase mode, 10 pixels were designed in order to be driven in two phase transfer using the same command than the four register phases.
When the commands are well setted, this organization allows to clamp and to sample the output signal on a stable state of these phases.

Two gates of different type end each readout register in order to adjust the conversion factor depending on the amount of charges. In this way, it is possible to read up to 800Ke-. This conversion factor control is then obtained by applying a continuous voltage over one of these two gates.
Two conversion factors are then available.

III.3 - AMPLIFIER.

The output amplifier is made of two MOS transitors. The "head" MOS transistor is used to read the charges stemmed from the readout register, and the "foot" MOS transistor is used or not (depending on the application) as a current source externally controlable. An advantage is then given since it is possible to control the bias current of this amplifier stage and to fix the bandwidth, and all bias conditions by adjusting the voltage level applied to the head MOS transistor.

III.4 - PACKAGE.

In order to get the buttable configuration on three sides, it was necessary to develop a specific package. Principally, manufactured in two parts, it receives the 2048^2 sensor with a flatness better than 10µm.
Three sides of this die project beyond the package in order to offer the buttable configuration. The base plate of this package is in metal to insure a stable substrate potential and to clamp thermically all the device.

The connection of the different electronic elements integrated on the die, are made directly in the 33 pin package.
In this way, the signal propagation time are greatly decreased, allowing thus to drive symetrically the critical phases.

This device is also available in a standard package (one device).

IV - CONCLUSION.

The design of all the device including the package, is totally oriented to meet the highest performance specifically required for low light level imaging. Two patents are currently being deposited to improve considerably the output signal, by increasing simultaneously the signal to noise ratio, the linearity, the charge handling capacity and propose finally a great advantage for the user by suppressing linearly the classical coupling due to the reset signal on the output signal one.

For the moment, the first runs are processed and the validation of this device is began showing very encouraging results.