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A SMART PIXEL ARRAY FOR HIGH LUMINOSITY PARTICLE DETECTION EXPERIMENTS AT THE SUPERCONDUCTING SUPERCOLLIDER

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Presented by Jacques Millaud

LBL: New Array Architecture Concept

- **Eliminate X – Y organization;**
  ⇒ **Column-based Structure:** One-dimensional organization simplifies array design and operation.
  ⇒ **Bonus:** No transverse lines crossing within the array; no transverse peripheral circuitry.
  ⇒ **Penalty:** Pixel address function along a column must be added; this increases pixel cell area.

- **Decentralize control of hit recording;**
  ⇒ **Local Action:** Hit recording controlled by local column logic.
  ⇒ **Reduced Rate:** Circuitry peak activity rate is reduced from 5 MHz to $\sim$ 88 kHz.
  ⇒ **Efficient Buffering:** Column buffers can be shallow, rather than storing an array-wide data field.
  ⇒ **Higher Luminosity:** Graceful behavior well beyond $10^{33} cm^{-2} s^{-1}$.

- **Real-time digital coincidence for Level I:**
  ⇒ **Simplification:** Straightforward digital design.
  ⇒ **Deadtimeless Behavior:** Read and Write.
  ⇒ **Easily variable Trigger I delay:** ΔT $\nearrow$.

PIN DIODE
DETECTOR WAFER

AMPLIFIER/READOUT CHIP

MASS CONNECTIVITY
(ie SOLDER BUMPS)

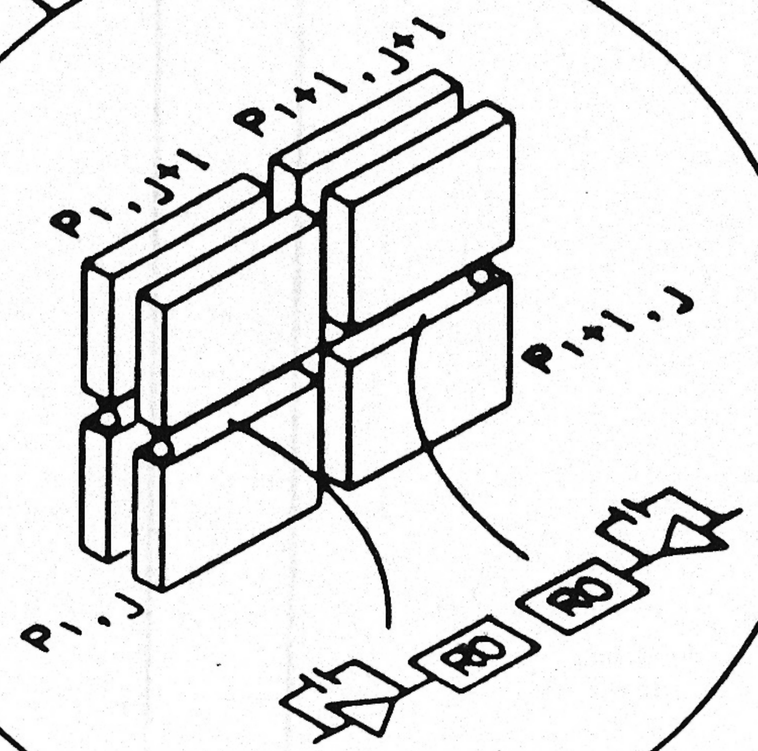
ASSEMBLIES

COLUMN RO

COLUMN RO

COLUMN RO

COLUMN RO



COLLECTING CHIP

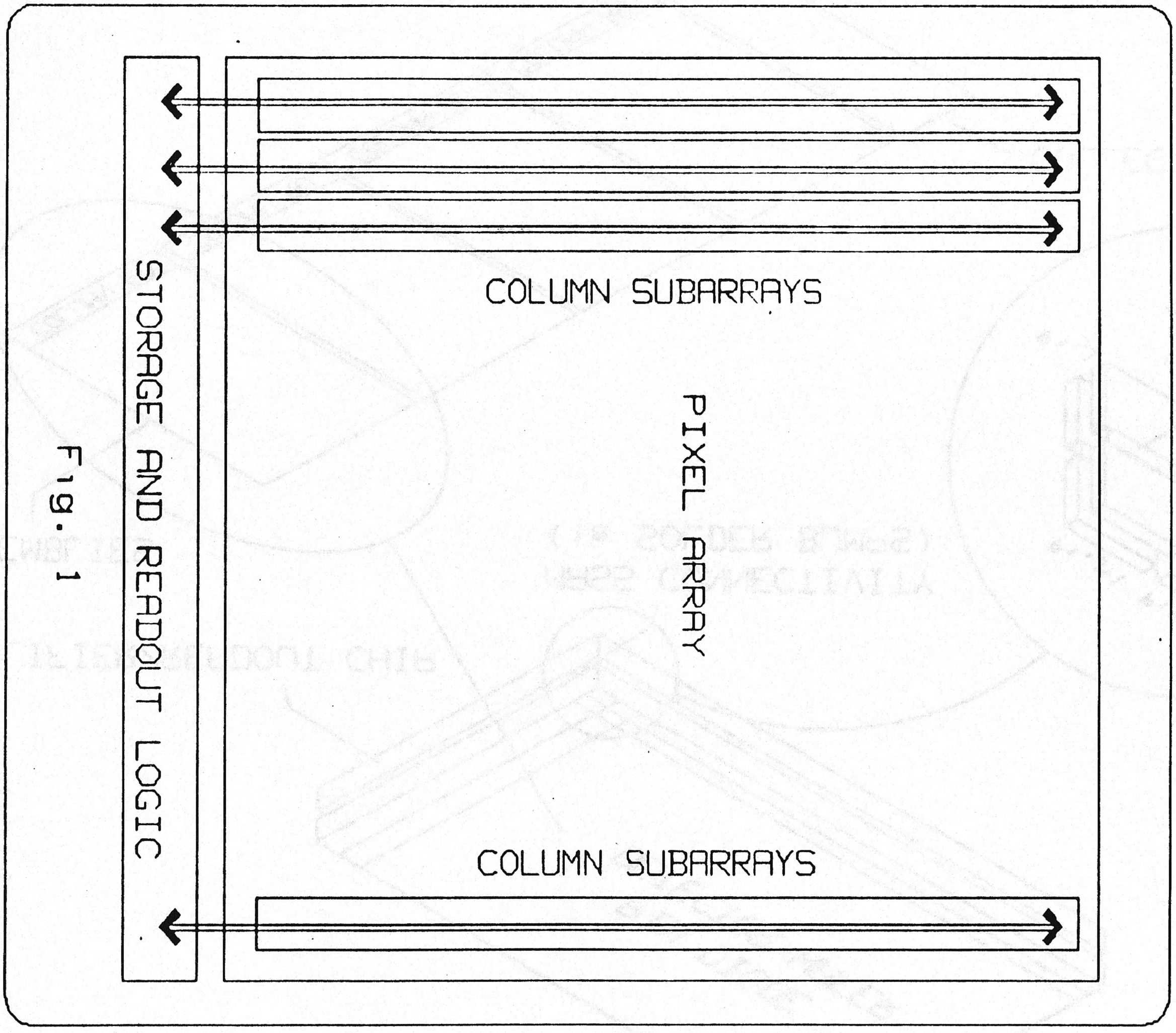

COLUMN SUBARRAYS
PIXEL ARRAY
STORAGE AND READOUT LOGIC
COLUMN SUBARRAYS

Fig. 1

"Smart Pixel" Detectors for the SSC

- **Smart Pixel Concept developed at LBL**
  - Only struck pixels are read out;
  - Built-in level I trigger delay.

- **Column-based array architecture defined**
  - New concept reduces rates, simplifies design;
  - Permits operation well above design luminosity.

- **Pixel cell circuit design "solved"**
  - Nearly all specifications met;
  - "Final" design cycle underway.

- **Small pixel capacitance** ($\simeq$ 350 fF)
  - Permits very high S/N ratios $\simeq$ 200;
  - Fast time response for modest power.

- **Small pixel leakage current**
  - Negligible shot noise contribution;
  - Detectors can be DC-coupled.

- **Bump-bonded hybrid technology**
  - Separate optimization of technologies;
  - Commercial solutions for integration.

- **Array Size:** 64 x 256 ($2cm^2$)