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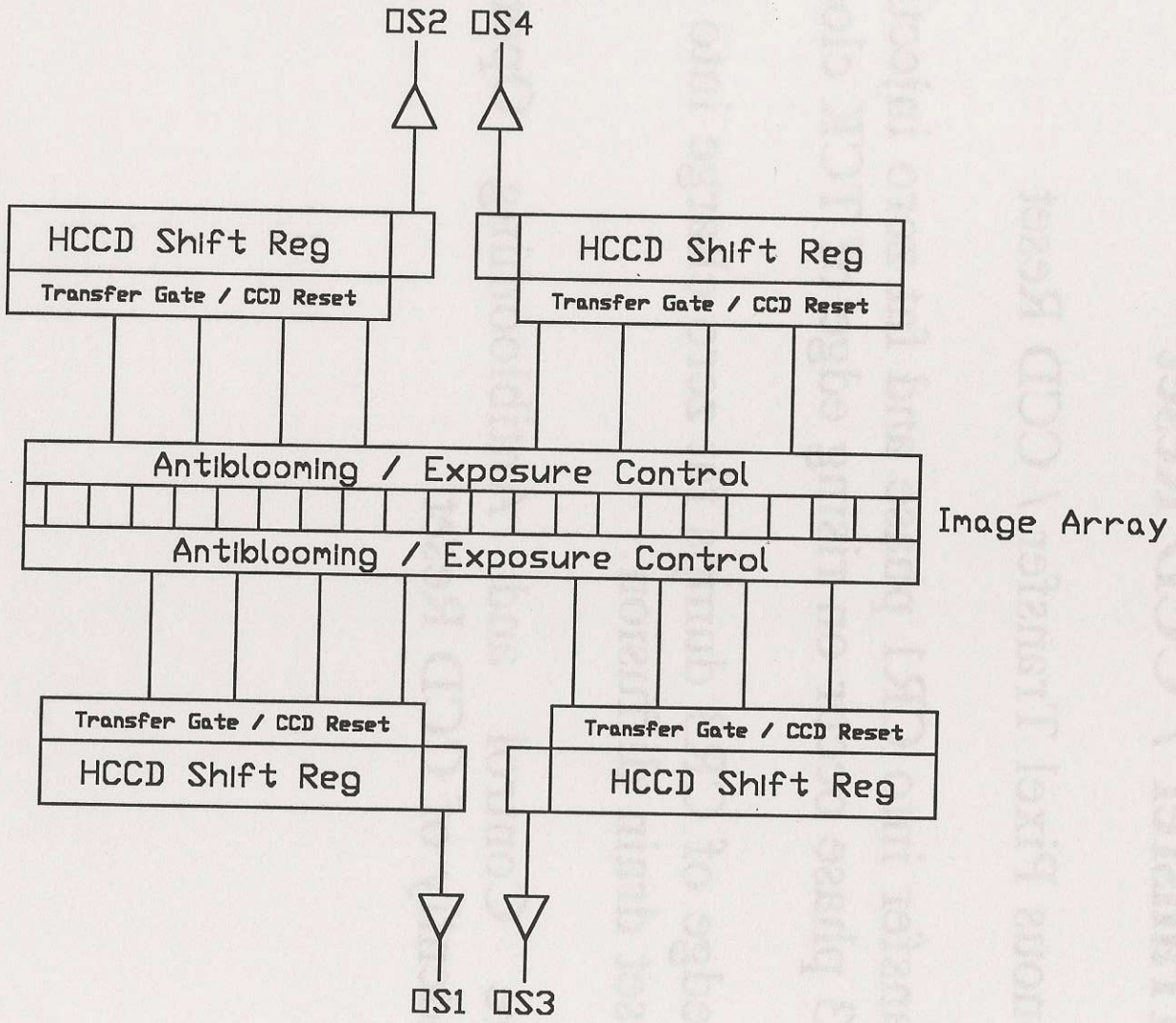

Figure 1 - Image Sensor Architecture

Pixel Transfer / CCD Reset

Synchronous Pixel Transfer / CCD Reset

Pixel transfer into CR1 phase and fat zero injection into CR3 phase occur on rising edge of TCK clock.

Falling edge of CR3 dumps fat zero charge into the CCD reset drain diffusion.

Exposure Control and Antiblooming Operate Independently of CCD Reset

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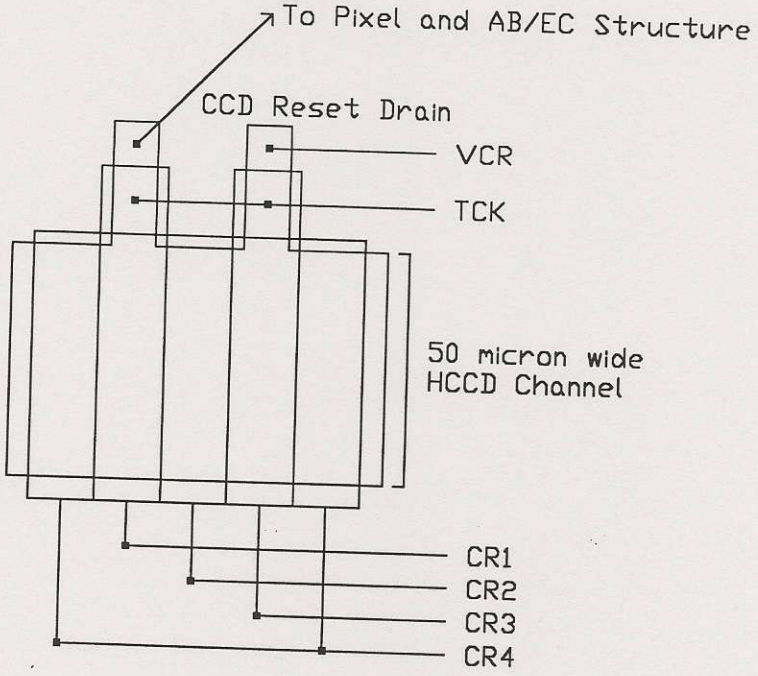

Figure 2 - Unit HCCD Cell

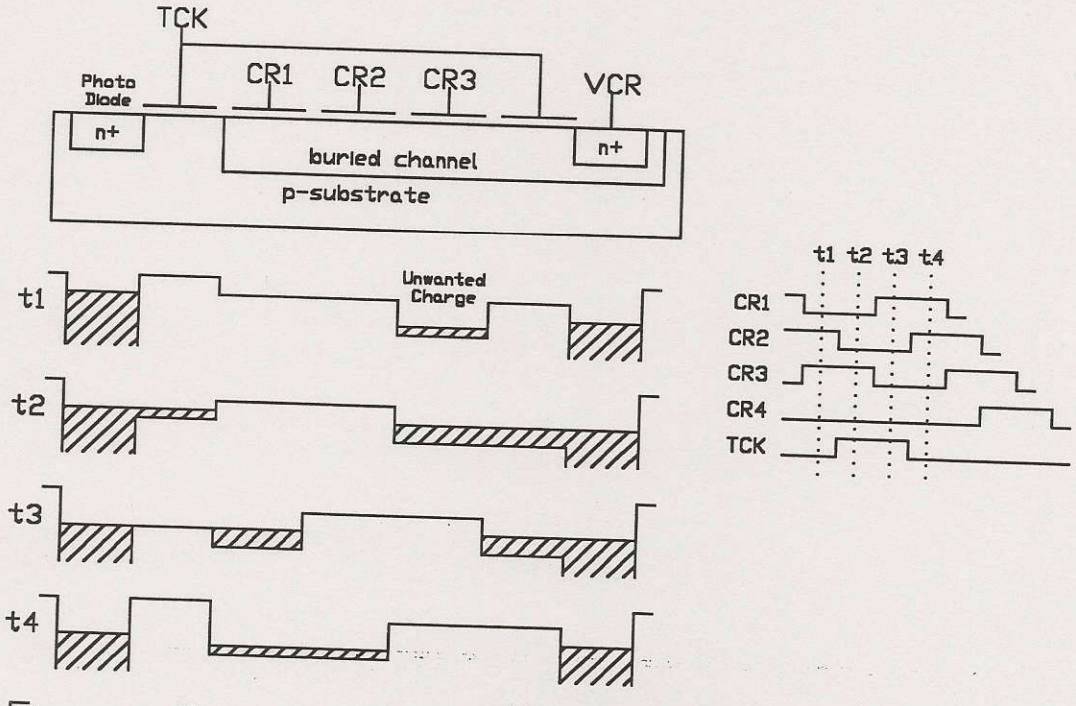

Figure 3 - Pixel Transfer/CCD Reset

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