A HIGH PACKING DENSITY PIXEL WITH PUNCHTHROUGH READ-OUT METHOD FOR AN HDTV INTERLINE-CCD

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Abstract; A new pixel structure for a high-packing-density interline CCD is proposed, in which signal charges are read out from the photodiodes to the vertical CCD by a punchthrough mechanism. This read-out method makes it possible to reduce the depth of the VCCD channel and the second p-well by implanting these two layers after diffusion of the photodiode n-layer. Spreading resistance measurements on dummy wafers show that the depths of these layers are 0.28 μm and 0.6 μm, respectively. Moreover, the photodiode n layer is covered with a surface p^+ layer, even at the transfer region. We describes the results of simulations and experiments on a test image sensor with pixel dimensions of 7.3 μm (H) x 7.6 μm (V). From the experimental data, we estimate the characteristics of an image sensor with pixel dimension 5.0 μm (H) x 5.2 μm (V). Such a device should have a maximum charge handling capability of 1.4×10^5 electrons, a smear level of -88 dB, a sensitivity of 1.5×10^3 electrons/lx with a 30% fill-factor, no image lag, and a low photodiode dark signal of less than 14 electrons at 60 ℃. These results indicate that an IL-CCD with a punchthrough read-out structure is suitable for image sensors with a high pixel density such as 2/3 inch 2 million pixel image sensors for high-definition TV applications.

I. INTRODUCTION

The demand for cheaper and more compact video equipment has created an inevitable trend towards reduction of the pixel size in CCD image sensors. As the pixel size is reduced, it becomes increasingly difficult to maintain a high charge handling capability in the vertical CCD (VCCD) and a low smear. The maximum charge handling capability has been increased by the usage of arsenic impurities for the VCCD channel, which allows the channel depth to be shallowed to 0.4 μm [12]. Nevertheless the charge handling capability is still insufficient for pixels smaller than 5.0 μm x 5.3 μm. Meanwhile, the problem of smear has been tackled by using frame interline transfer CCD image sensors (FIT-CCD) [1]. However, FIT-CCD sensors have a larger chip size than conventional interline transfer CCDs (IL-CCD).

In this paper, we propose a new IL-CCD pixel structure in which signal charges are read out from the photodiodes to the VCCD by a punchthrough mechanism. This read-out method makes it possible to increase the charge handling capability by reducing the depth of the VCCD channel. Also, it enables smear to be suppressed to the same extent as in FIT-CCDs by reducing the depth of the second p-well. Moreover, the proposed structure has a low photodiode dark current achieved by covering the surface of the photodiode n-layer with a surface p^+ layer, even at the transfer region.

II. LIMITATIONS OF CONVENTIONAL STRUCTURE

A cross-sectional view of the conventional pixel structure [2] is shown in Fig. 1. The low concentration p-well in the n-type substrate acts as a vertical overflow barrier to suppress blooming [3]. The low concentration n-well [4] reduces the substrate bias voltage at which charge overflows from the photodiode n-layer to the substrate. The VCCD consists of an n-type buried channel and double poly-silicon electrodes. The second p-well around the channel provides a potential barrier for smear reduction [5] [6]. The high concentration p-layer on the top of the photodiode n-layer helps suppress the dark current [7] [8].

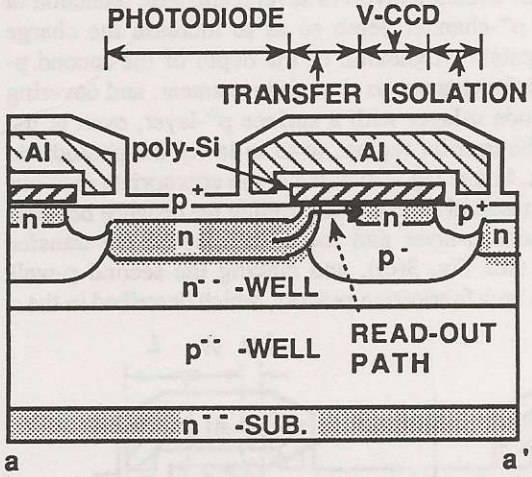

Fig. 1 Cross-sectional view of conventional pixel structure. Gray areas denote remaining n-type regions.

In this structure, signal charges are read out from the photodiode n-layer to the VCCD n-channel through the surface channel of the transfer MOS transistor. The poly-silicon electrode of the VCCD overlying the transfer region forms the gate of the MOS transistor [9]. This read-out scheme requires the photodiode n-layer to extend beneath the poly-silicon edge as the source of the MOS transistor. This results in a larger photodiode dark current, because the $Si-SiO_2$ interface under the polysilicon edge is depleted and its interface states are activated.

Moreover, the suppression of image lag brings about further restrictions in that the photodiode n-layer and the surface p-layer must both be implanted self-aligned to the edge

of the poly-silicon electrode in order to achieve a suitable source area under the electrode [10]. A results of this self-alignment is that the VCCD channel and the second p-well are subject to a thermal budget in forming the deep photodiode n-layer, because both layers must be formed before the poly-silicon electrode. As a result, the VCCD channel and the second p-well cannot be made any shallower, and the maximum charge handling capability is low, because of a low unit capacitance. Also, the smear level is high, because of the large area of the depletion layer around the channel.

Ⅲ. PUNCHTHROUGH READ-OUT STRUCTURE

A. Pixel structure

A cross-sectional view of the punchthrough read-out pixel structure is shown in Fig. 2. In this structure, the signal charges are read out from the photodiode n-layer to the VCCD through the bulk channel by a punchthrough mechanism. Consequently, there is no need for the transfer MOS transistor as used in the conventional structure, and there is no need for the photodiode n-layer to extend beneath the poly-silicon electrode as a source of the MOS transistor. Moreover, since there is no need for a source, the photodiode n-layer does not have to to be self-aligned to the edge of the polysilicon. As a result, the VCCD n^+-channel and the p-well can be made shallower by implanting them after the thermal step to form the photodiode n-layer.

In order to overcome the limitations of the conventional structure, this structure involves several changes: reduction of the VCCD n^+-channel depth so as to increase the charge handling capability, reduction of the depth of the second p-well around the channel so as to reduce smear, and covering the photodiode n-layer with a surface p^+-layer, even at the surface of the transfer region, so as to lower the photodiode dark current. Image lag is avoided at the appropriate read-out voltage as a result of precisely controlling the distance between the photodiode n-layer and the n^+-channel at the transfer region, *Lr*, (see Fig. 3(c)), and making the second p-well shallower. A new fabrication process, which described in the next section, fulfills these requirements. Isolation between the photodiode and the VCCD is achieved by making the distance between the photodiode n-layer and the n+ channel at the isolation region, *Li*, (see Fig. 3(c)) longer than that at the transfer region, *Lr*, and by separating the second n-well at the isolation region. These changes ensure that the potential at the isolation region is always higher than that at the transfer region.

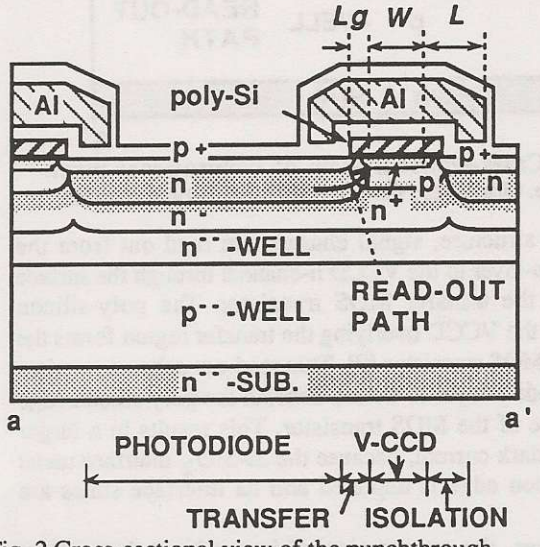

Fig. 2 Cross-sectional view of the punchthrough structure. Gray areas denote remaining n-type regions.

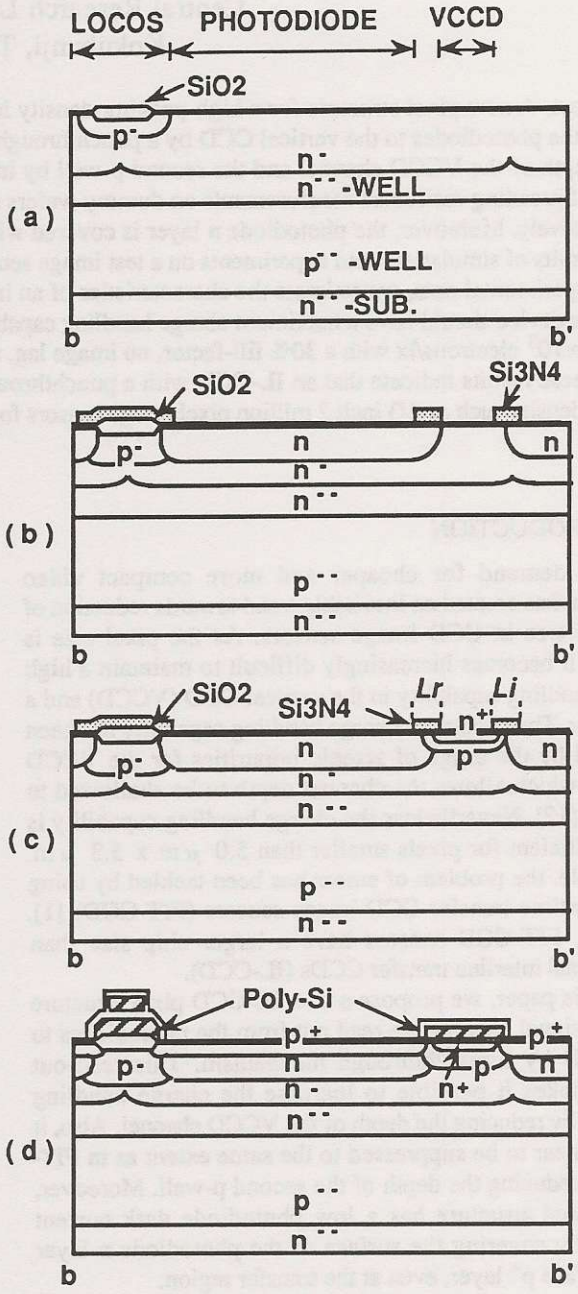

Fig. 3 Cross sectional view of the punchthrough structure during various stages of fabrication.

B. Fabrication Steps

The fabrication of the punchthrough read-out structure is illustrated in Fig. 3. After the p-well, the n-well and the second n-well are diffused in the n-type substrate, (a) a LOCOS region is formed to isolate the vertically adjacent photodiode, (b) a thin oxide layer is grown on the substrate,

and then Si_3N_4 is deposited and patterned on the photodiode and the VCCD area. Next, phosphorous is implanted into the photodiode area and diffused. After that, (c) arsenic and boron are implanted using the patterned Si_3N_4 mask, forming the VCCD buried channel and the second p-well, respectively. After low temperature gate oxidation, (d) the first poly-silicon is deposited with the addition of phosphorus gas (in-situ doping) and defined to form the gate electrodes. The second and the third poly-silicon electrodes are formed in the same way as the first. Then boron is implanted all over the pixels to form the surface high concentration p-layer.

In this process, the n^+ channel and the second p-well are made shallower by implanting both layers after the diffusion of the photodiode n layer, depositing the poly-silicons with in-situ doping and low temperature gate oxidation, and implanting the n^+ channel and the second p-well after the formation of the LOCOS. The thermal budget to the VCCD channel and the second p-well is summarized in Table I. Taking into account the dependence of diffusivity on temperature, all the thermal budget times were adjusted for a temperature of 1000℃. The total thermal budget is reduced to 1/10 that of the conventional process.The depths of the VCCD channel and the second p-well were calculated, and were also measured by the spreading resistance method [13] using dummy wafers. Their depth is defined as the distance from the surface to a point at which the concentration of the layer equals that of the substrate. Here, the concentration of a layer is assumed to have a Gaussian profile. The results are listed in Table II, which shows that the new process nearly halves the depths of the n^+ channel and the second p-well.

TABLE I
THERMAL BUDGET FOR THE VCCD CHANNEL AND THE SECOND P-WELL

Step	n-Channel Second p-well			
	Prop.	Conv.	Prop.	Conv.
Diffusion of Photodiode n-layer	0	415	0	415
Gate Oxidation, Doping to Gate electrode	60	325	60	325
LOCOS	0	160	0	160
Other	30	60	50	80
Total	90	960	110	980

UNITS: minutes at 1000℃

TABLE II
DEPTH OF THE VCCD CHANNEL AND THE SECOND P-WELL

	n-Channel Second p-well			
	Prop.	Conv.	Prop.	Conv.
Calculation	0.3	0.6	0.8	1.7
Measurement	0.28	0.42	0.6	1.3

UNITS: μm

In this process, the distances between the photodiode n-layers and the n^+-channel, *Lr*, *Li*, are defined by the width of Si_3N_4, as shown in Fig. 3 (c). As a result, the punchthrough voltage is precisely controlled. Also, the condition for making the distance at the isolation region, *Li*, longer than that at the transfer region, *Lr*, is ensured

IV. CHARACTERISTICS

To demonstrate the feasibility of the proposed structure, we fabricated a test sensor consisting of several lines of pixels, each with a pixel size of 7.3 μm (H) x 7.6 μm, suitable for a 1-inch 2-million-pixel sensor. The channel width of the VCCD, *W*, the distance from the edge of the VCCD n-channel to the edge of the aluminum (the light shield length), *L*, and the distance from the edge of the VCCD n-channel to the edge of the poly-silicon electrode, *Lg*, (see Fig. 2) were varied between these lines, but the center values were as follows: *W* was 1.2 μm, *L* was 1.0 μm both on the transfer region and on the isolation region, and *Lg* was 0.3 μm, resulting in an optical aperture ratio of 40%. These devices were all fabricated with three poly-silicon and two aluminum layers. The minimum width of the poly-silicon electrodes was 0.8 μm. In all cases, the gate oxide thickness was 35 nm, and the oxide thickness between the aluminum and the substrate, t_{ox}, was 330 nm. Our measured results are shown in comparison with the results of our simulations.

A. Maximum Charge Handling Capability

We performed a two-dimensional computer simulator of both the punchthrough and the conventional read-out structure, with the electrode biased to the peak voltage of the transfer pulse. We calculated the charge stored when the static potential under the electrode was reached 1 V lower than that when the electrode was biased at the low voltage of the transfer pulse. We assumed that the punchthrough structure has a VCCD channel depth of 0.3 μm and a gate oxide thickness of 35 nm, and that the conventional structure has a VCCD channel depth of 0.6 μm and gate oxide thickness 50 nm. The results are shown in Fig. 4. The Simulation indicates that the maximum charge handling capability is nearly twice as large in the punchthrough structure.

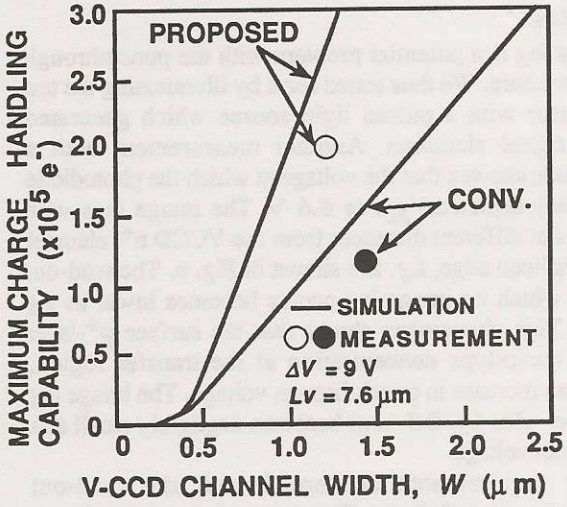

Fig. 4 Maximum charge handling capability. ΔV denotes the clockswing and Lv denotes twice the channel length.

We also performed experiments on test image sensors, and measured the maximum charge which could be stored

without overflowing to an empty neighbor. These charges were input to the VCCD using a potential equilibrium method. The clockswing swing, ΔV, was set at 9 V. These results are also shown in Fig. 4. The measured values confirm the simulations, and the maximum charge handling capability reaches $2x10^5$ electrons at a 1.2 μm channel width.

B. Smear

We carried out two-dimensional simulation using the device simulator CADDETH [14]. As shown in Fig. 5, by reducing the depth of the second p-well around the channel from 1.7 μm to 0.8 μm, the smear level is reduced by about 10 dB when the light shield length, L, is 1.0 µm. Measurements for three pixels with different light shield lengths confirm these simulations, and show that the smear level reaches -98 dB at L=1.0 µm.

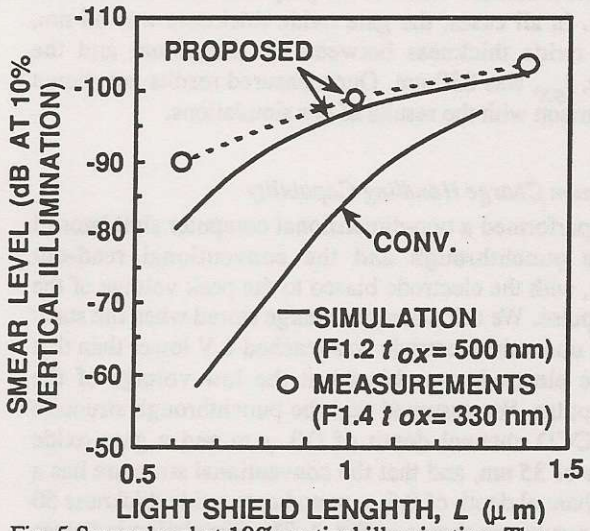

Fig. 5 Smear level at 10% vertical illumination. The parameter *tox* denotes the oxide thickness between the aluminum and the substrate.

C. Image Lag

Image lag is a potential problem with the punchthrough read-out structure. We thus tested for it by illuminating the test image sensor with a pulsed light source which generated $1.1x10^4$ signal electrons. Another measurement with a dummy diode showed that the voltage at which the photodiode is completely depleted, V_{PD}, is 6.6 V. The image lags with three pixels at different distances from the VCCD n^+- channel to the polysilicon edge, Lg, are shown in Fig. 6. The read-out voltage at which no image lag occurs becomes lower as Lg increases. This phenomena shows that the surface p^+-layer heightens the p-type concentration at the transfer region, leading to an increase in punchthrough voltage. The image lag for the pixel with Lg=0.3 μm becomes negligibly small at a 10 V read-out voltage.

Other requirements concerned with the read-out characteristics are as follows: First, to prevent excess charge overflowing to the VCCD, the potential barrier between the photodiode and the substrate must be lower than that between the photodiode and the VCCD when the transfer pulse voltage is high. Secondly, to achieve highly saturated photodiode signals, this potential barrier must be sufficiently higher than the photodiode potential when the photodiode n-layer is completely depleted. Experiments on the pixels with an of Lg=0.3 μm showed that excess charges stop overflowing to the VCCD channel at a substrate voltage of 16.5V, at which point the high voltage of the transfer pulse is -2V. This result show that the potential barrier condition is satisfied under a reasonable substrate bias. Measured saturation signal of the photodiode under this condition reaches to $0.8x10^5$ electrons. This saturation signal is small compared to the maximum charge handling capability of the VCCD, $2x10^5$ electrons, but improvements can be made by heightening the potential barrier between the photodiode and the VCCD to the extent of the read-out voltage reaching 15 V. In summary, measurements of the substrate bias voltage and the saturation signal show that the punchthrough read-out structure satisfies the two requirements above as well as suppressing image lag.

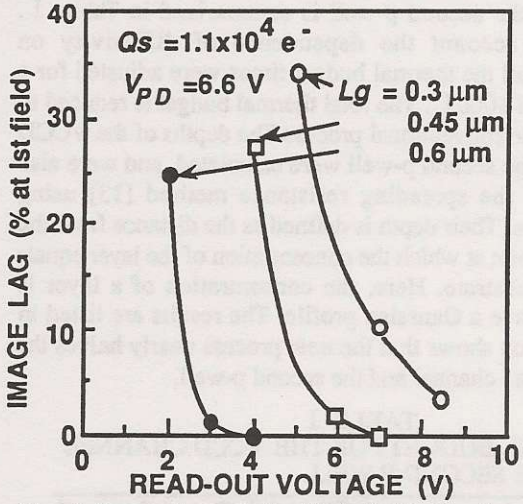

Fig. 6 Image Lag at the first field. Qs denotes signal charge and V_{PD} denotes the voltage at which the photodiode is completly depleted.

D. Photodiode Dark Current

The photodiode dark currents generated at the transfer region were measured using dummy diodes. The poly-silicon electrode was DC-biased and the current flowing to the photodiode was measured. The results are given in Fig. 7. In the conventional structure, the dark current begins to increase at -2 V because the surface of the photodiode n-layer under the electrode begins to deplete. On the other hand, the dark current remains constant up to 0 V in the proposed structure with Lg=0.3 μm. This phenomenon shows there is no depletion region at the $Si-SiO_2$ interface in the transfer region. Another measurement with the test image sensor showed that the photodiode dark signal is 14 electrons at 60℃, which is lower than that of the conventional structure, 20 electrons. These results confirm the punchthrough read-out structure eliminates the depletion region at the $Si-SiO_2$ interface in the transfer region, and reduces the photodiode dark current.

E. Sensitivity

The photoconversion characteristics measured with the test image sensor, which has a 40% fill-factor, show that its sensitivity to a 2856 K tungsten lamp reaches $4.2x10^3$ electrons/lx with an IR cut filter.

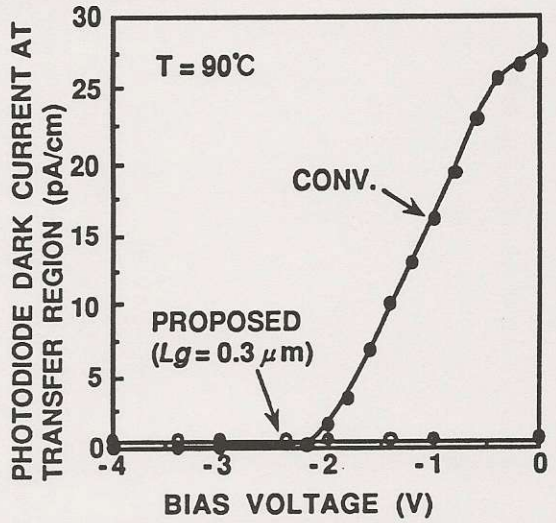

Fig. 7 Photodiode dark current at the transfer region measured as a function of the polysilicon DC-bias using a dummy diode.

VI. ESTIMATION OF PERFORMANCE OF 2/3-INCH HDTV IMAGE SENSOR

Using the data measured for the test image sensor with pixel dimensions 7.3 μm x 7.6 μm, it is possible to estimate the characteristics of an image sensor with pixel dimensions 5.0 μm x 5.2 μm, which would be suitable for 2/3 inch HDTV image sensors. As summarized in Table Ⅲ, such a device should have a maximum charge handling capability of 1.4×10^5 electrons with a 1.2 μm VCCD channel width, a smear of -88 dB with a 0.8 μm light-shield length, a sensitivity of 1.5×10^3 electrons/lx with a 30% fill-factor, no image lag, and a low photodiode dark signal of less than 14 electrons at 60℃. These results indicate that an IL-CCD with a punchthrough read-out structure is suitable for image sensors with a high pixel density such as 2/3 inch 2 million pixel image sensors for HDTV applications.

TABLE Ⅲ
ESTIMATED CHARACTERISTICS OF A 2/3-INCH HDTV SENSOR WITH THE PUNCHTHROUGH PIXEL STRUCTURE

Image Format	2/3 inch
Number of Pixels	1920 (H) x 1035(V)
Pixel Size	5.0 (H) x 5.2 (V) μm^2
Chip Size	11.6 (H) x 8 (V) mm^2
Maximum Charge Handling Capability	$1.4 \times 10^5 e^-$
Smear Level	-88 dB (1/10 V F1.4)
Sensitivity (2856 K, with IR Cut Filter)	$1.5 \times 10^3 e^-$/lx
Image Lag	None
Photodiode Dark Current	<14 e^- (60℃)

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