A Review of Photo Detector Elements for Interline CCD

T. H. Lee and B. C. Burkey
Eastman Kodak Company
Rochester, NY 14650-2008

Outline

- Introduction
  - Photo Capacitor
  - np Junction Photodiode
  - Photoconductor Layers
  - p^+np Multiple Junction Photodiode
- Problems and Issues of Photo Detector Elements
  - Lag
  - Charge Capacity
  - Photo Response
  - Blooming control
  - Electronic Shutter
  - Crosstalk and Smear
  - Non-linearity
  - Dark current and Noise

Operation of *p-n* Junction Photodetectors in a Photon Flux Integrating Mode

GENE P. WECKLER, MEMBER, IEEE

Abstract—A technique for operating a *p-n* junction photodiode in a photon flux integration mode is described. In this mode the *p-n* junction is charged to a reverse voltage (less than its breakdown voltage) and then open-circuited. The voltage across the junction, with zero incident illumination, will decay at a rate that is independent of junction area. Time constants in the order of seconds may be achieved with silicon planar structures at room temperature. Under illumination, the rate of decay of charge depends linearly on the intensity of the incident illumination, so that the total charge removed is proportional to the time integral of illumination.

Operation of *p-n* junction photodiodes is analyzed for this mode and boundary conditions are established. A practical structure utilizing this mode of operation is discussed. This structure makes use of the nearly ideal switch characteristics of an insulated gate field-effect transistor to periodically sample a photodiode. Advantages offered by this device structure include 1) linear dependence of signal charge on light intensity over several orders of magnitude; 2) electronically controllable sensitivity; 3) ease of integration into arrays for image sensing.

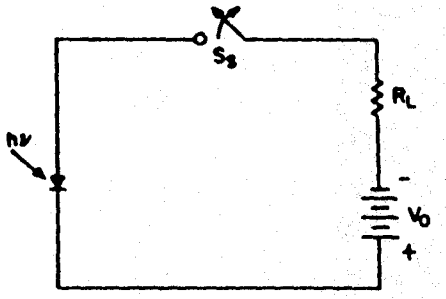
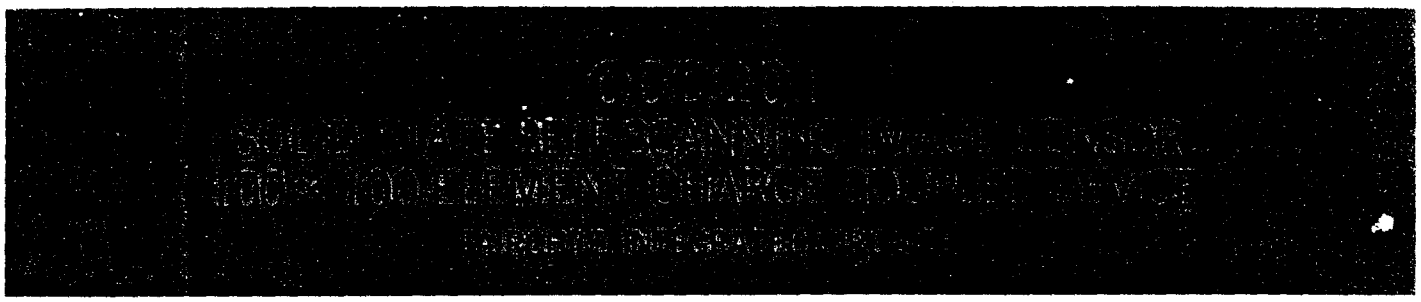


Fig. 1. An idealized circuit for analyzing storage mode operation of a *p-n* junction diode.



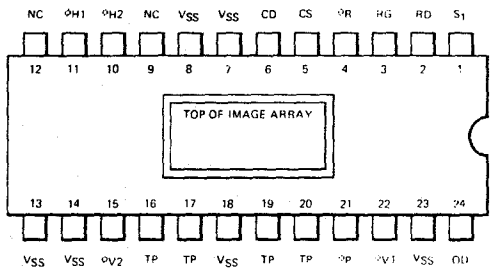
GENERAL DESCRIPTION – The CCD201 is a 2-Phase 10,000-Element Self-Scanning Image Sensor. It uses charge coupled technology with buried channels and ion-implanted barriers. The light sensitive area is a 100 x 100 array of photo elements which provide an image aspect ratio of 4 x 3. The image sensing elements are 1.2 mils x 0.8 mils located on 1.2 mil vertical centers and 1.6 mil horizontal centers.

In addition to the image sensing array, the CCD201 chip includes: 100 columns of 2-phase analog shift registers interdigitated in the photosensor array, a 102-element 2-phase analog output shift register, an output detector/preamplifier and a compensation output amplifier.

The device is packaged in a 24-lead Dual In-Line package with an optical glass window.

- **2-PHASE CLOCK OPERATION**
- **100 x 100-ELEMENT ARRAY ON A SINGLE CHIP**
- **INTERLACED SELF SCANNING**
- **ALL OPERATING VOLTAGES UNDER 20 V**
- **ON-CHIP VIDEO PREAMPLIFIER AND COMPENSATION CIRCUIT**
- **LOW POWER 50 mW TYP**
- **PACKAGED IN 24-LEAD DIP WITH OPTICAL GLASS WINDOW**

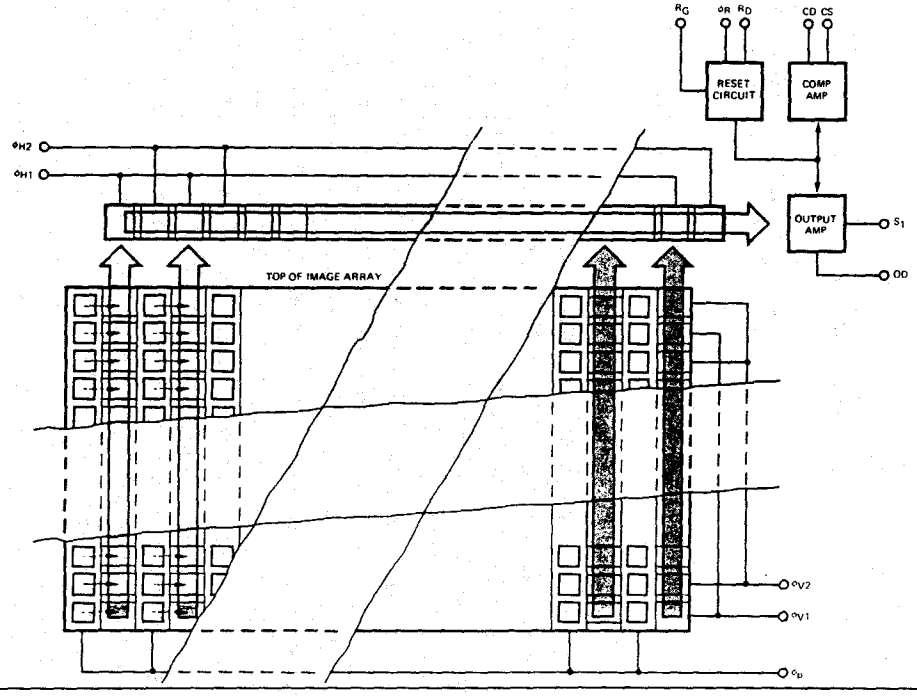
CONNECTION DIAGRAM
DIP (TOP VIEW)



LEAD NAMES

SYMBOL	FUNCTION
S_1	Output Amplifier Source
RD	Reset Drain
RG	Reset Gate
ϕ_R	Reset Clock
CS	Compensation Amplifier Source
CD	Compensation Amplifier Drain
ϕ_{H1}, ϕ_{H2}	Horizontal Register Clocks
ϕ_{V1}, ϕ_{V2}	Vertical Clocks
ϕ_P	Photogate Clock
OD	Output Amplifier Drain
TP	Production Test Points

BLOCK DIAGRAM



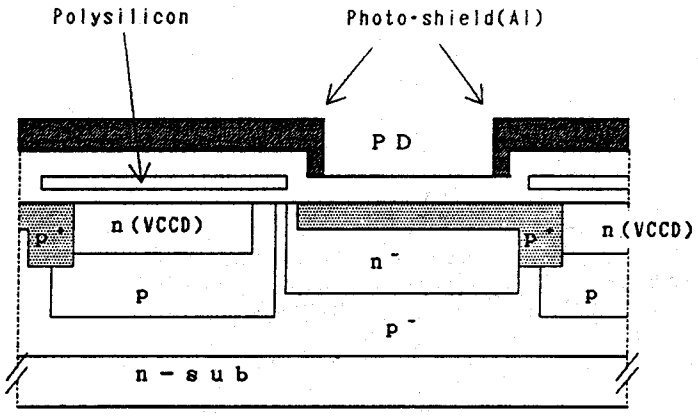


Fig. 5. Cross-sectional view of a unit cell.

Kuriyama et al

IEEE Trans

ED-38

May 1991

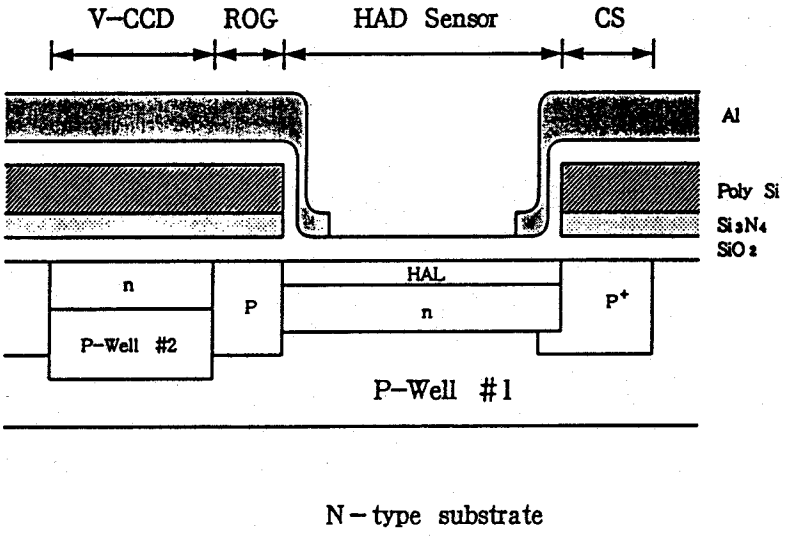


Fig. 3. Schematic cross-sectional view of the unit cell.

Hojo etal

IEEE Trans

ED-38

May 1991

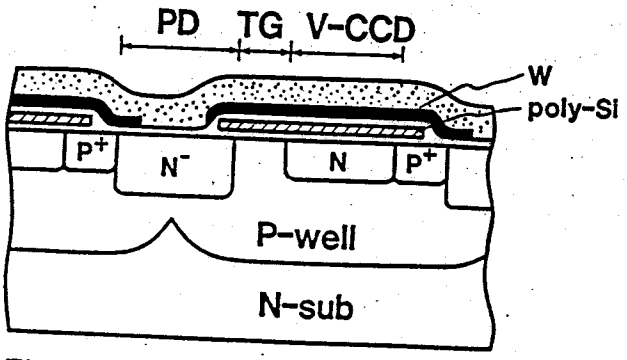


Fig. 5. Cross-sectional view of a unit pixel.

Toyoda et al

IEEE Trans ED-38

May 1991

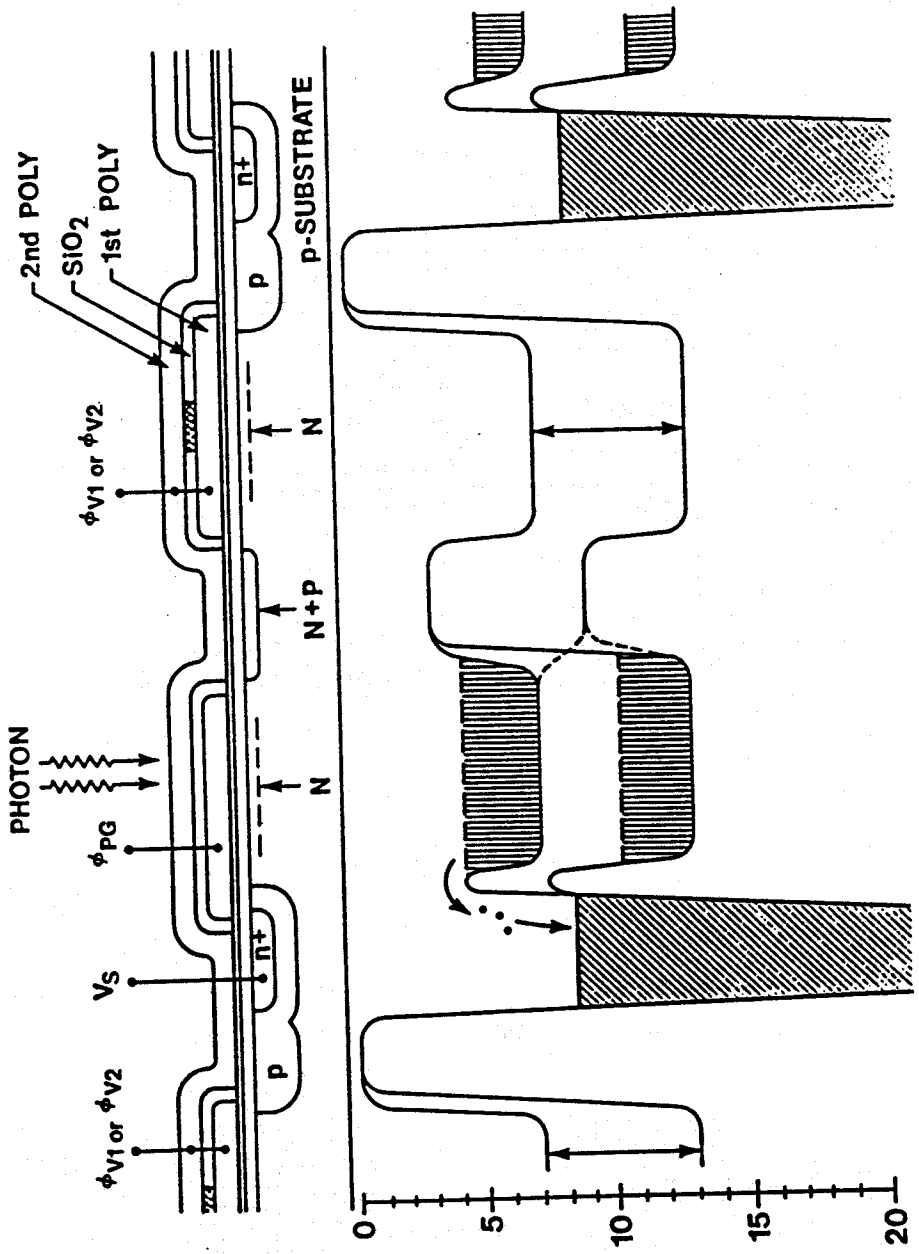


FIG. 2. PHOTOCELL CROSS-SECTION

SONY

TOP AND CROSSSECTIONAL VIEWS OF THE CCD IMAGER

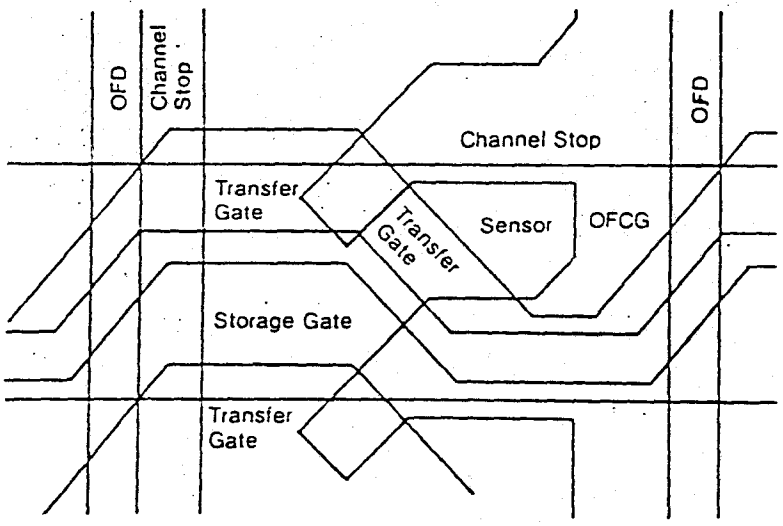


FIG. 5-1 TOP VIEW

OFG: Overflow Drain
OFCG:. Overflow Control Gate

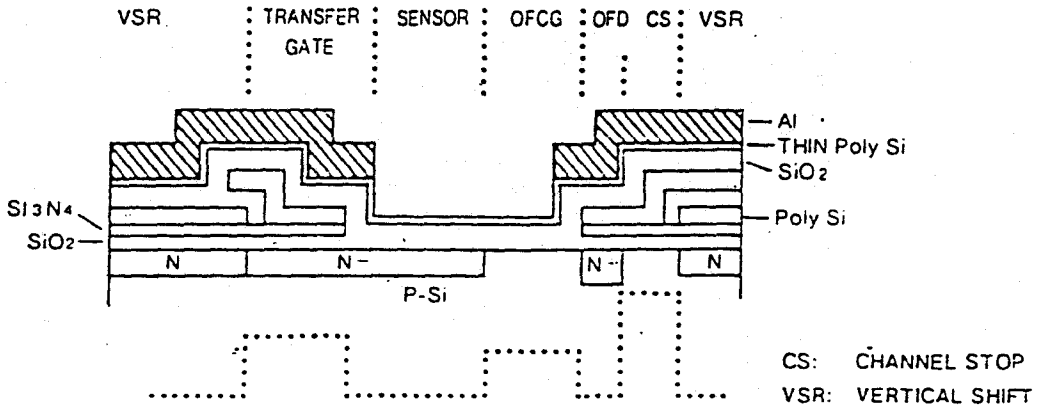


FIG. 5-2 CROSSSECTIONAL VIEW

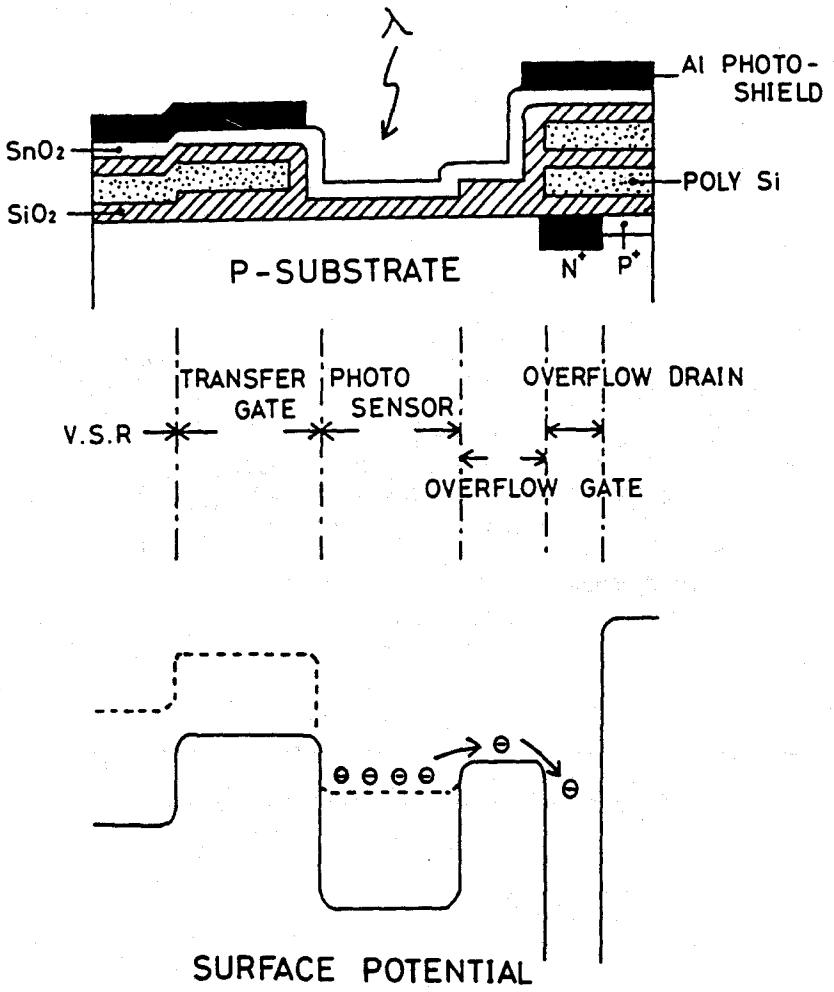


FIGURE 3—Cross sectional view and surface potential of antiblooming system.

Matsumoto et al / SONY

ISSCC 1978

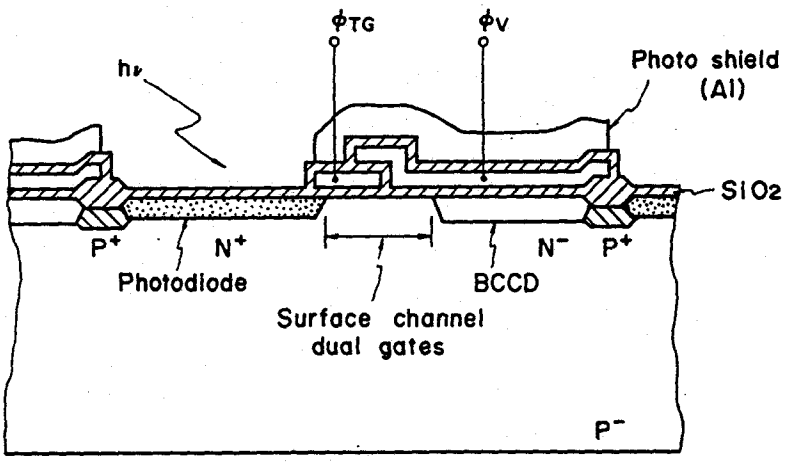
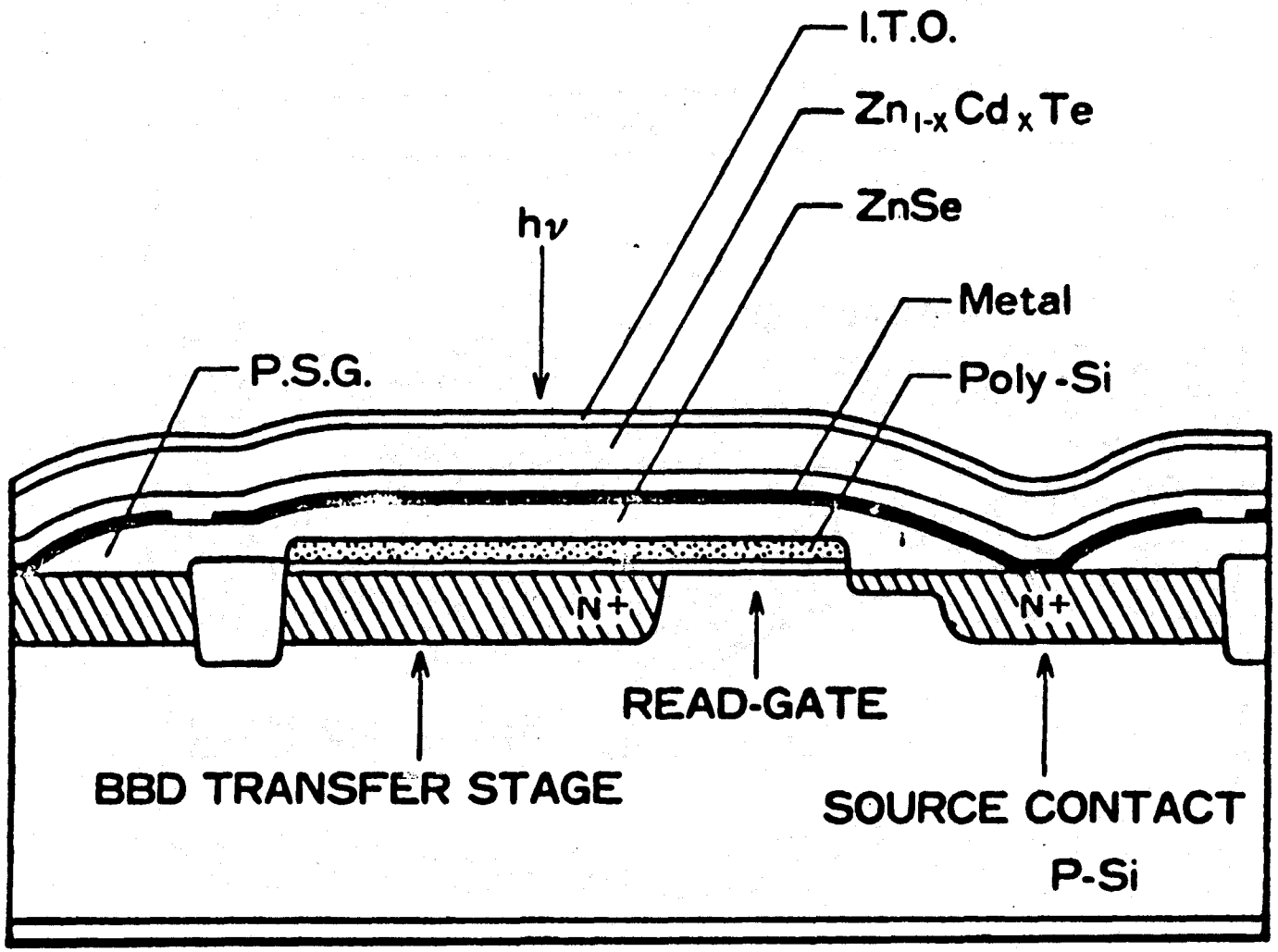


FIGURE 2—Cross sectional view of a unit cell.

Ishihara et al

ISSCC, 1980



Ref. Terui et al
ISSCC Tech. Digest
1980 p. 34

S.Manabe, et al.," A 2 Million Pixel CCD Imager Overlaid with an Amorphous Silicon Photoconversion Layer "

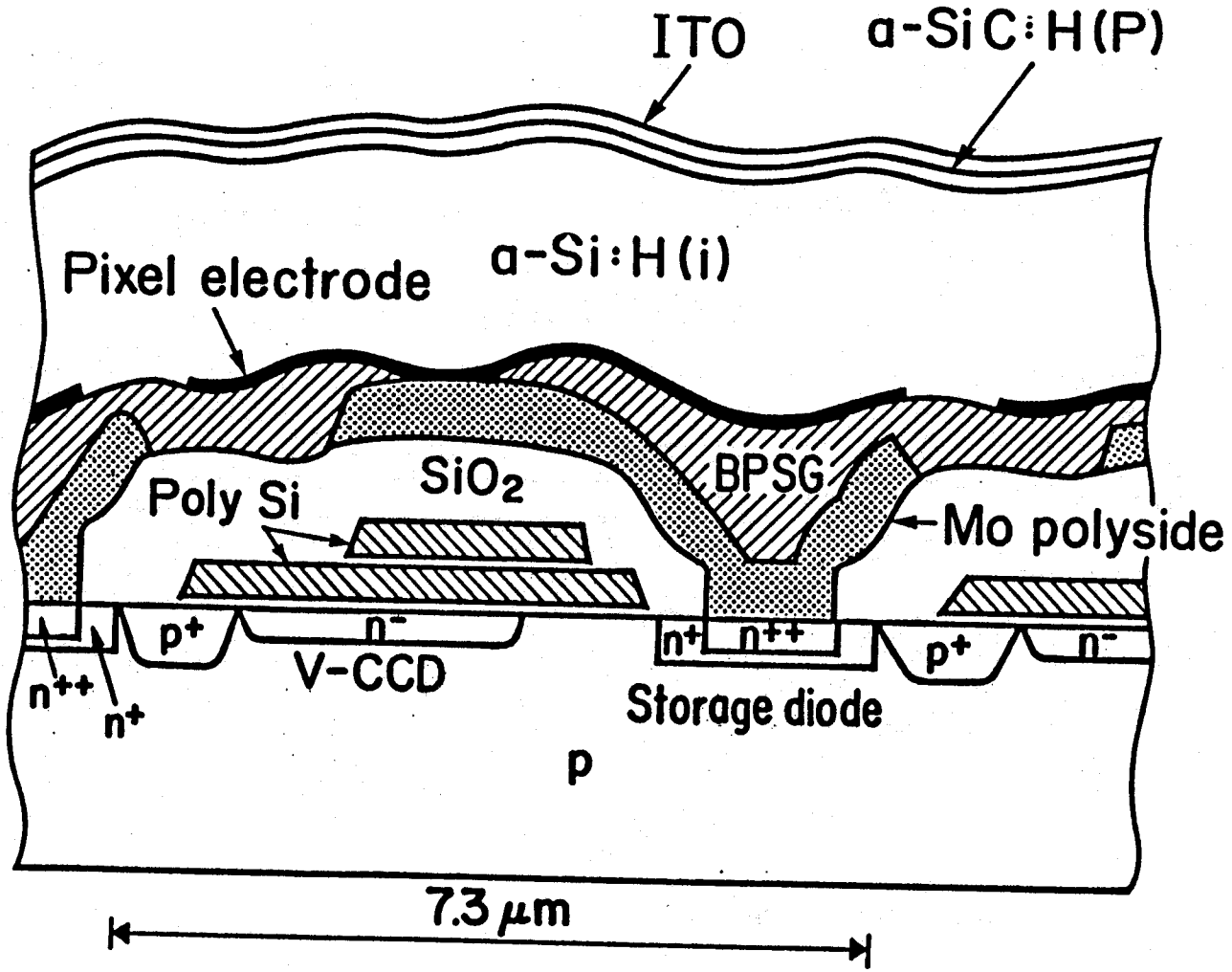
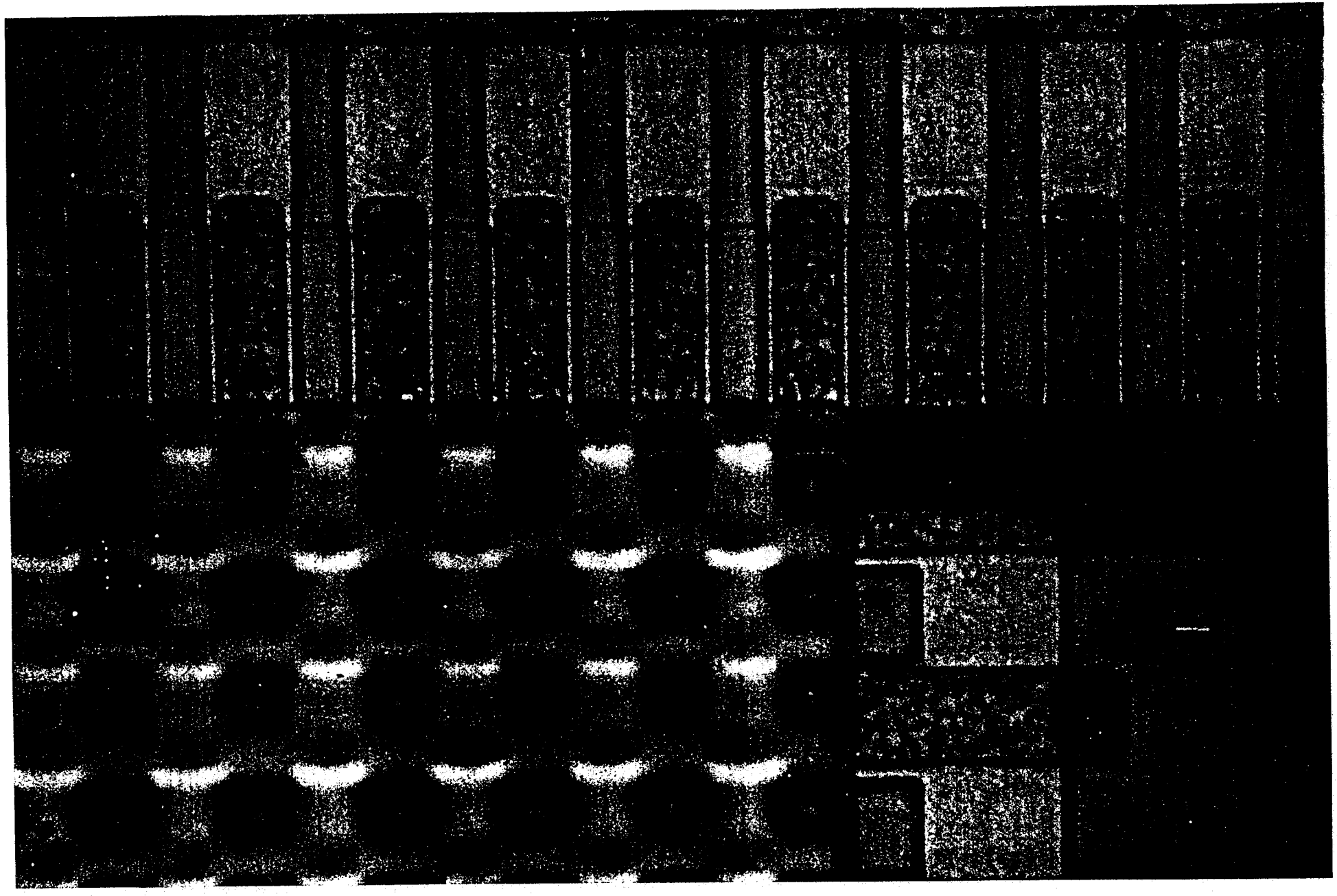
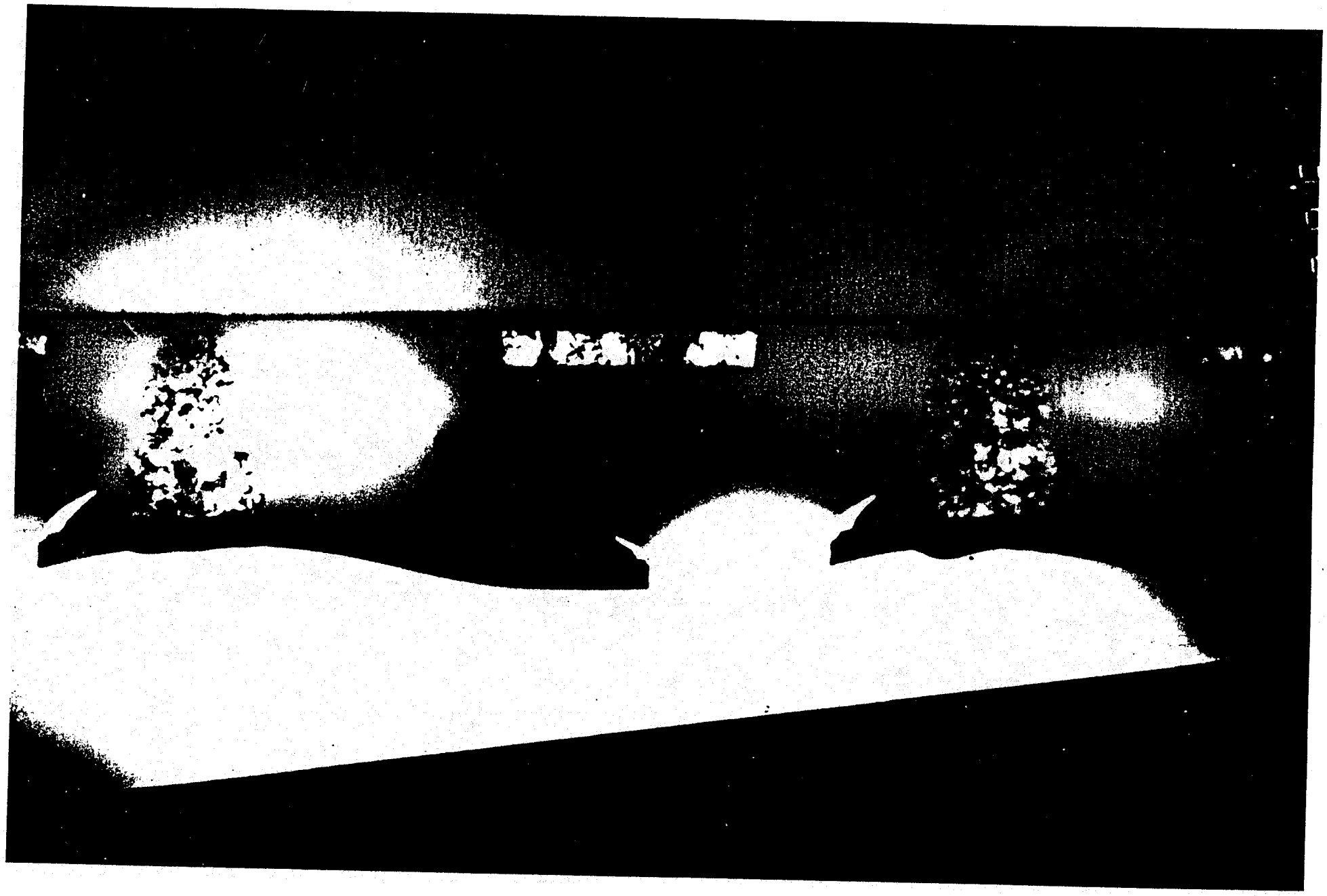


FIGURE 2 Cross section view of unit cell





NO IMAGE LAG PHOTODIODE STRUCTURE IN THE INTERLINE CCD IMAGE SENSOR

Nobukazu Teranishi, Akiyoshi Kohono, Yasuo Ishihara, Eiji Oda and Kouichi Arai

Microelectronics Research Laboratories, Nippon Electric Co., Ltd.

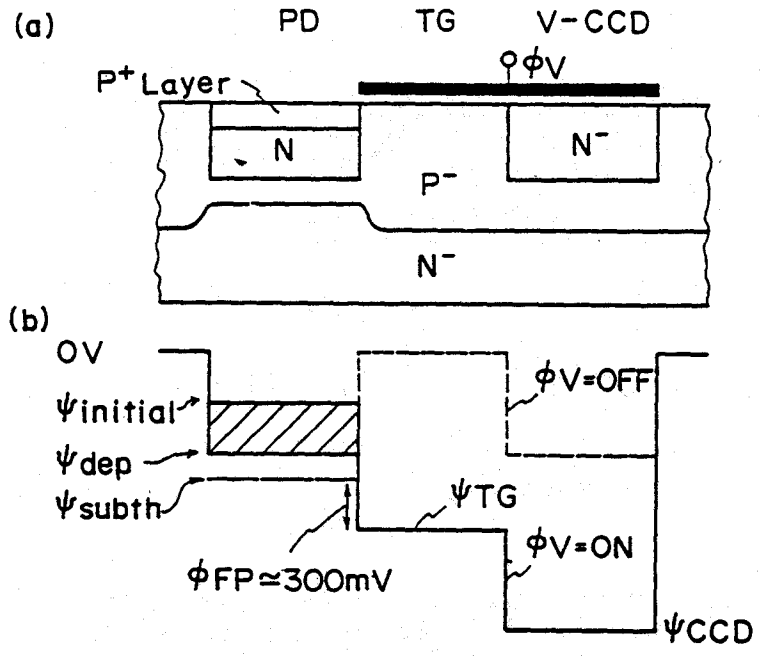


Fig.5. P^+NP^- structure photodiode
(a) Unit cell cross sectional view
(b) Potential profile in a complete transfer mode

IEDM 82

THE PINNED PHOTODIODE FOR AN INTERLINE-TRANSFER CCD IMAGE SENSOR

B. C. Burkey, W. C. Chang, J. Littlehale, T. H. Lee,
T. J. Tredwell, J. P. Lavine, E. A. Trabka

Research Laboratories, Eastman Kodak Company
Rochester, New York 14650

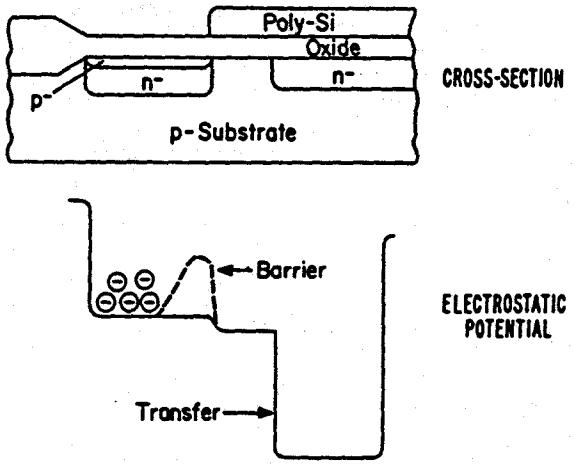
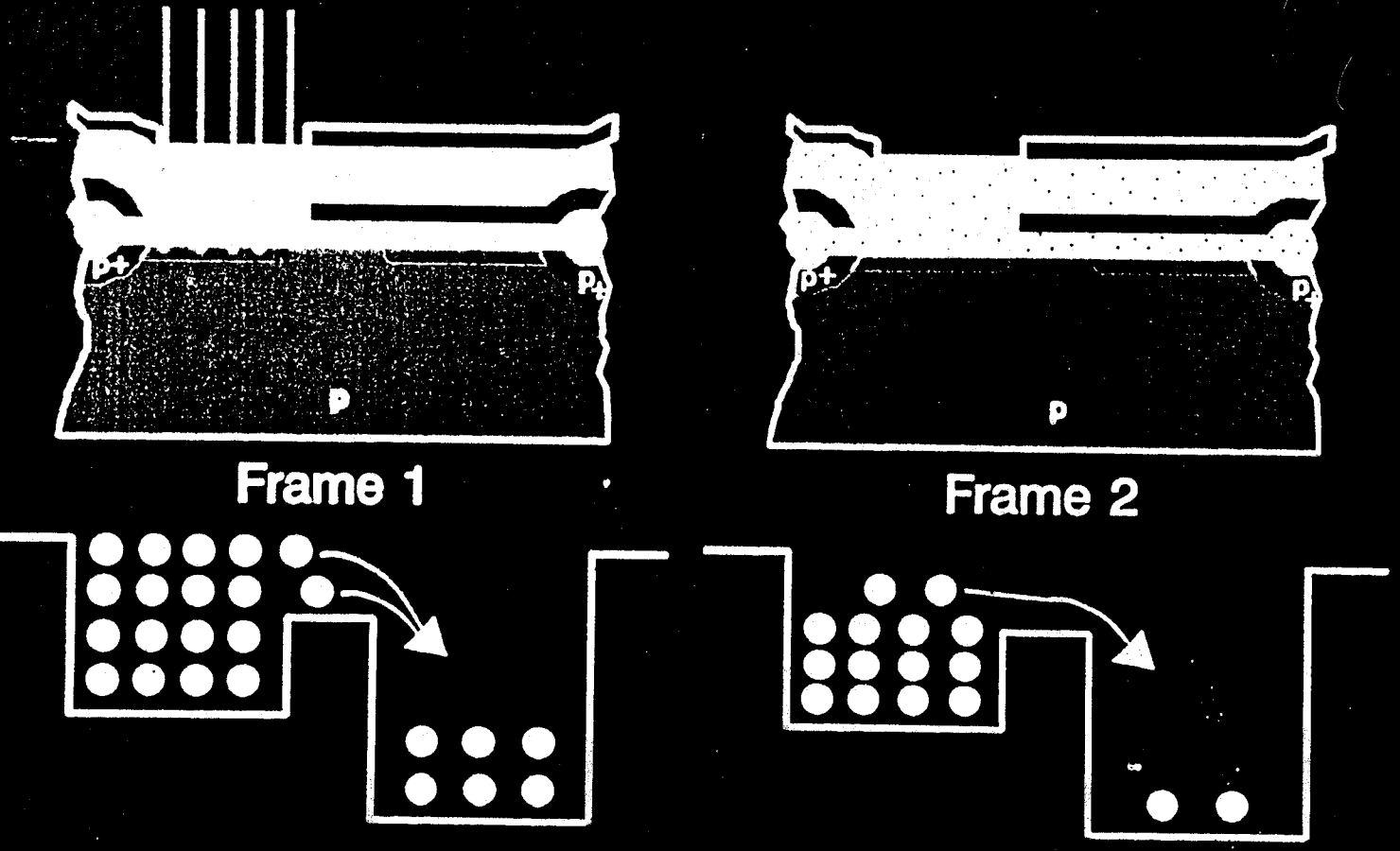


Fig. 8. Image cell schematic indicating a potential barrier at the edge of the transfer gate.

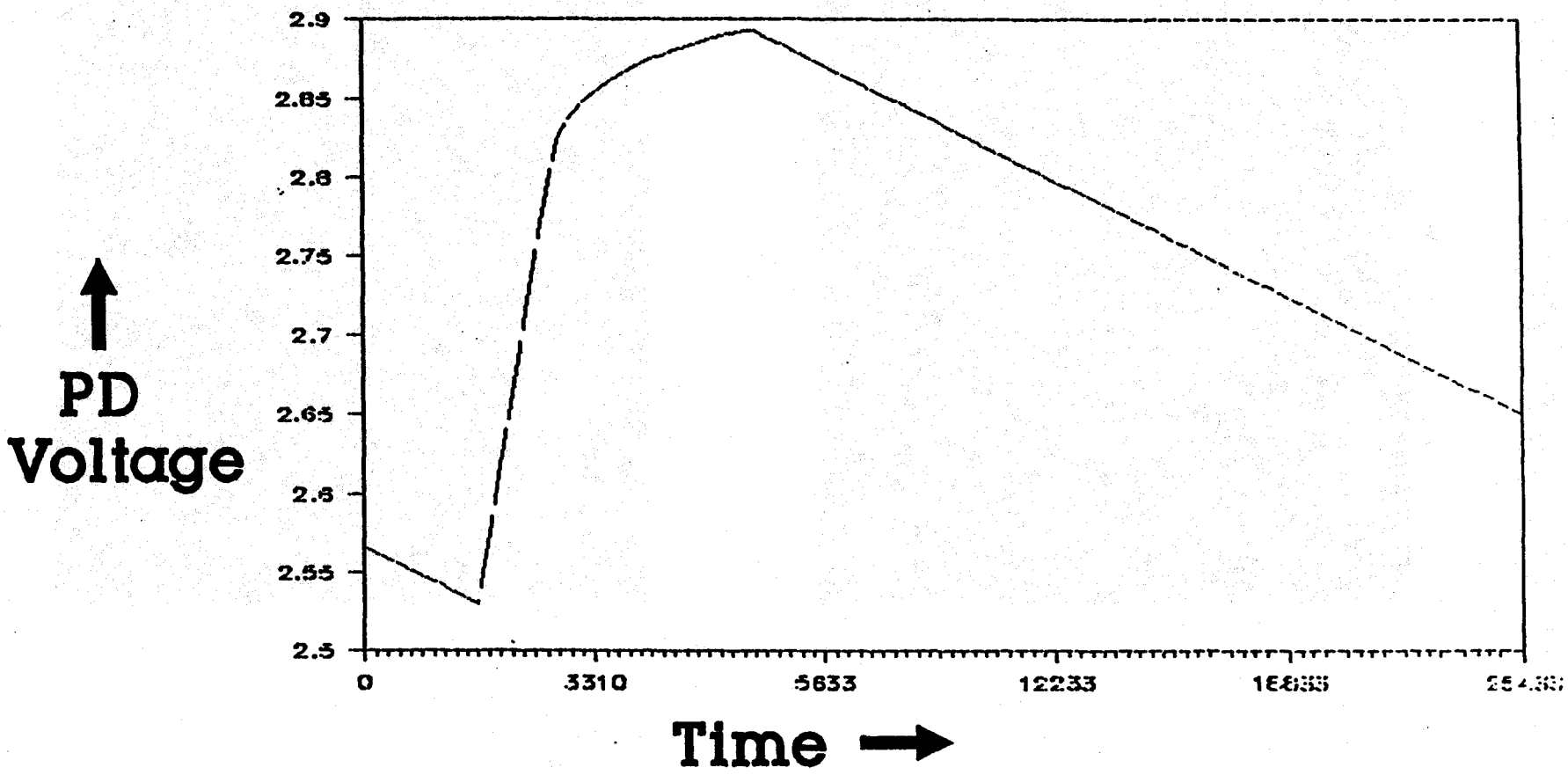
LAG IS DUE TO INCOMPLETE READOUT OF THE PHOTOSIGNAL FROM A DIODE.

CHARGE LEFT BEHIND IS READ OUT IN SUBSEQUENT FRAMES, CAUSING GHOST IMAGES TRAILING MOVING OBJECTS.

LAG IN CCD IMAGE SENSORS

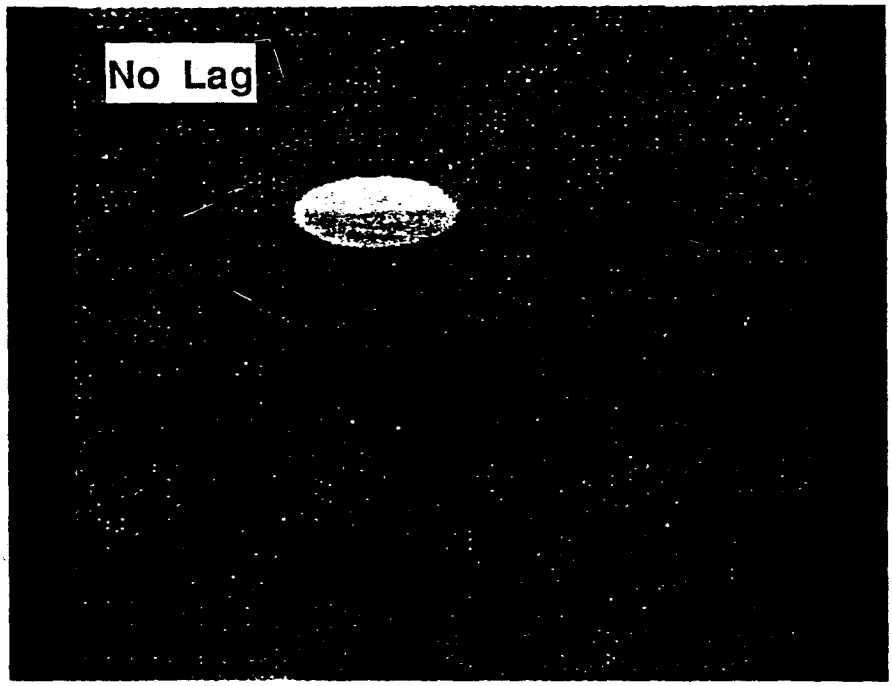


Photodiode Voltage vs Time

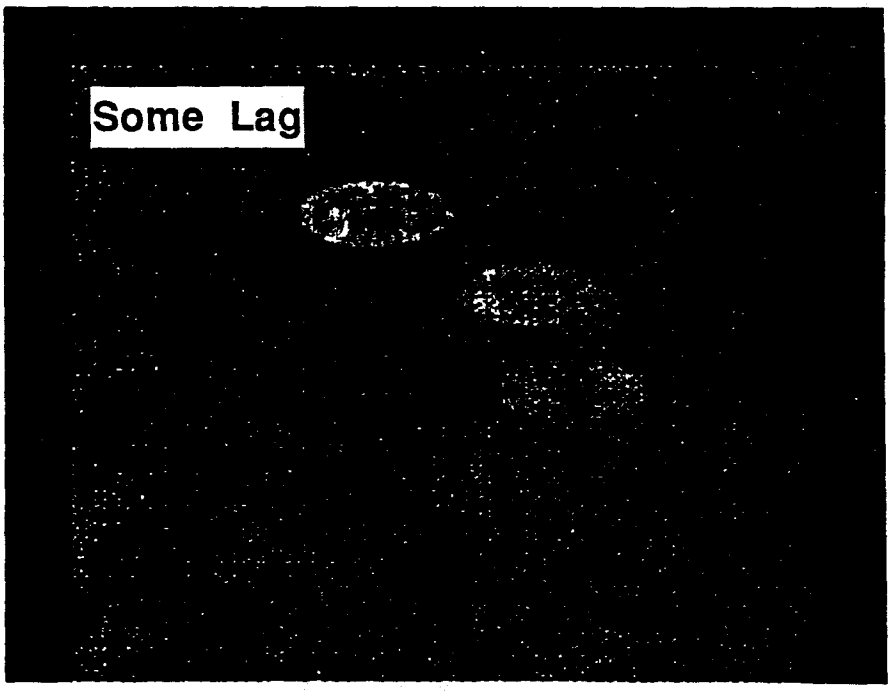


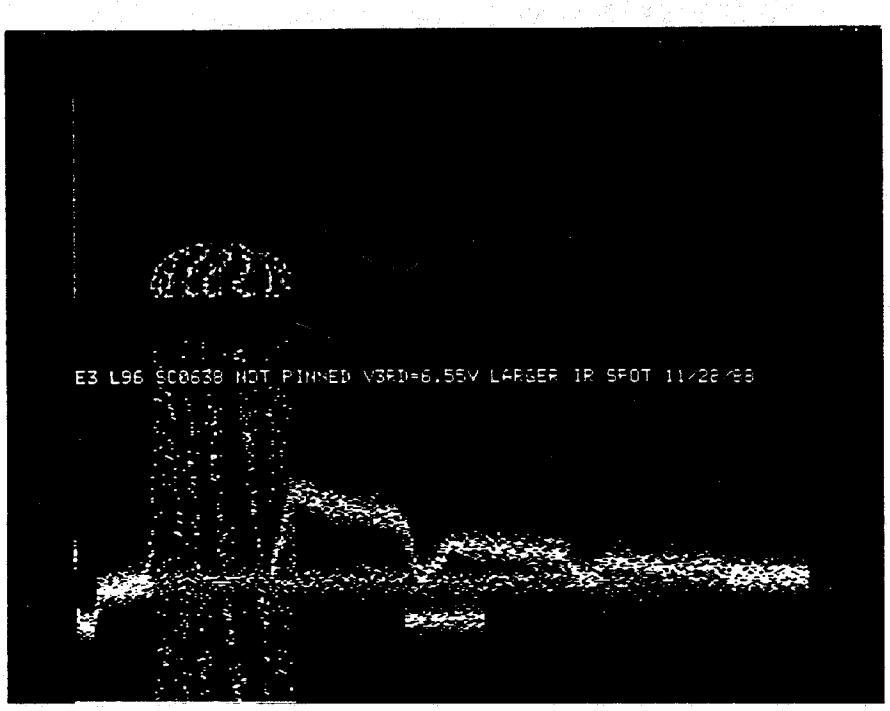
LAG vs CLOCK LEVEL

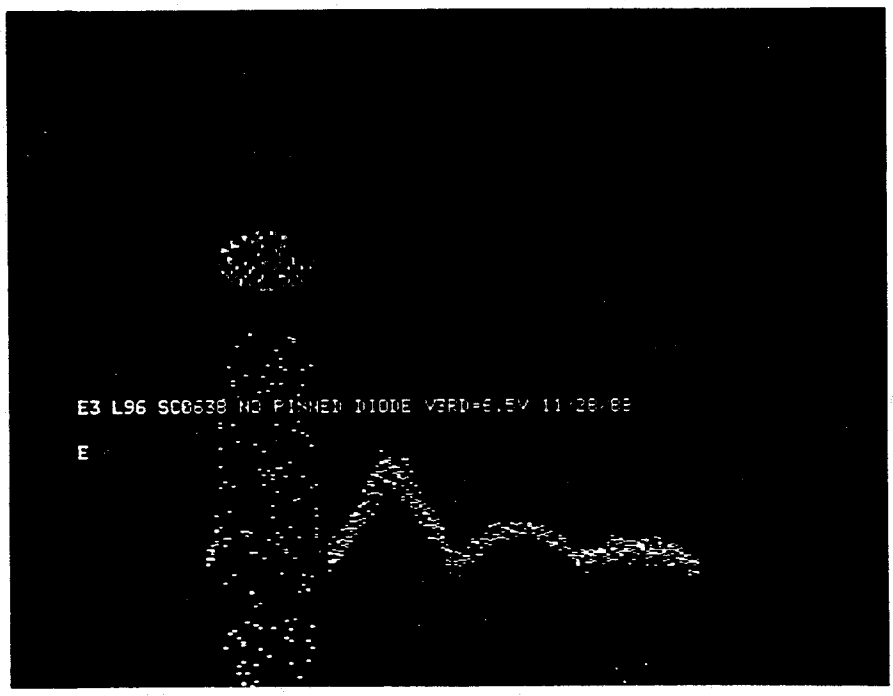
NORMAL CLOCKING
V3RD=10V
NO LAG!



MISADJUST V3RD
TO INDUCE LAG
V3RD=3.4V




E3 L96 SC0638 NOT PINNED VRD=6.55V LARGER IR SPOT 11/28/88


E3 L96 SC0638 NO PINNED DIODE VRD=6.5V 11/28/88
E

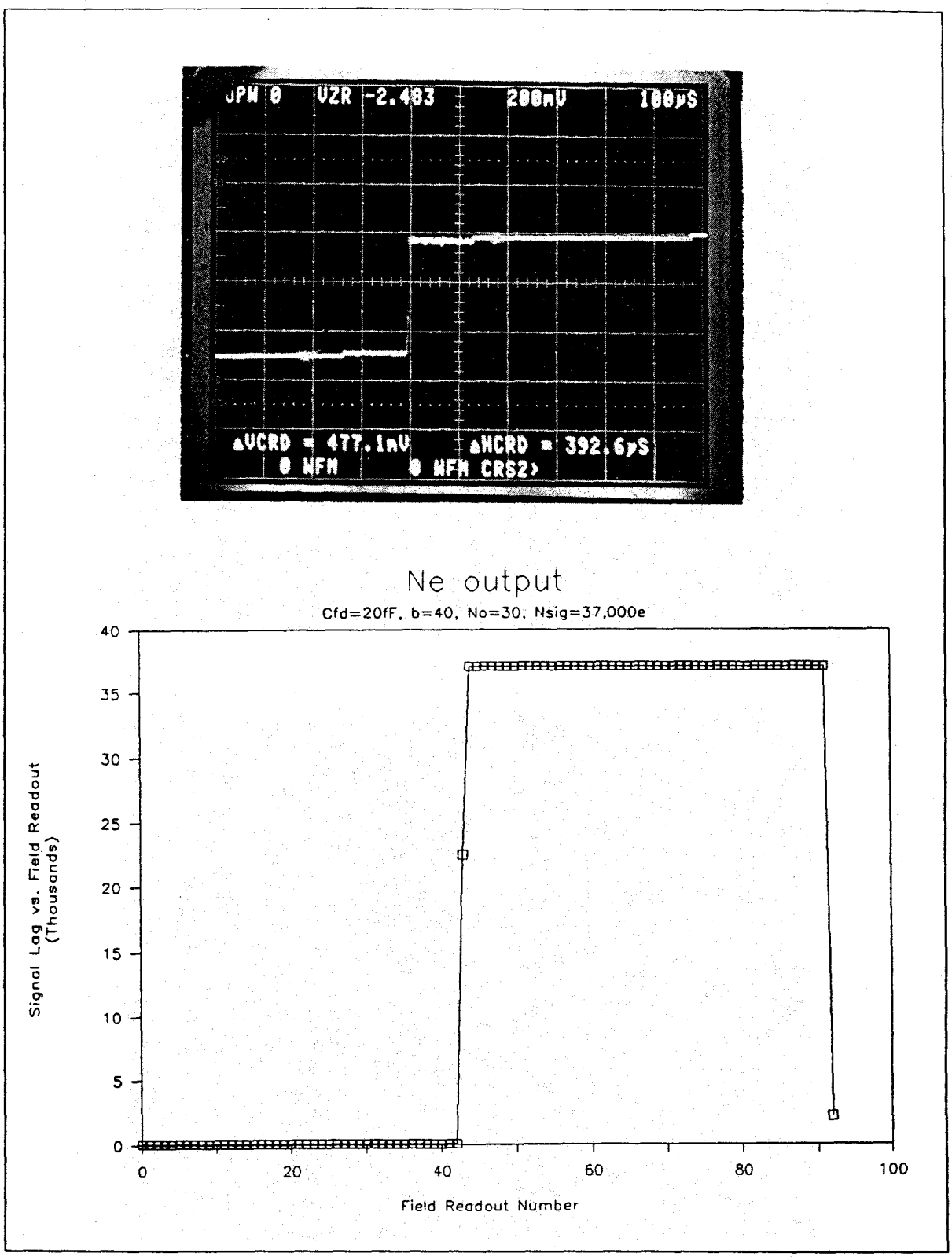
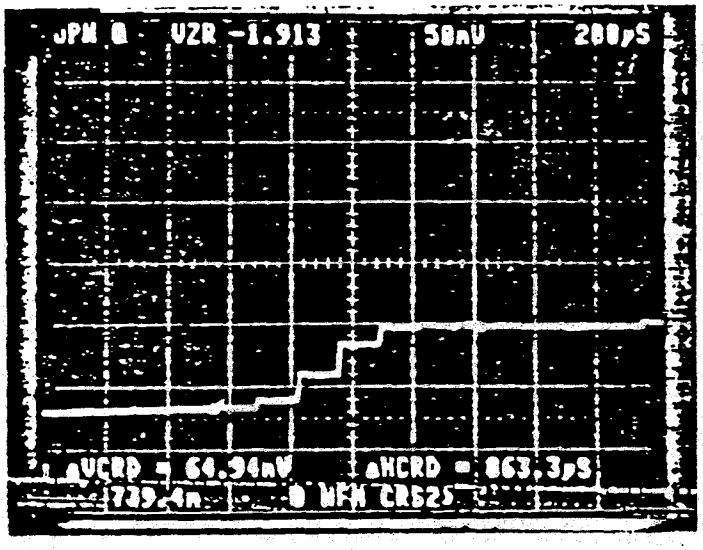


Figure 5-50. Signal lag with unpinned photodiode — 37,000 electrons signal. Run 3C-01.



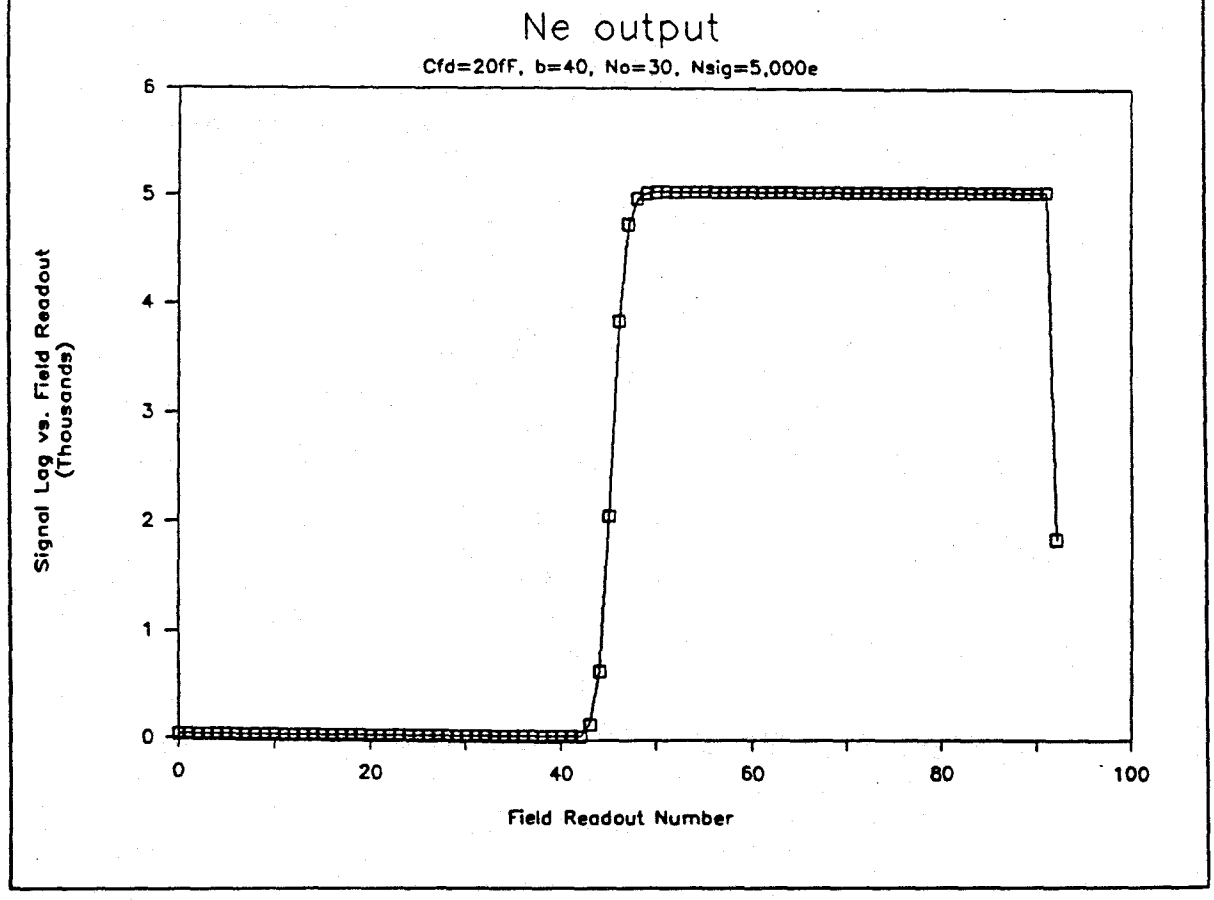
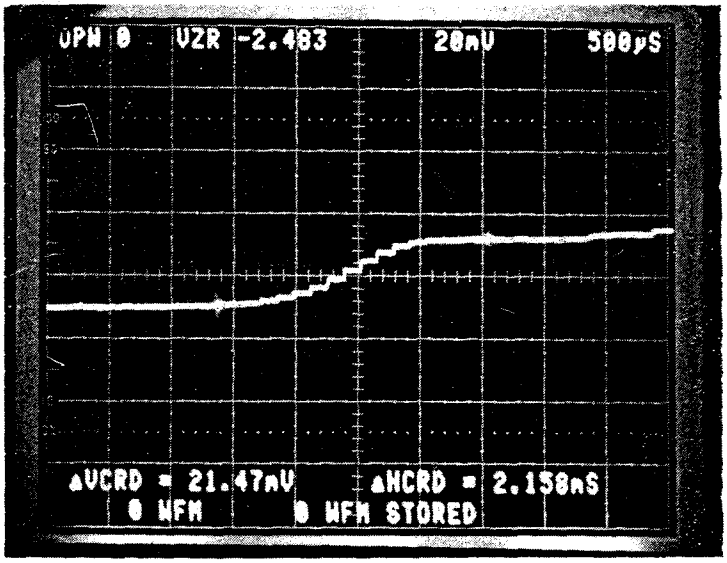


Figure 5-51. Signal lag with unpinned photodiode — 5,000 electrons signal. Run 3C-01.



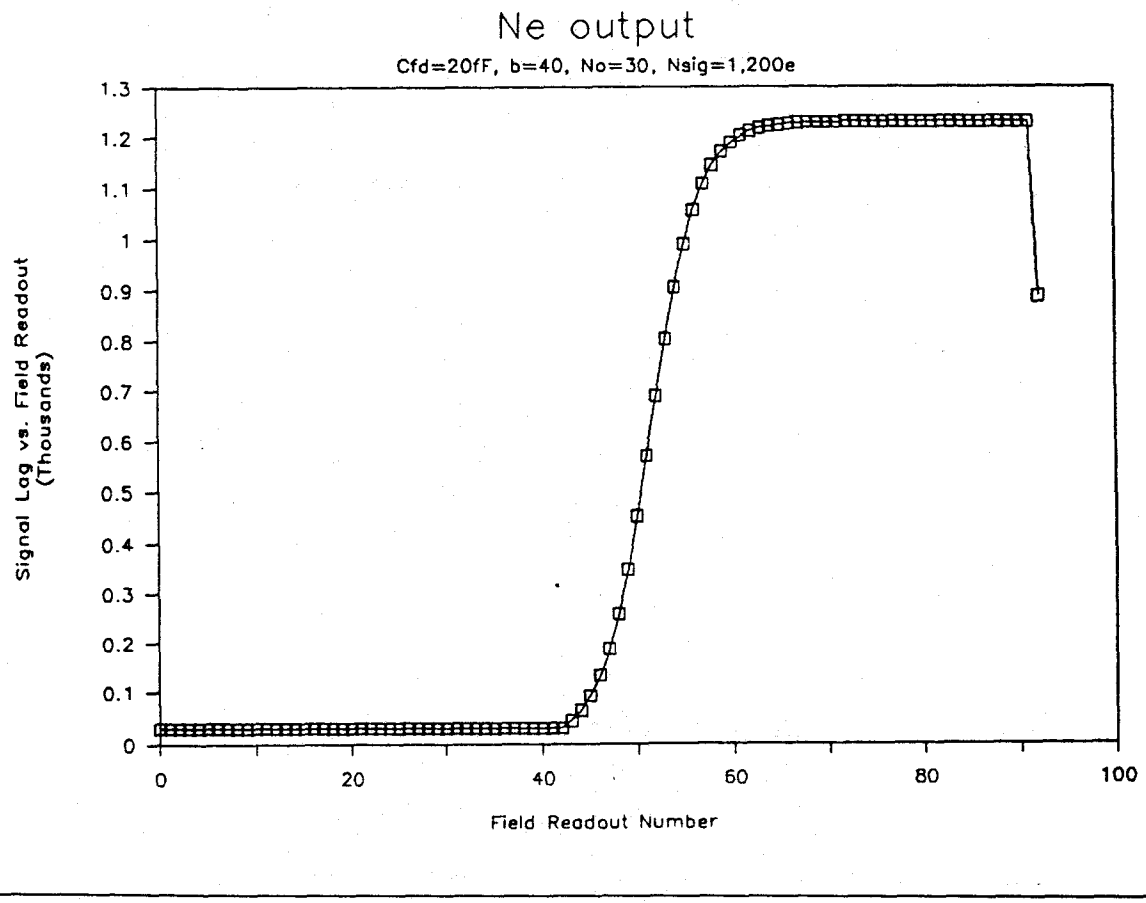


Figure 5-52. Signal lag with unpinned photodiode — 1,200 electrons signal. Run 3C-01

NO IMAGE LAG PHOTODIODE STRUCTURE IN THE INTERLINE CCD IMAGE SENSOR

Nobukazu Teranishi, Akiyoshi Kohono, Yasuo Ishihara, Eiji Oda and Kouichi Arai

Microelectronics Research Laboratories, Nippon Electric Co., Ltd.

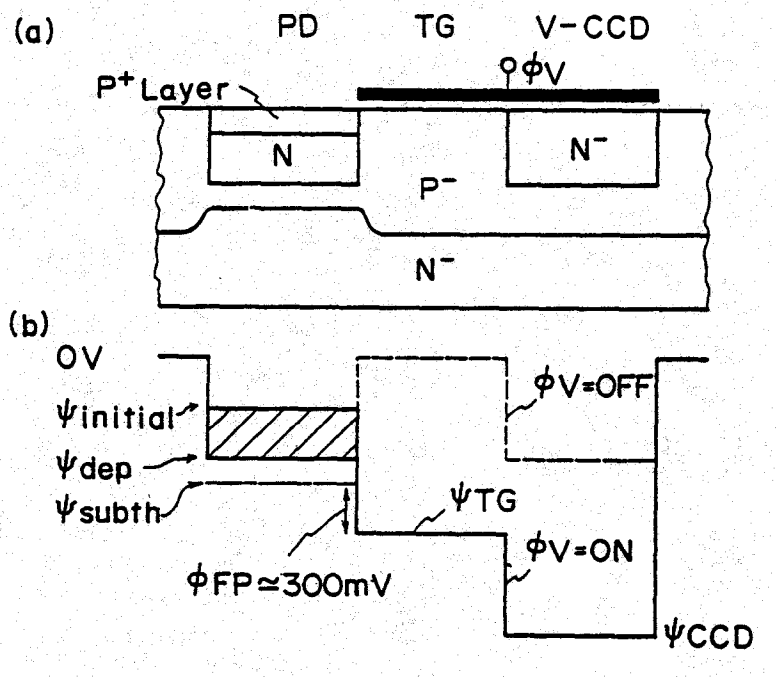
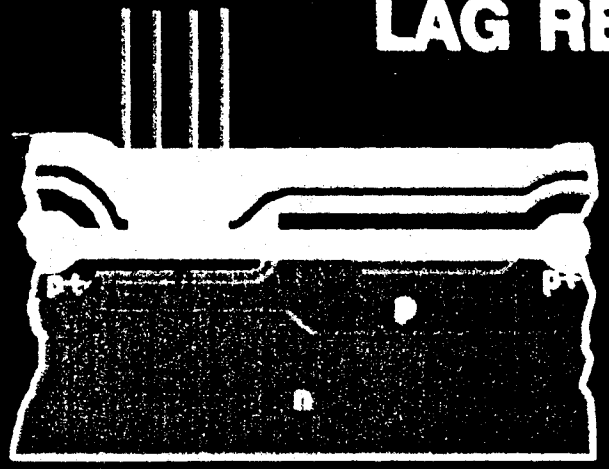


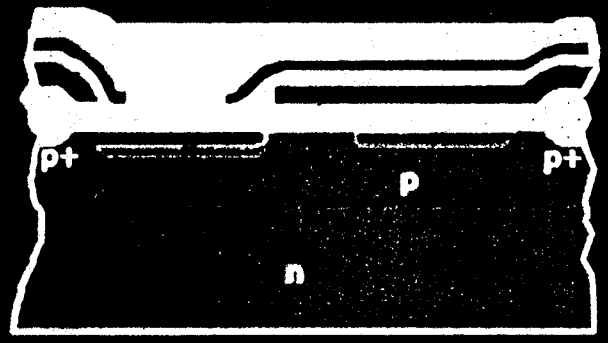
Fig.5. P^+NP^- structure photodiode
(a) Unit cell cross sectional view
(b) Potential profile in a complete transfer mode

IEDM 82

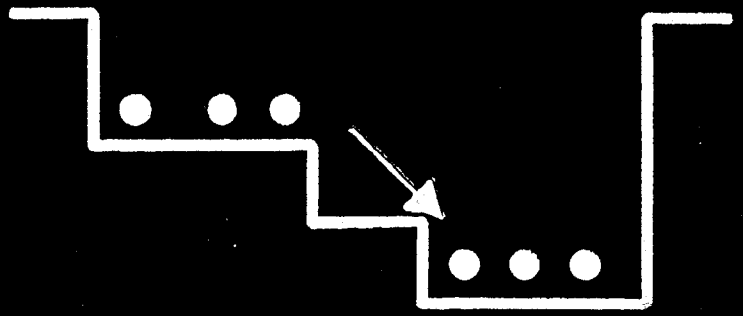
PINNED PHOTODIODE FOR LAG REDUCTION IN CCD's

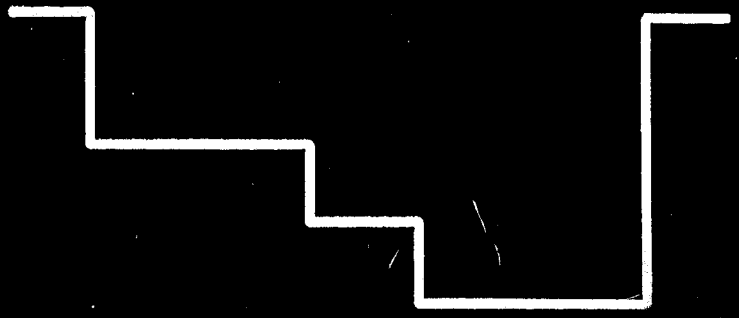


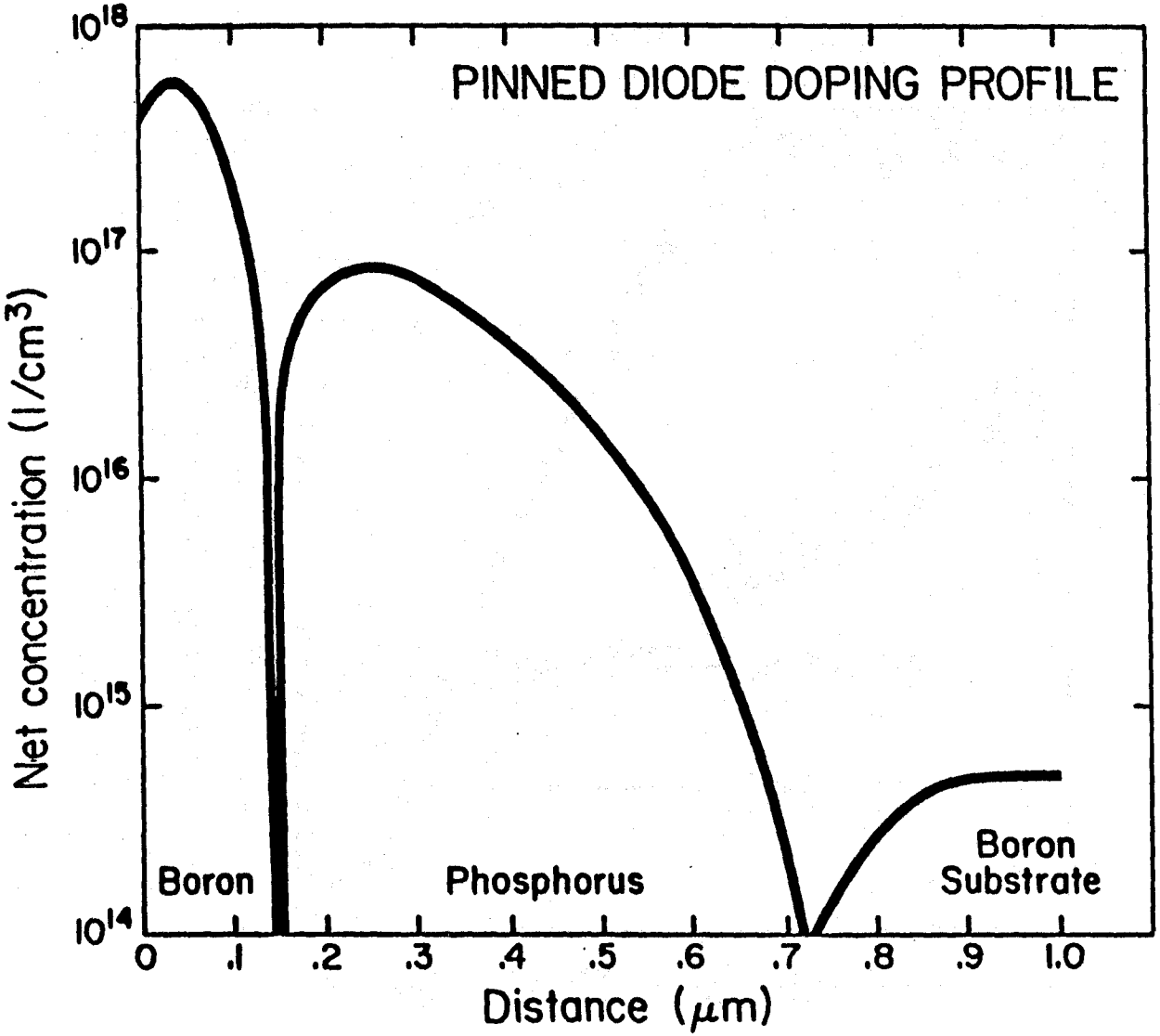
Frame 1

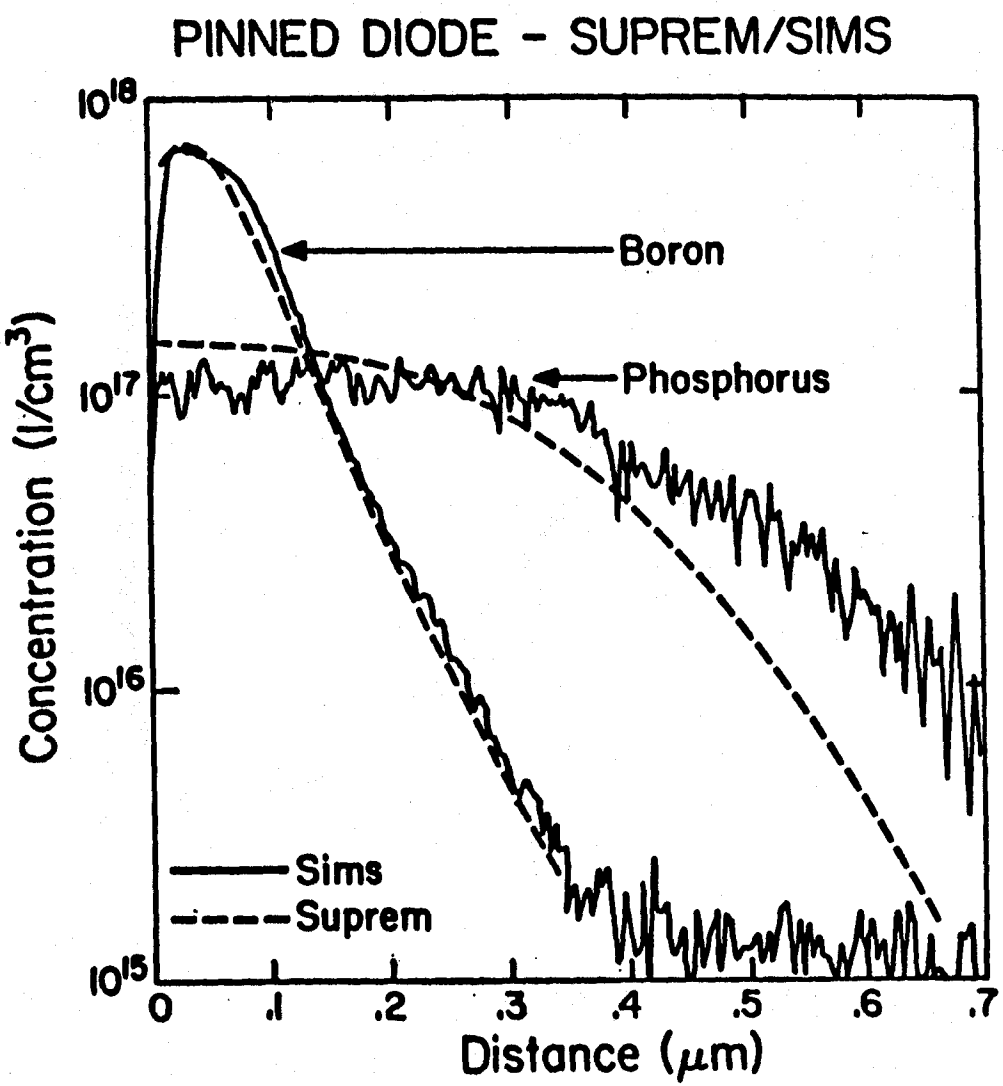


Frame 2

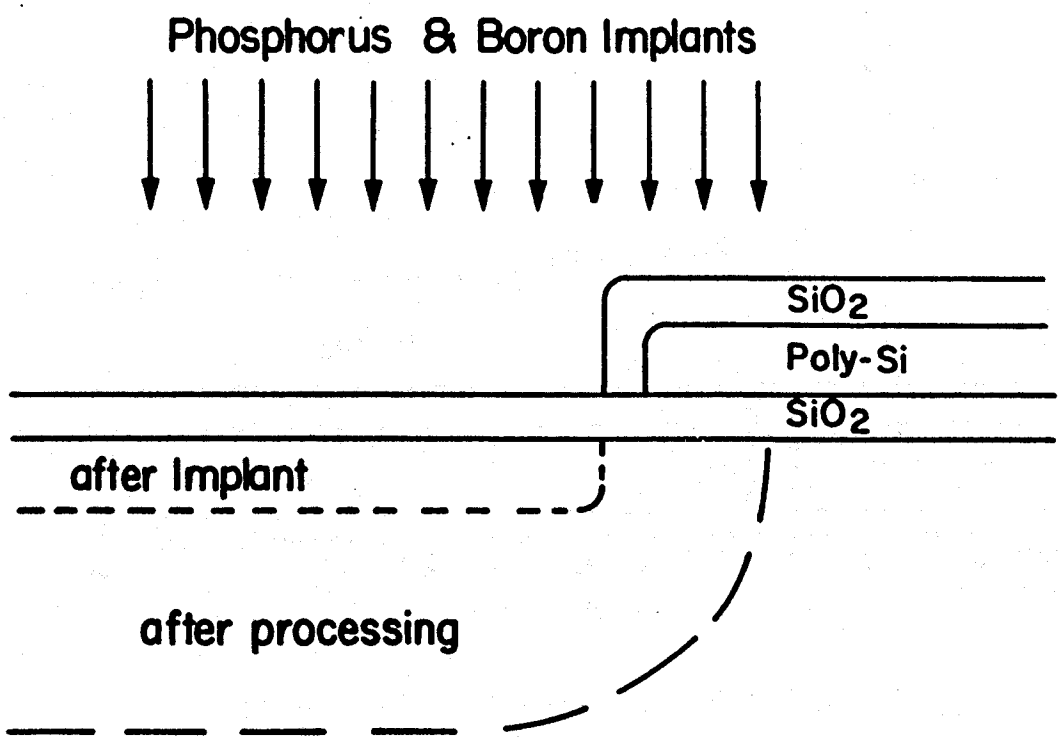




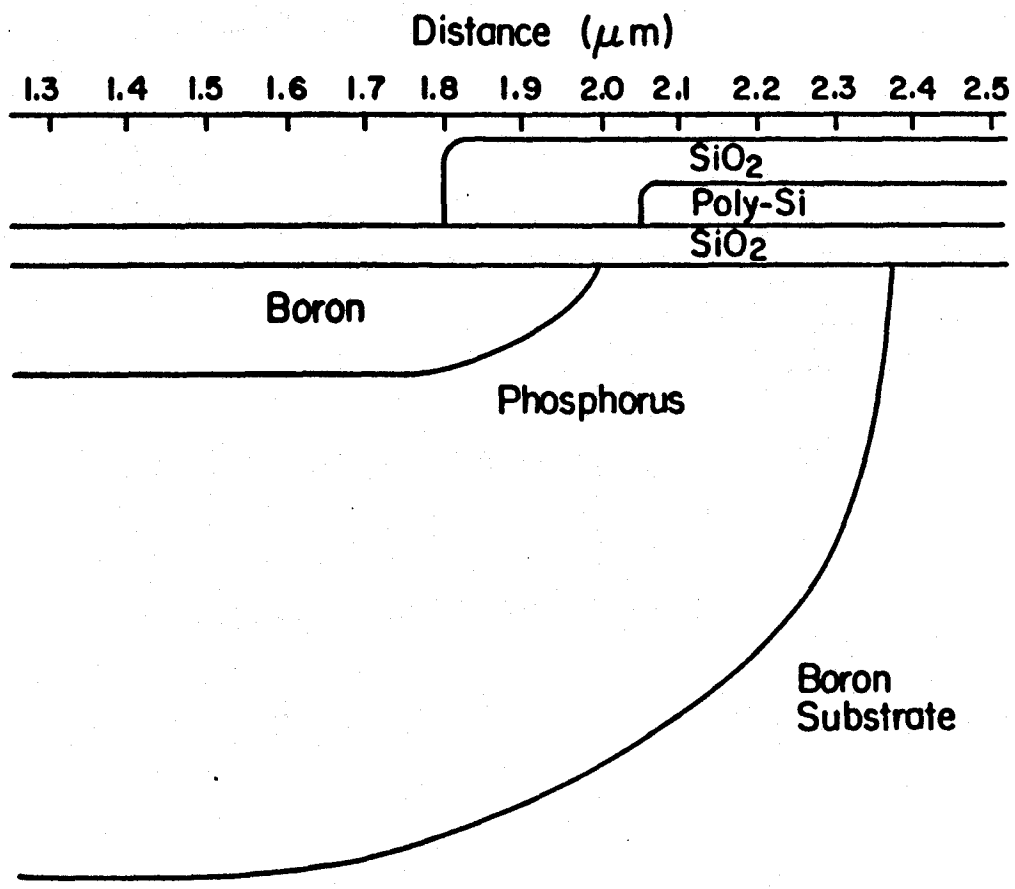

PINNED DIODE DOPING PROFILE
Net concentration (1/cm3)
10^18
10^17
10^16
10^15
10^14
Boron
Phosphorus
Boron
Substrate
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
Distance (μm)


PINNED DIODE - SUPREM/SIMS
Concentration (1/cm³)
10¹⁸
10¹⁷
10¹⁶
10¹⁵
Boron
Phosphorus
Sims
Suprem
0
.1
.2
.3
.4
.5
.6
.7
Distance (μm)

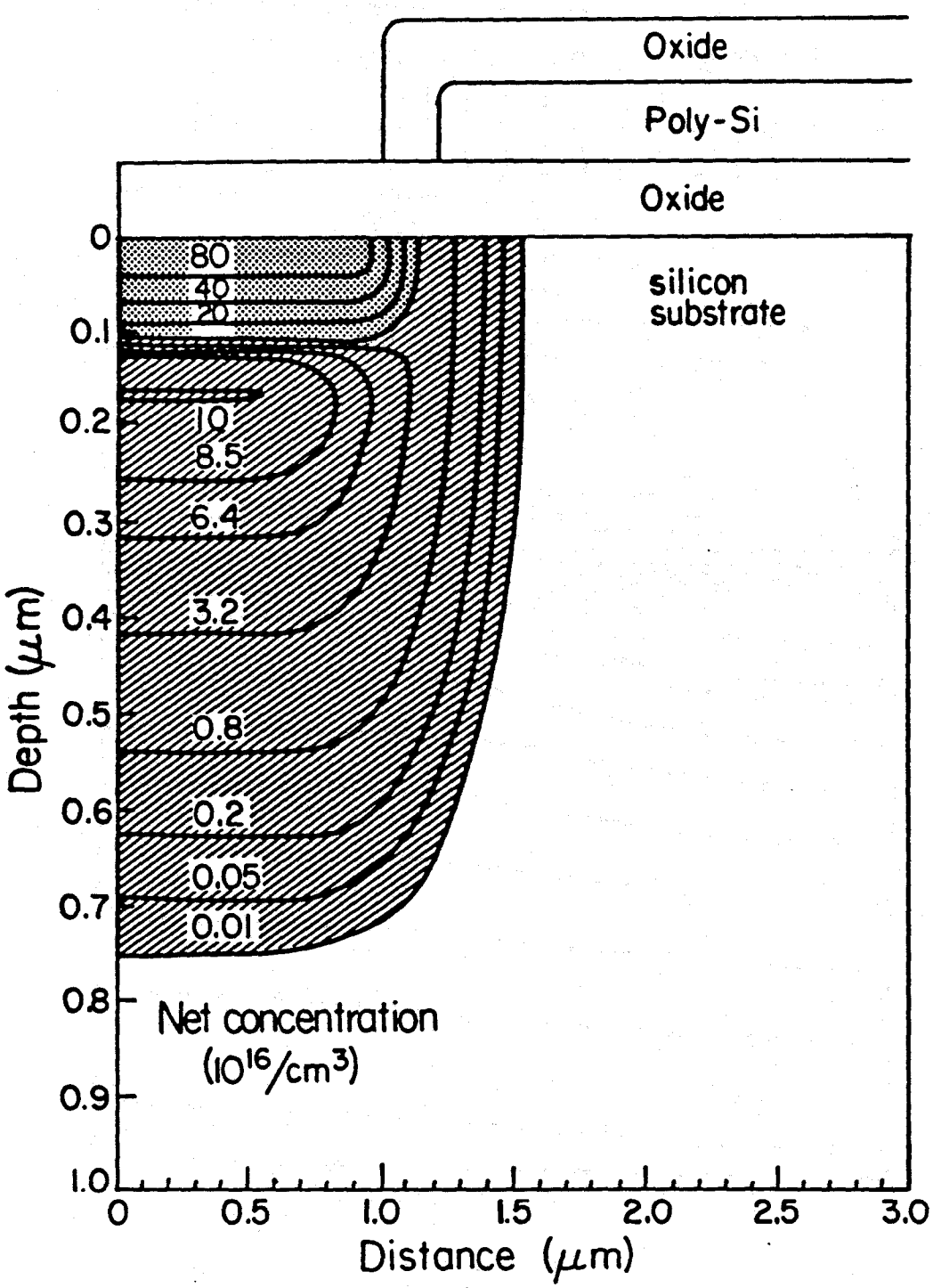
PINNED DIODE -TRANSFER GATE BARRIER



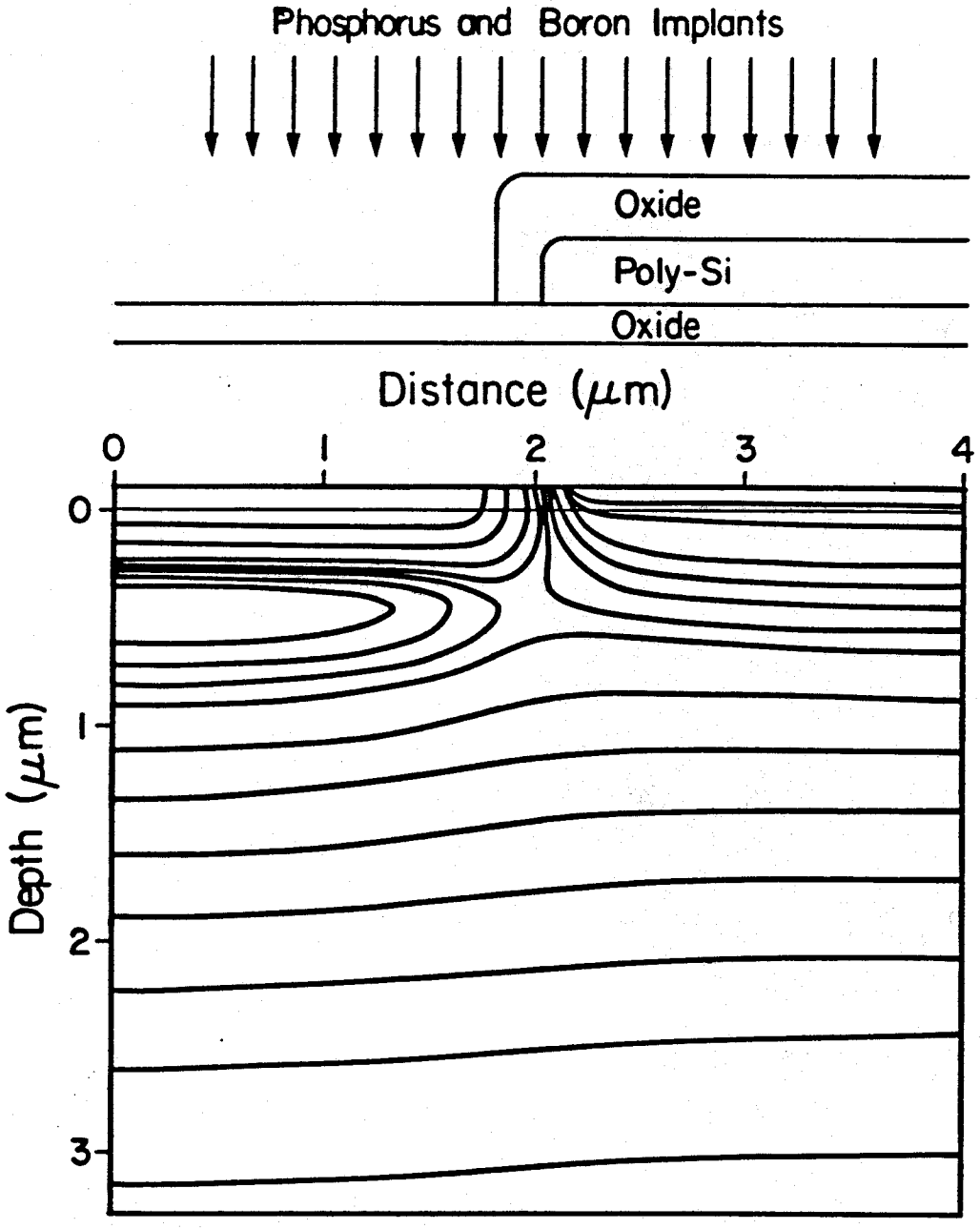
PINNED DIODE - TRANSFER GATE BARRIER



PINNED DIODE DOPING - SUPRA



PINNED DIODE-TRANSFER GATE BARRIER
ELECTROSTATIC POTENTIAL CONTOURS



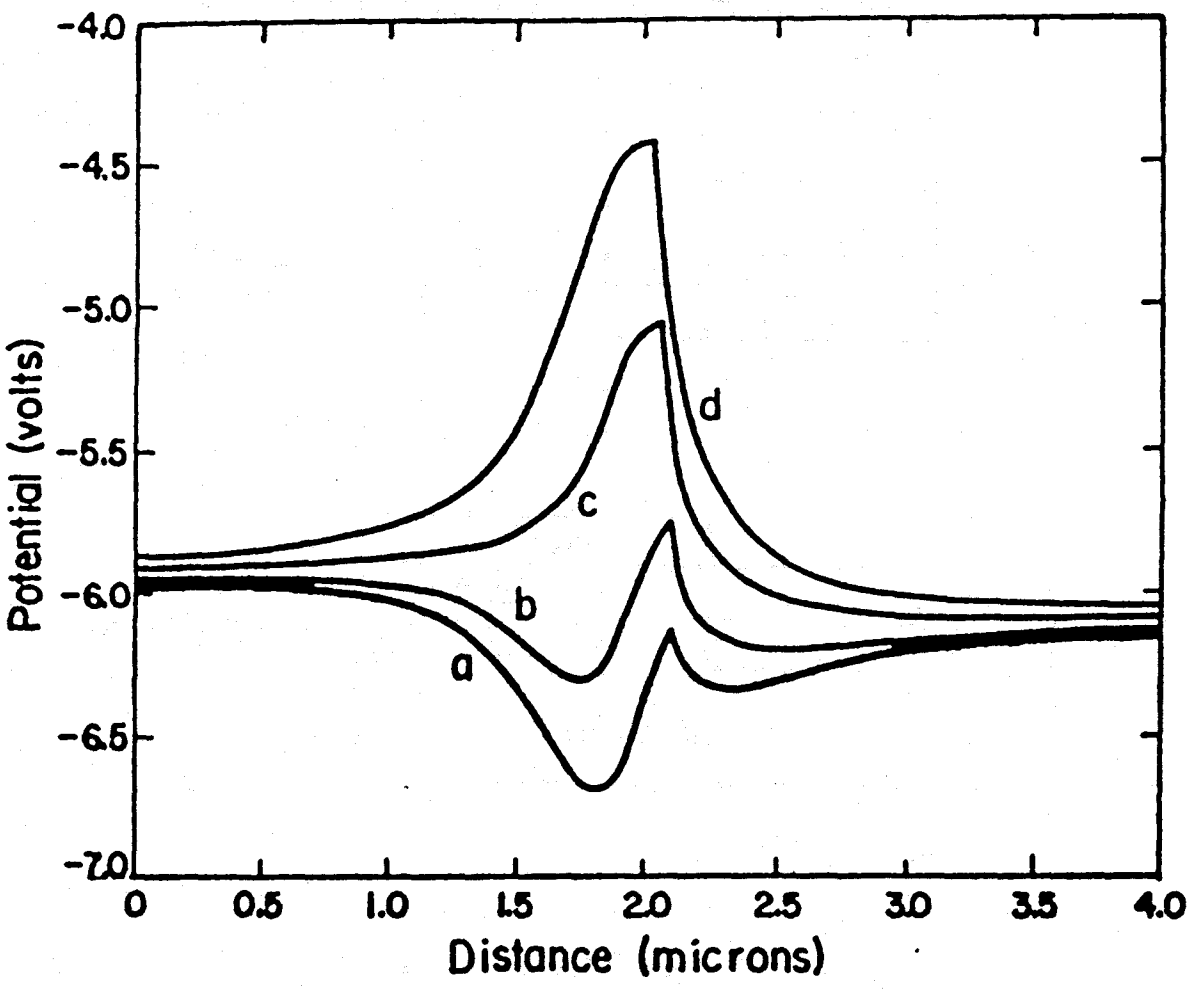
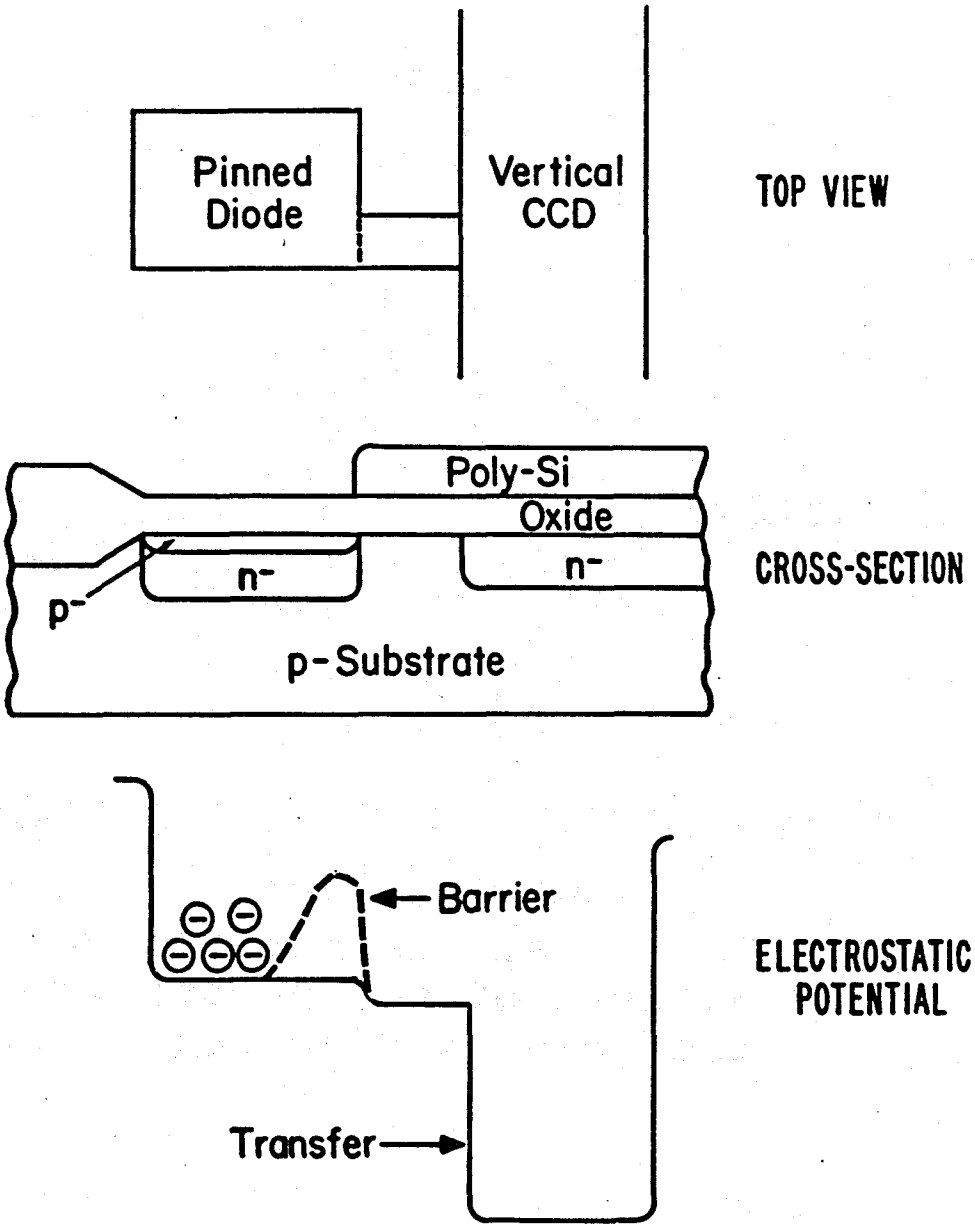
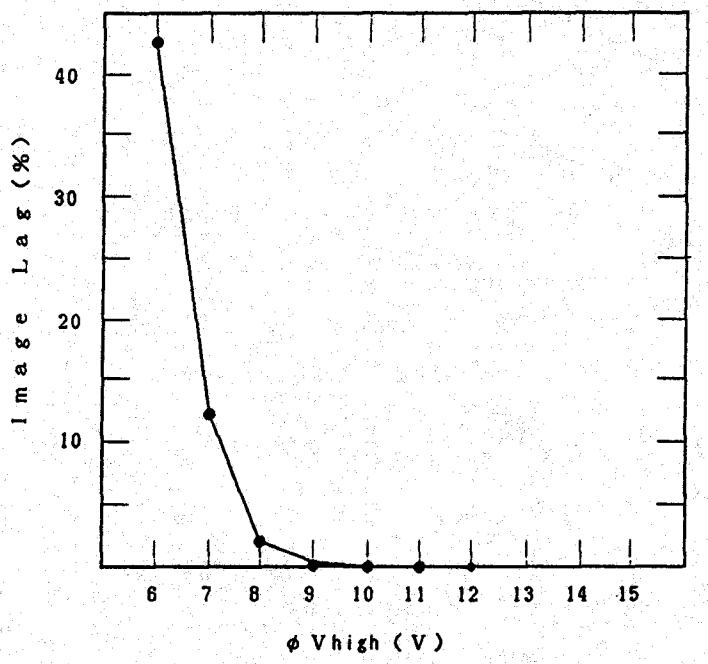


Fig. 11. Potential barrier for various offsets of the phosphorus from the poly-Si transfer gate.

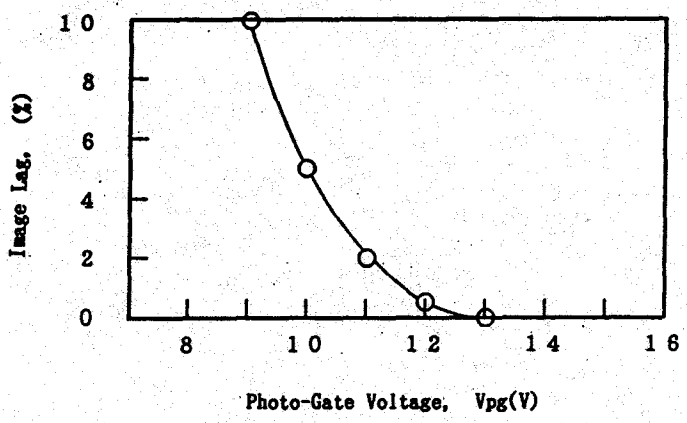
D4-IMAGE CELL ARCHITECTURE





Kuriyama et al

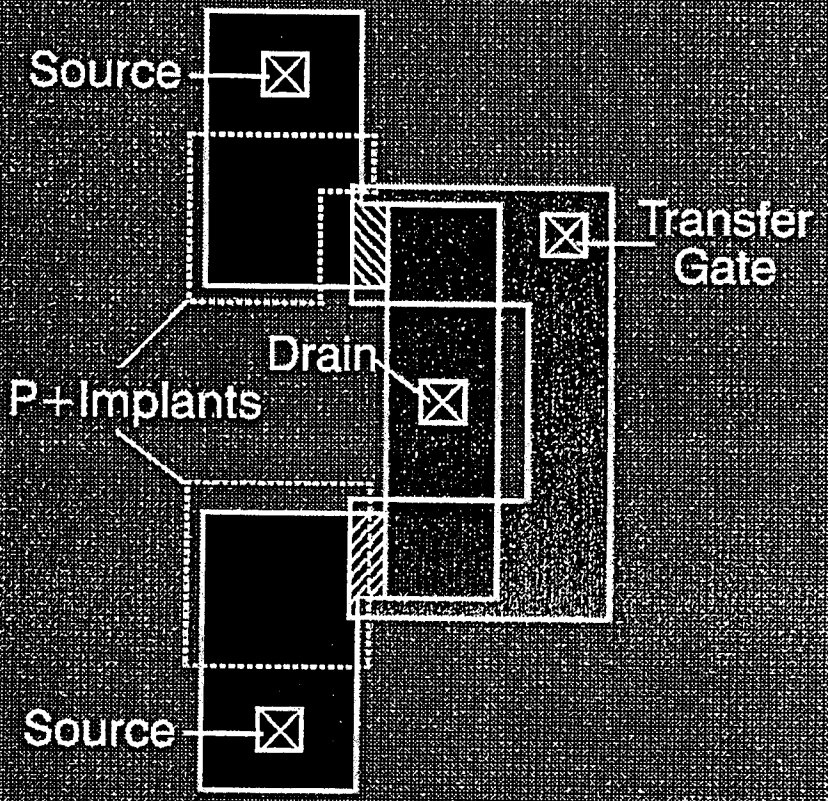
Fig. 12. Image lag as function of the VCCD transfer gate clock pulse amplitude (ϕV high).



Ando et al

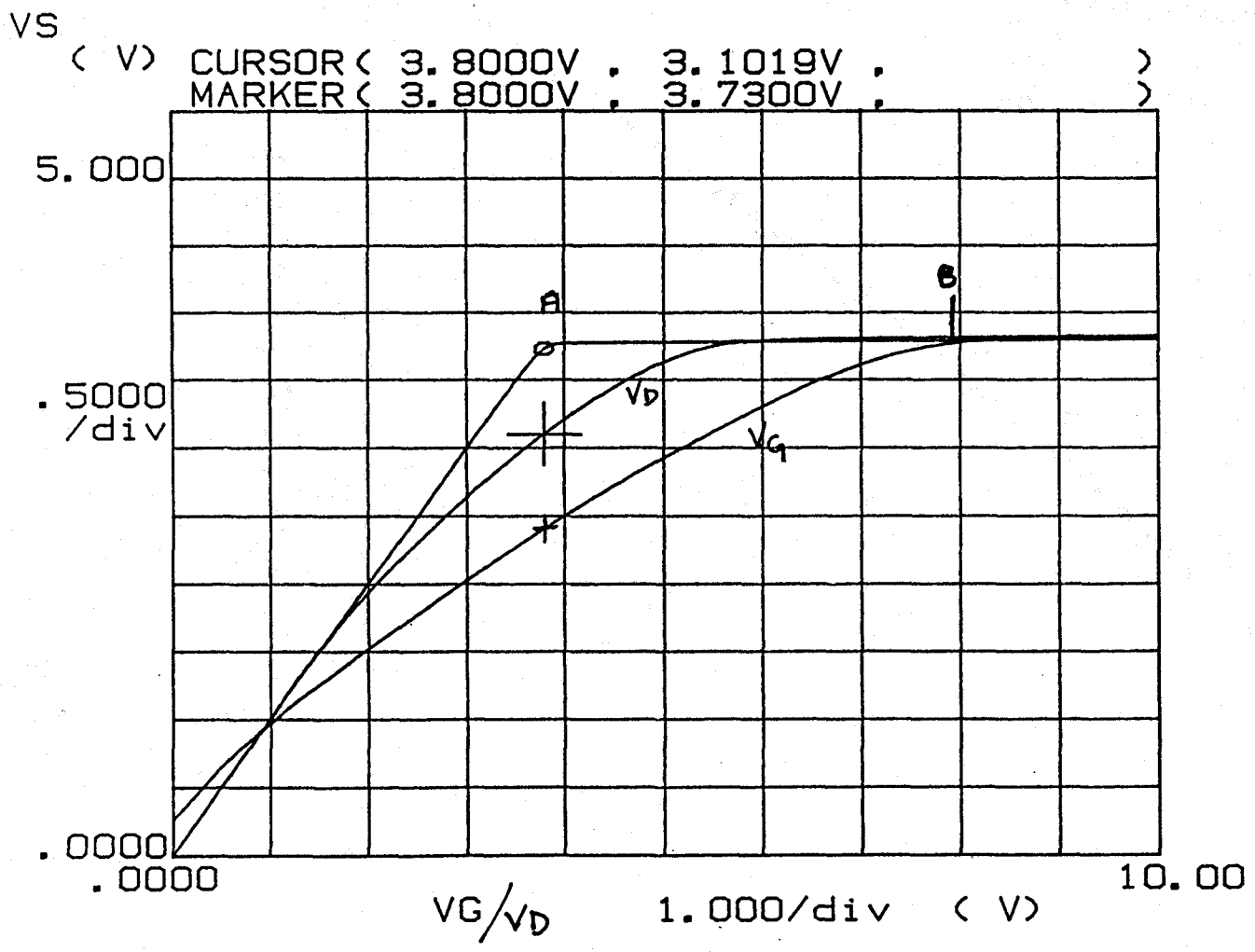
Fig. 10. Image lag characteristics of the device.

PD-TO-VCCD BARRIER TEST STRUCTURE



****** GRAPHICS PLOT ******

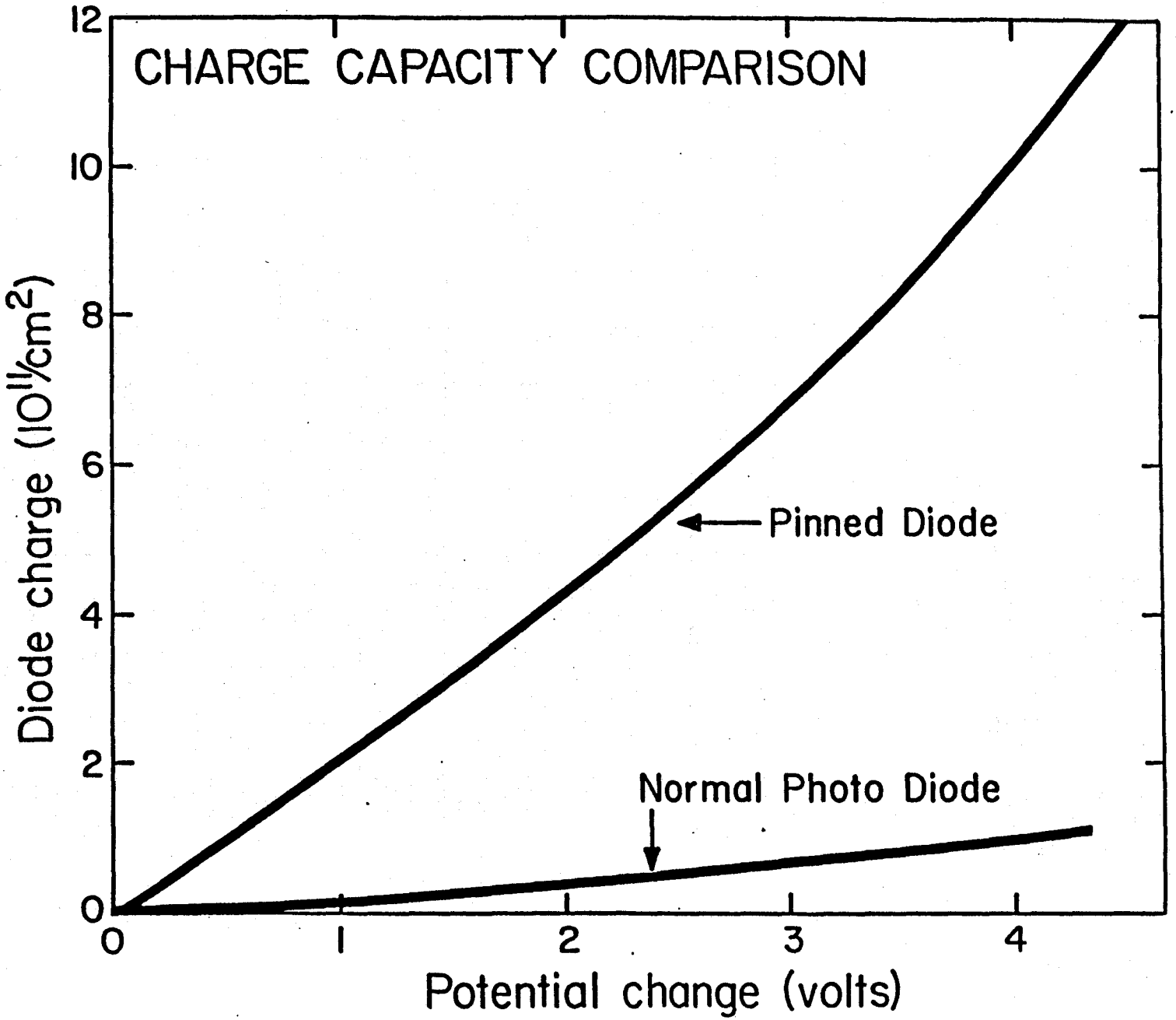
M2 3D77-14 TVOD 2

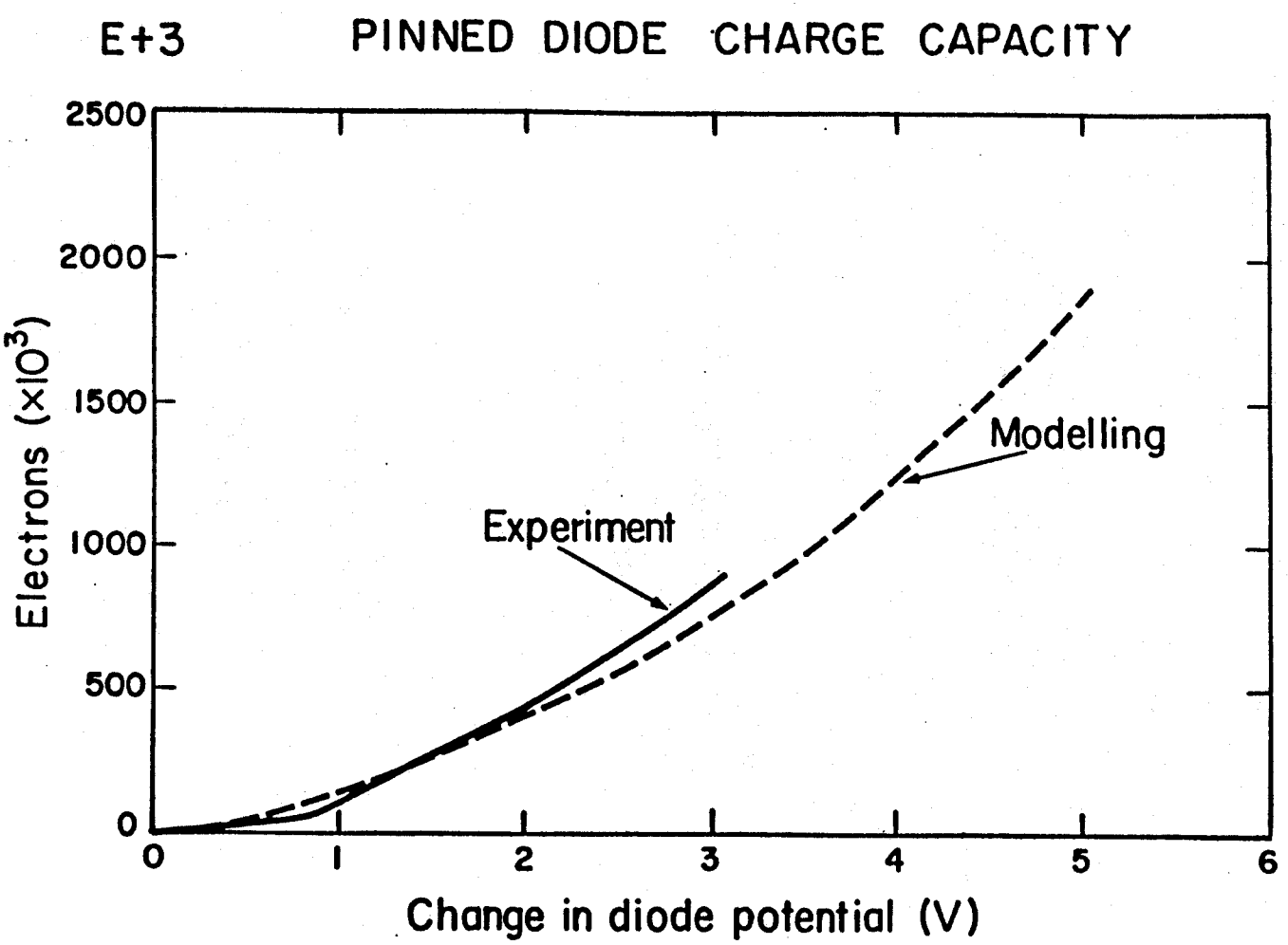


Variable1:
VG -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:

VD	-Ch2	15.000V
IS	-Ch3	-50.00nA
VW	-Ch4	.0000V
VSUB	-Vs1	15.000V
VS2	-Vs2	.0000V


CHARGE CAPACITY COMPARISON
Diode charge (10^{11}/cm^2)
Potential change (volts)
Pinned Diode
Normal Photo Diode
0
2
4
6
8
10
12
0
1
2
3
4


E+3
PINNED DIODE CHARGE CAPACITY
2500
2000
1500
1000
500
0
Electrons (×10³)
Modelling
Experiment
0
1
2
3
4
5
6
Change in diode potential (V)

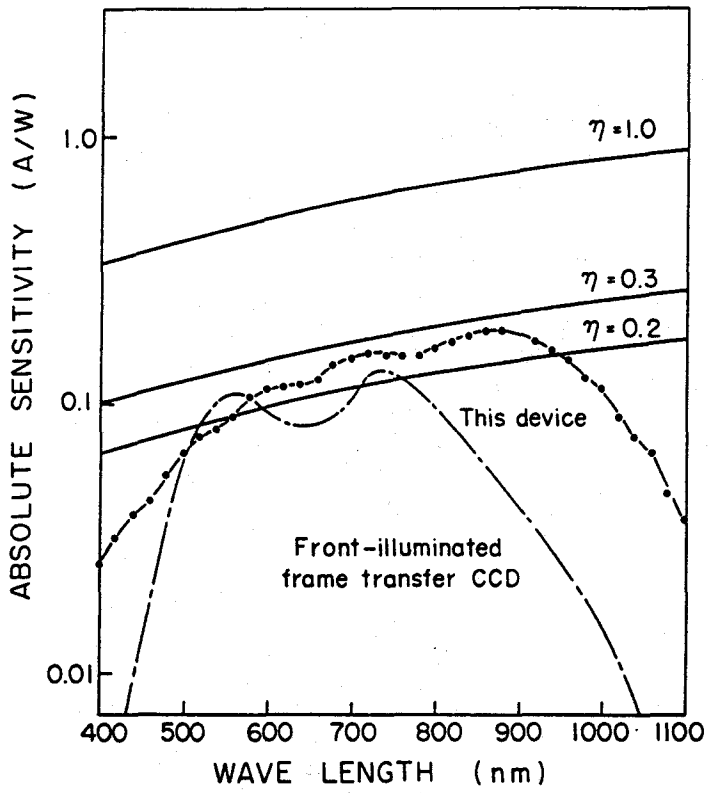
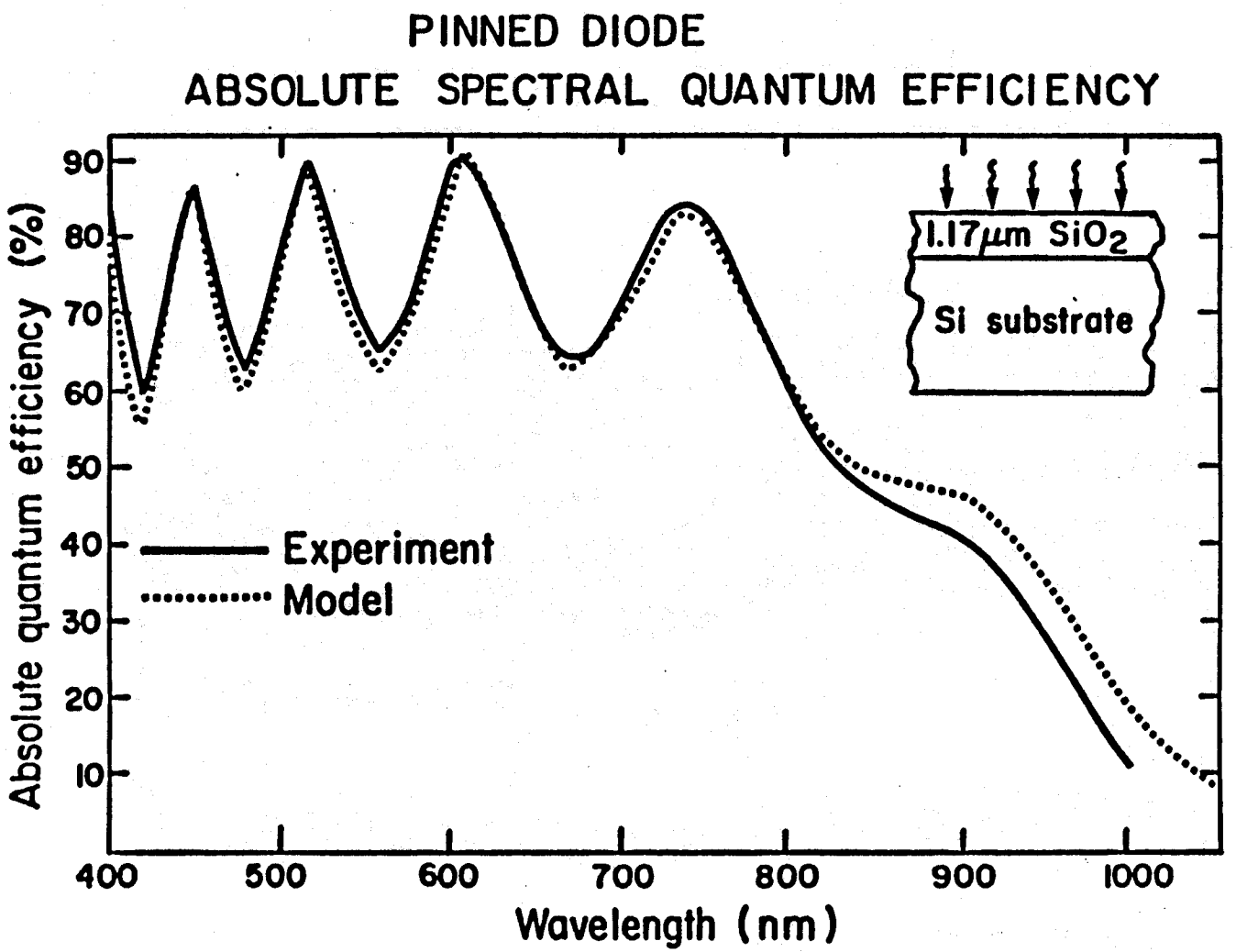


FIGURE 4—Spectral response.

Ishihara et al

ISSCC 80


PINNED DIODE
ABSOLUTE SPECTRAL QUANTUM EFFICIENCY
Absolute quantum efficiency (%)
90
80
70
60
50
40
30
20
10
400
500
600
700
800
900
1000
Wavelength (nm)
Experiment
Model
1.17μm SiO2
Si substrate

S.Manabe, et al.," A 2 Million Pixel CCD Imager Overlaid with an Amorphous Silicon Photoconversion Layer "

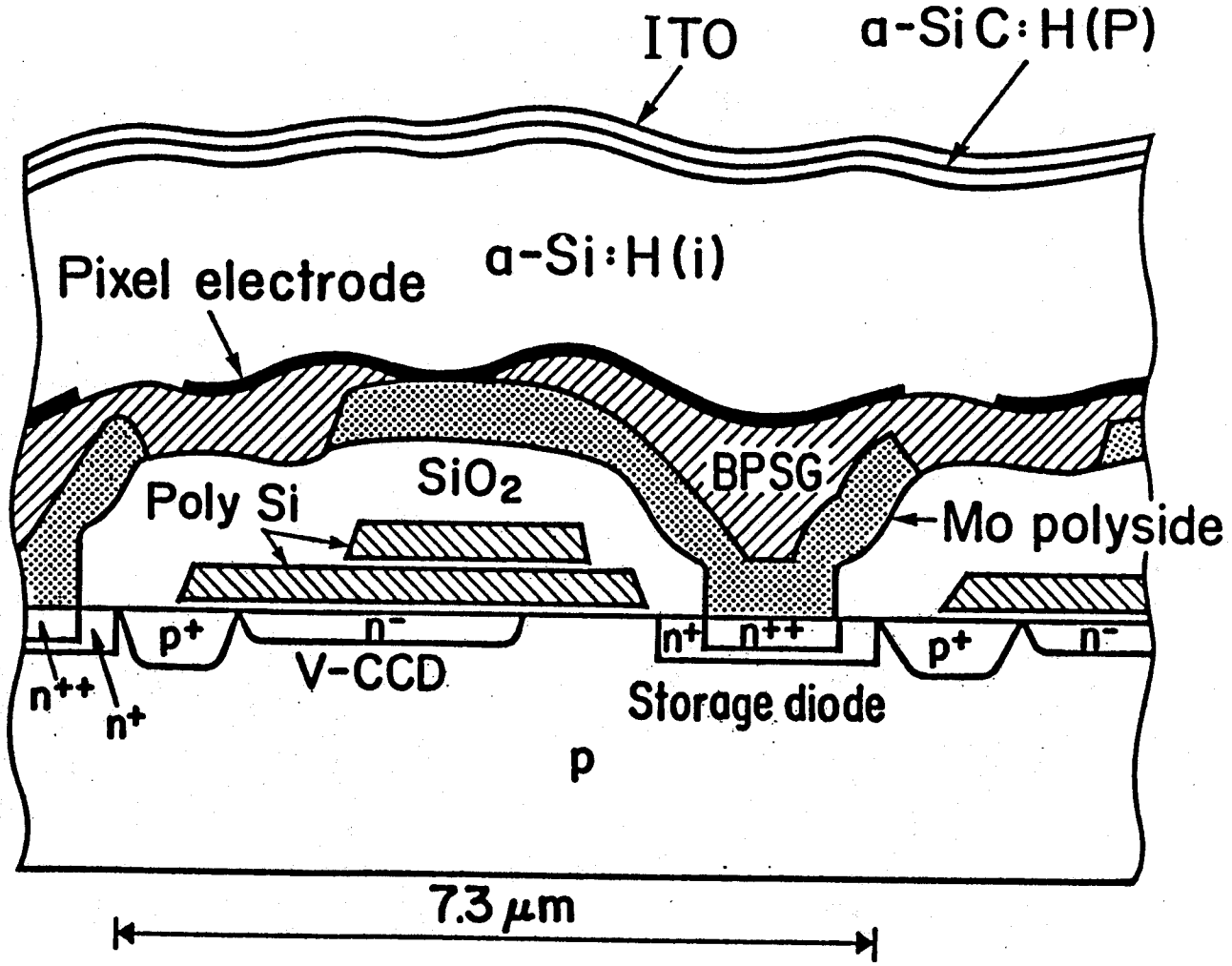
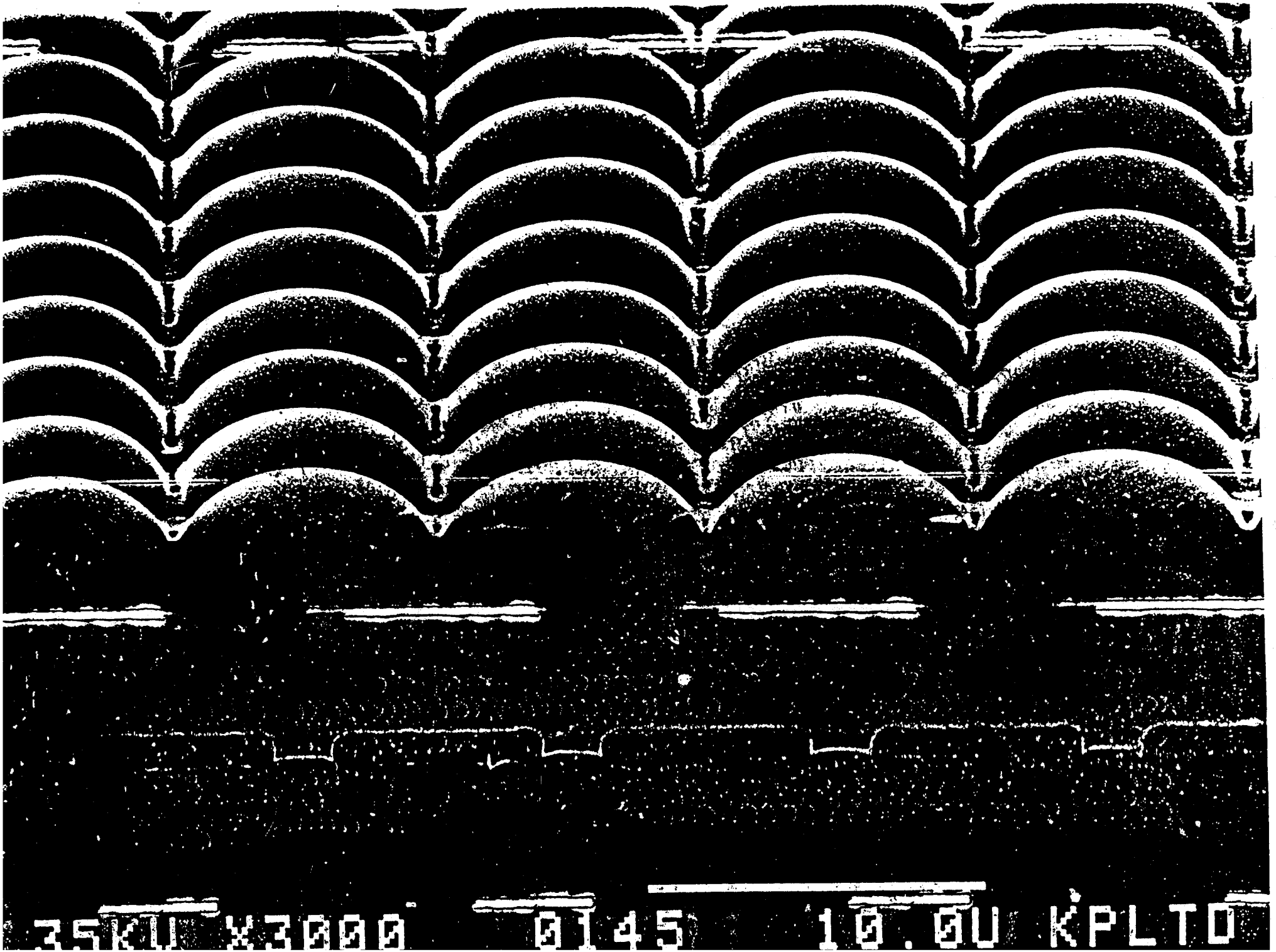
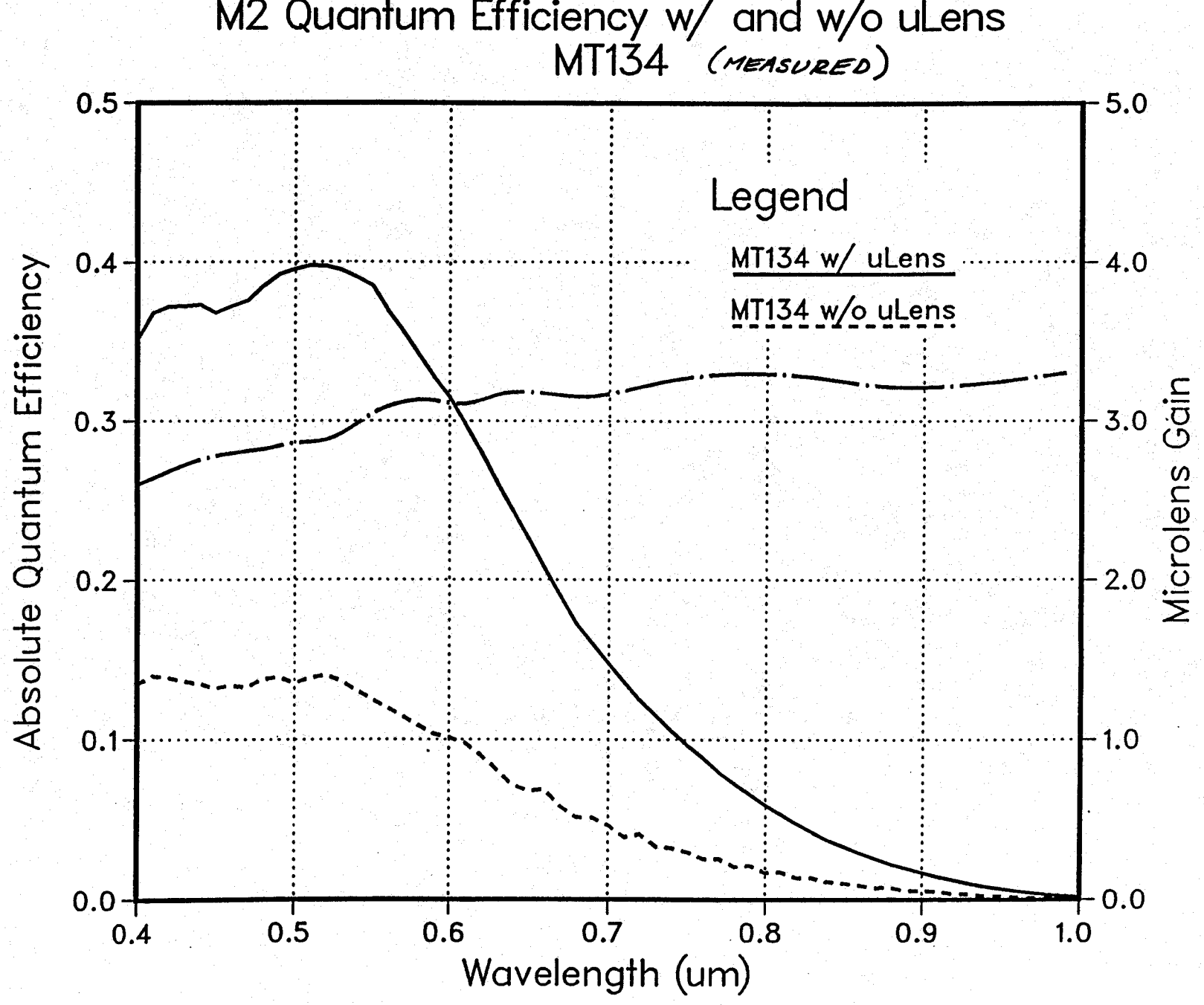
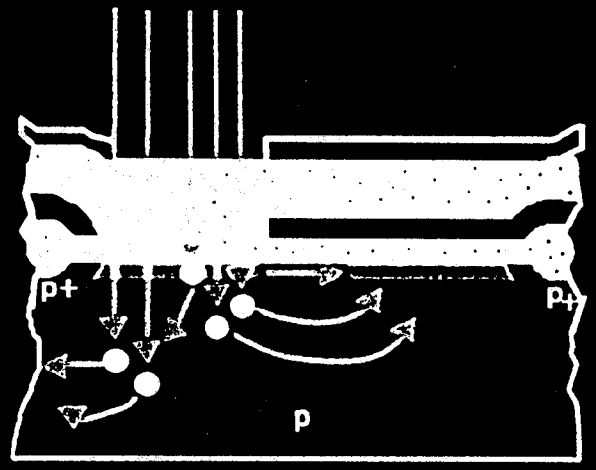


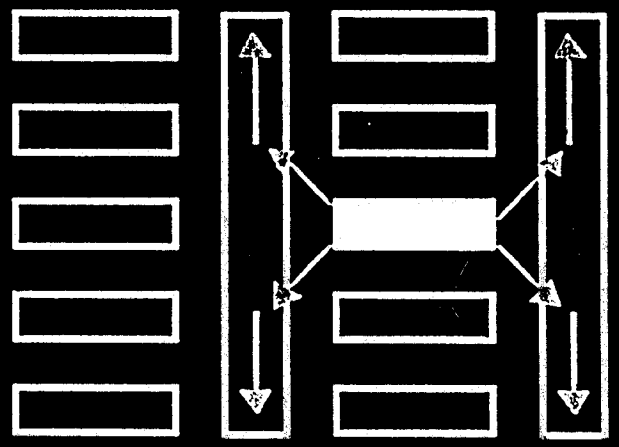
FIGURE 2 Cross section view of unit cell


35KV X3000 0145 10.0U KPLTD


M2 Quantum Efficiency w/ and w/o uLens
MT134 (MEASURED)
Legend
MT134 w/ uLens
MT134 w/o uLens
Absolute Quantum Efficiency
Microlens Gain
Wavelength (um)
0.0
0.1
0.2
0.3
0.4
0.5
1.0
2.0
3.0
4.0
5.0
0.4
0.5
0.6
0.7
0.8
0.9
1.0

BLOOMING IN CCD IMAGE SENSORS

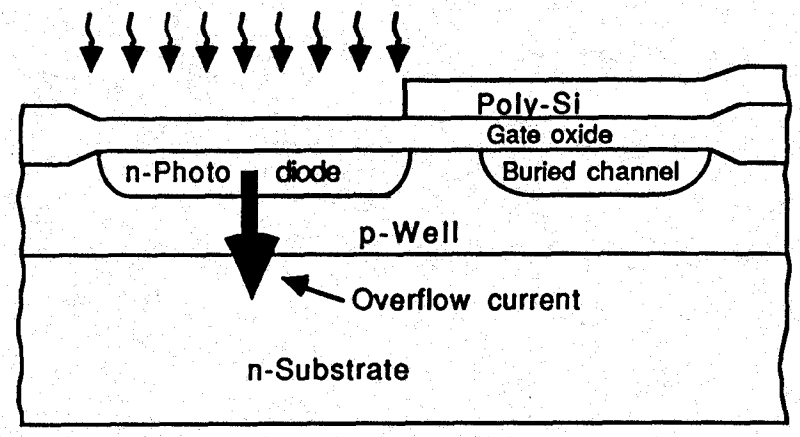




- Illumination Beyond Saturation Causes Overflow Into CCD
- Excess Charge Floods Vertical CCD

ANTIBLOOMING SCHEMES

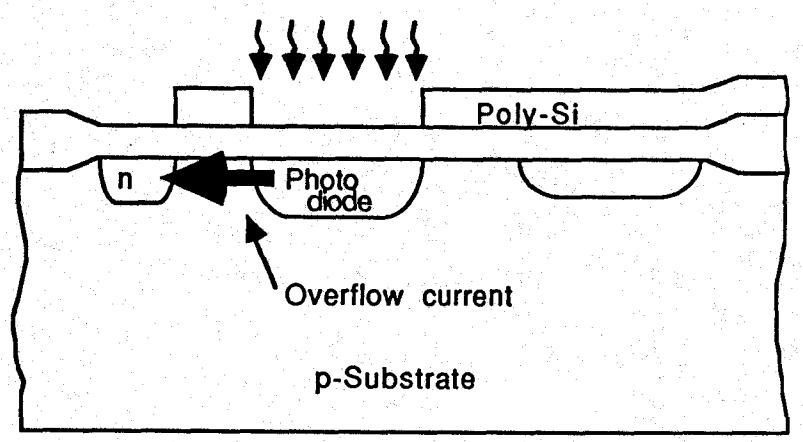
Vertical Overflow Drain (VOD)



Advantages
- Large fill factor
- More scalable
- Less image smear

Disadvantages
- Less red response
- More difficult to make lag free

Lateral Overflow Drain (LOD)



Advantages
- Better red response
- Easier to make lag free

Disadvantages
- Difficult to scale
- Much smaller fill factor
- More image smear

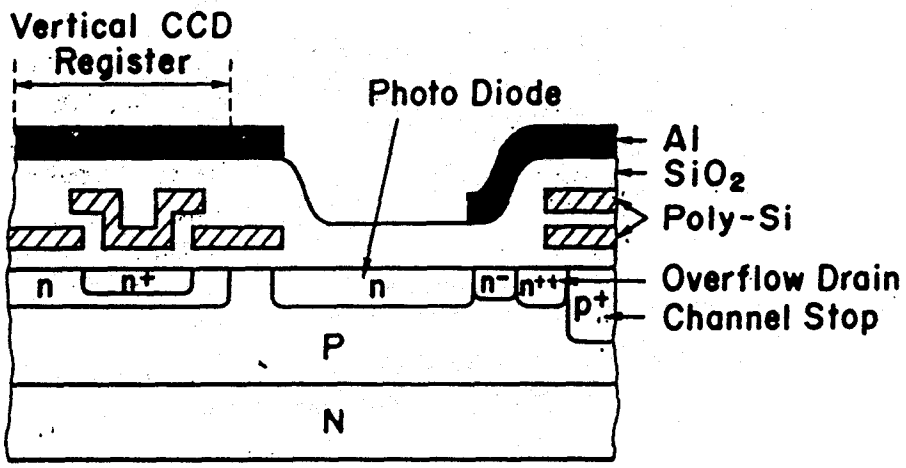


Fig. 3. Picture element cross section.

Furakawa et al

IEDM 1980

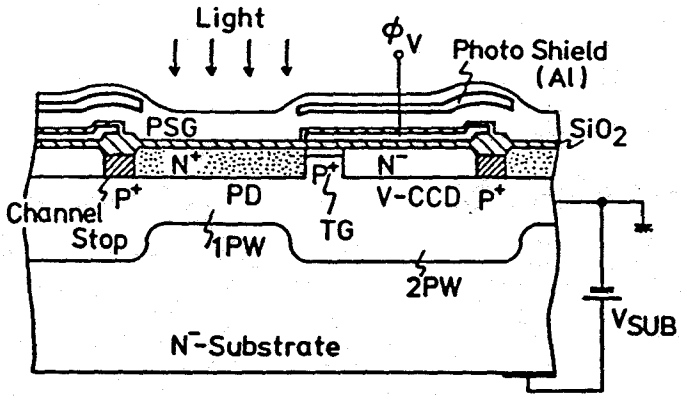


FIGURE 1—Cross sectional view of a unit cell for vertical overflow drain CCD image sensor.

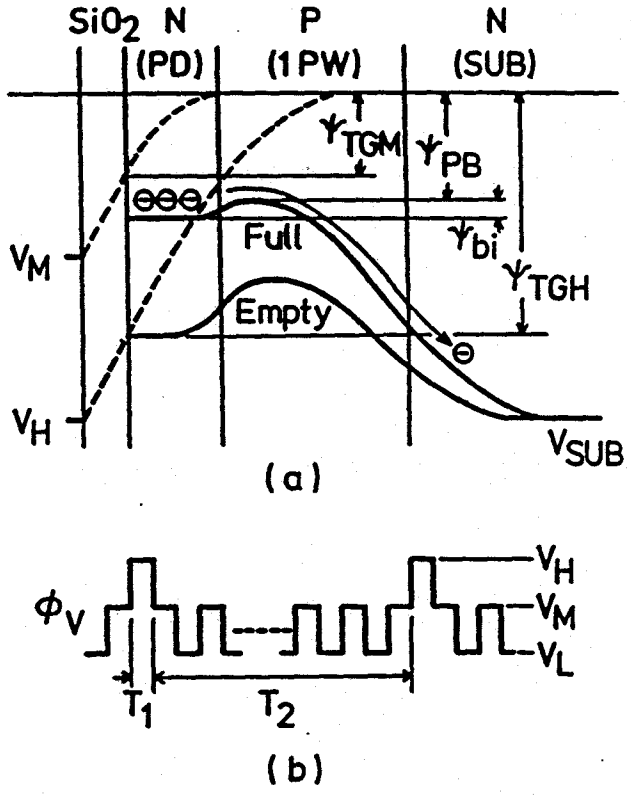
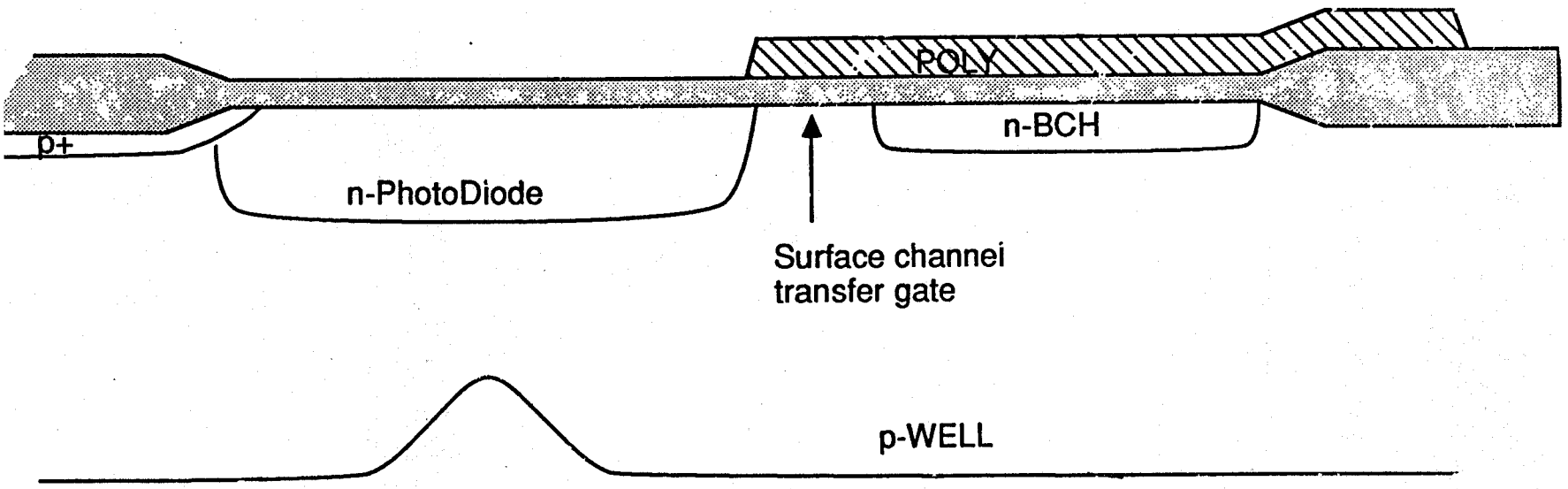


FIGURE 2—(*a*) Potential profiles under the PD and the TG region, and (*b*) one of the V-CCD clock pulses ϕ_V.

Ishihara / NEC

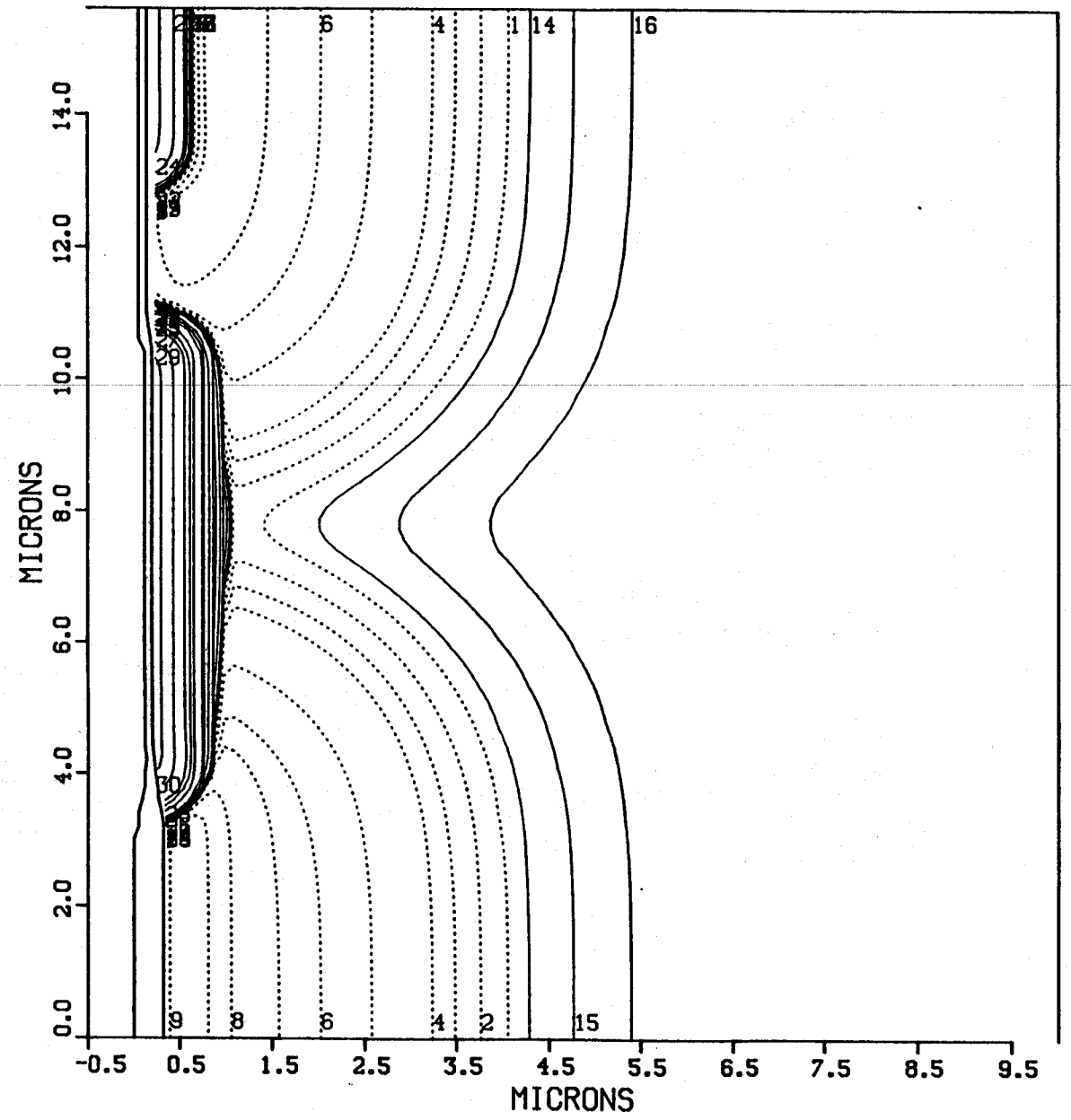
ISSCC 82

IEEE ED-30 84



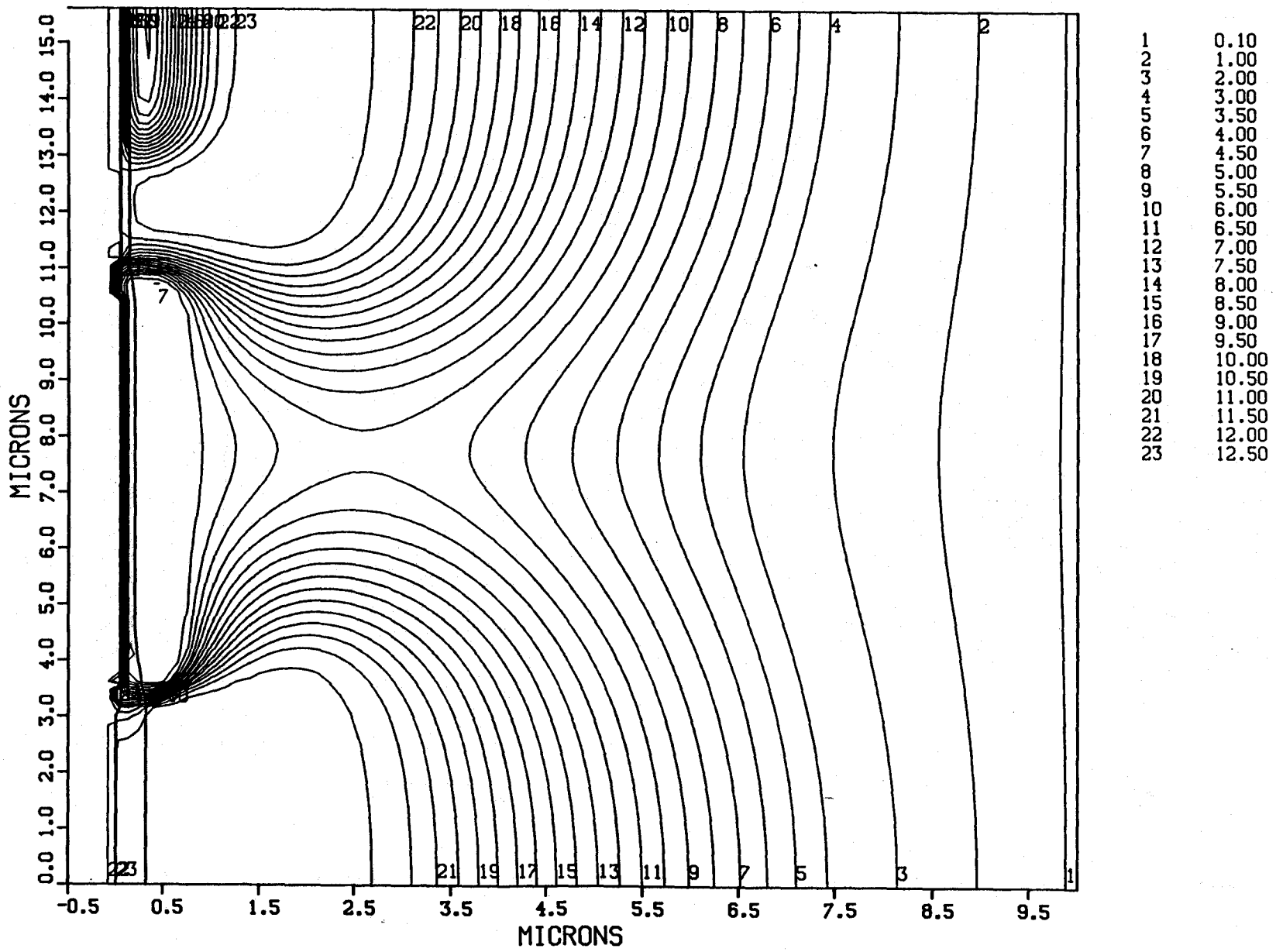
PIXEL CROSS-SECTION OF INTERLINE CCD WITH VOD

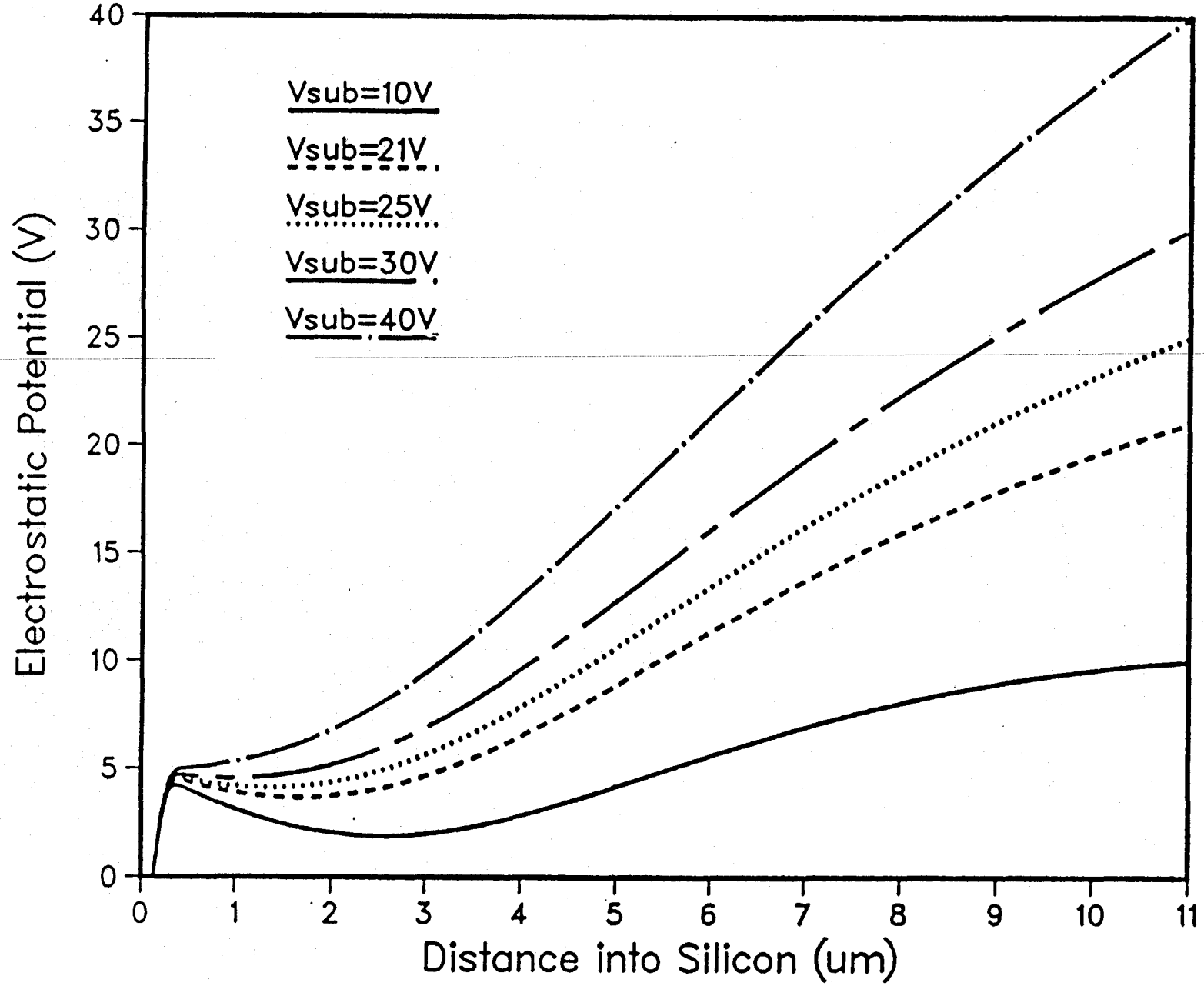
NOMINAL PROCESS

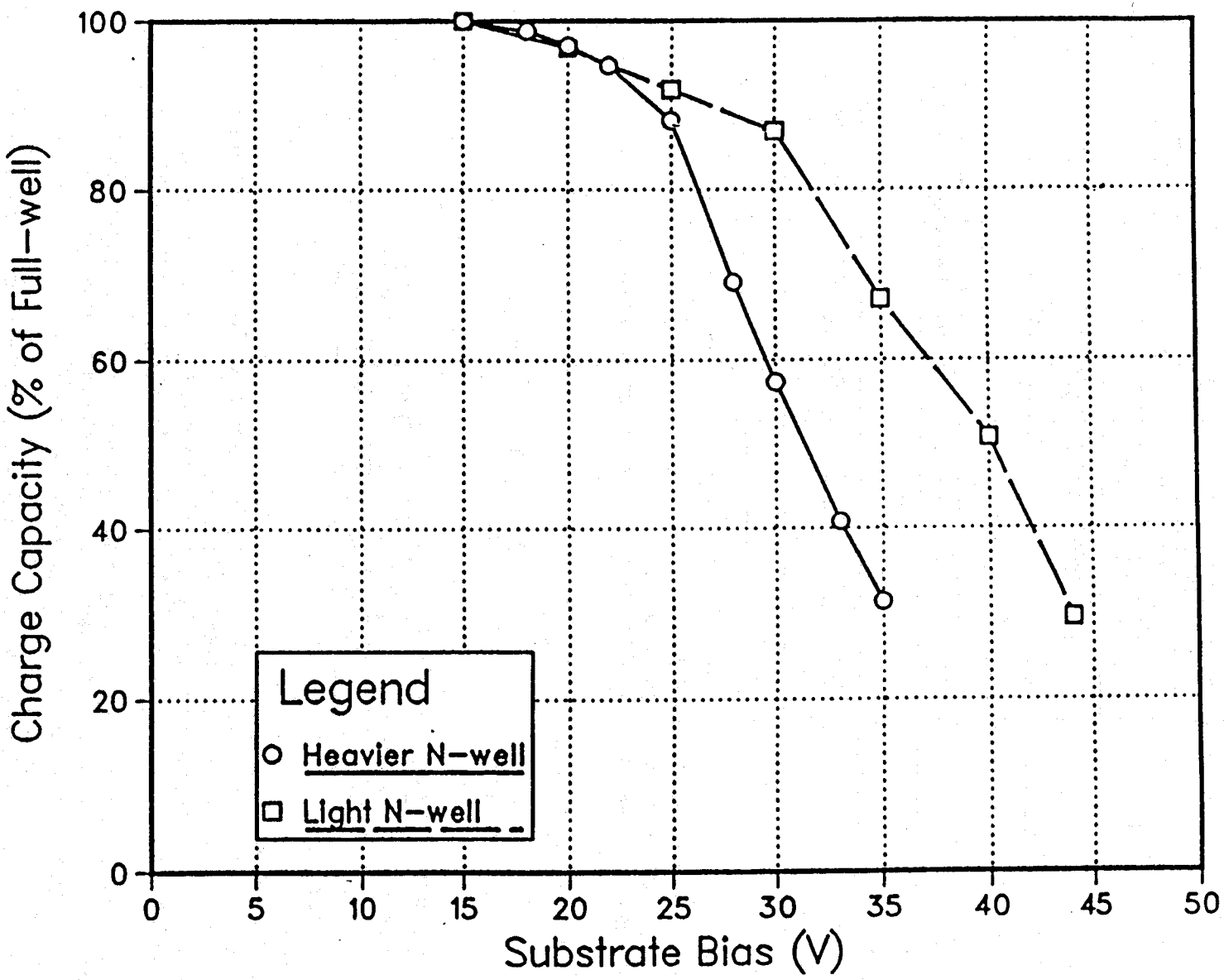


1	-1.00×10^{14}
2	-3.00×10^{14}
3	-6.00×10^{14}
4	-1.00×10^{15}
5	-3.00×10^{15}
6	-6.00×10^{15}
7	-1.00×10^{16}
8	-3.00×10^{16}
9	-6.00×10^{16}
10	-1.00×10^{17}
11	-3.00×10^{17}
12	-6.00×10^{17}
13	-1.00×10^{18}
14	1.00×10^{10}
15	1.00×10^{14}
16	1.40×10^{14}
17	3.00×10^{14}
18	6.00×10^{14}
19	1.00×10^{15}
20	3.00×10^{15}
21	6.00×10^{15}
22	1.00×10^{16}
23	3.00×10^{16}
24	6.00×10^{16}
25	1.00×10^{17}
26	3.00×10^{17}
27	6.00×10^{17}
28	1.00×10^{18}
29	3.00×10^{18}
30	6.00×10^{18}
31	1.00×10^{19}

VG-12,VS-12,VD-12,VTL-5 ,VTR--5, 9/3/86




Vsub=10V
Vsub=21V
Vsub=25V
Vsub=30V
Vsub=40V
Electrostatic Potential (V)
Distance into Silicon (um)
0
5
10
15
20
25
30
35
40
0
1
2
3
4
5
6
7
8
9
10
11



Measured charge capacity versus substrate bias.

Conditions

Item	Symbol	Min.	Typ.	Max	Unit	Remarks
ly voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	Vss	Ground with a 390 Ω resistance				±5 %
trate voltage adjustable range	V_{SUB}	9		19	V	Note 2
ılation range after substrate ge adjustment	V_{SUB}	-3		3	%	
ction transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

aracteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
ut circuit current	I_{DD}		5.0		mA	Note 3
current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

1. V_{PD} and V_{DD} must have the same voltage.
2. Indication of the substrate voltage (V_{SUB}) set value:
   The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

   V_{SUB} code – Two digit indication

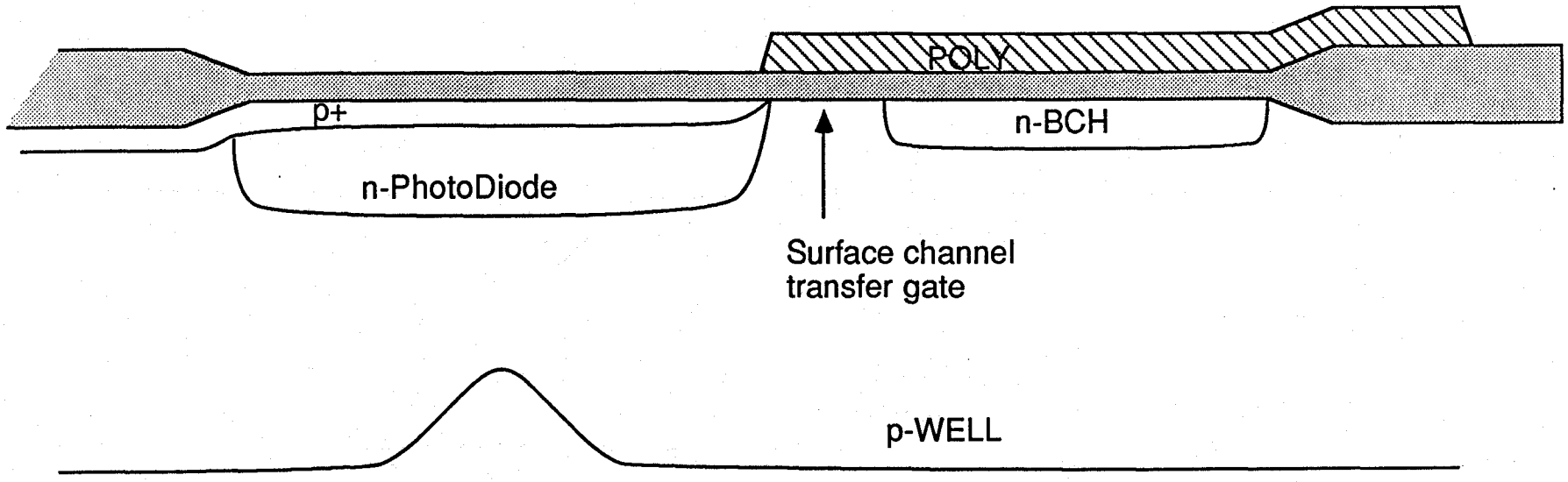
   □ □
   ↑ ↑
   Integral part Decimal part

   The integral codes correspond to the following actual values:

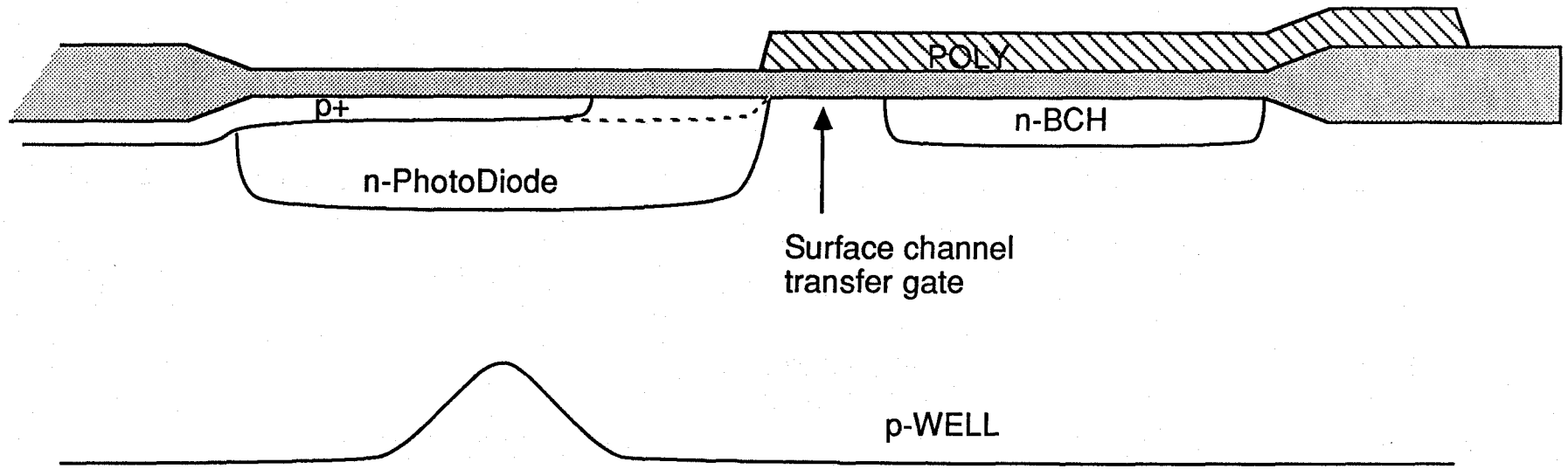
Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

   EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, Vss and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.



PIXEL CROSS-SECTION OF INTERLINE CCD WITH VOD



PIXEL CROSS-SECTION OF
INTERLINE CCD WITH VOD

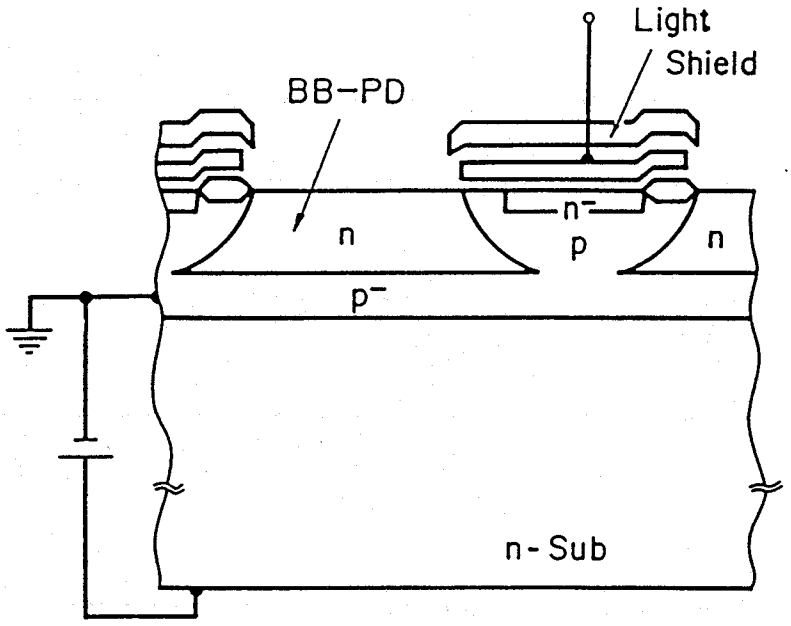
WPM 9.1: **A Smear-Suppressing CCD Imager**

Takao Kuroda, Toshihiro Kuriyama, Yuji Matsuda, Toshiyuki Kozono, Shigenori Matsumoto,

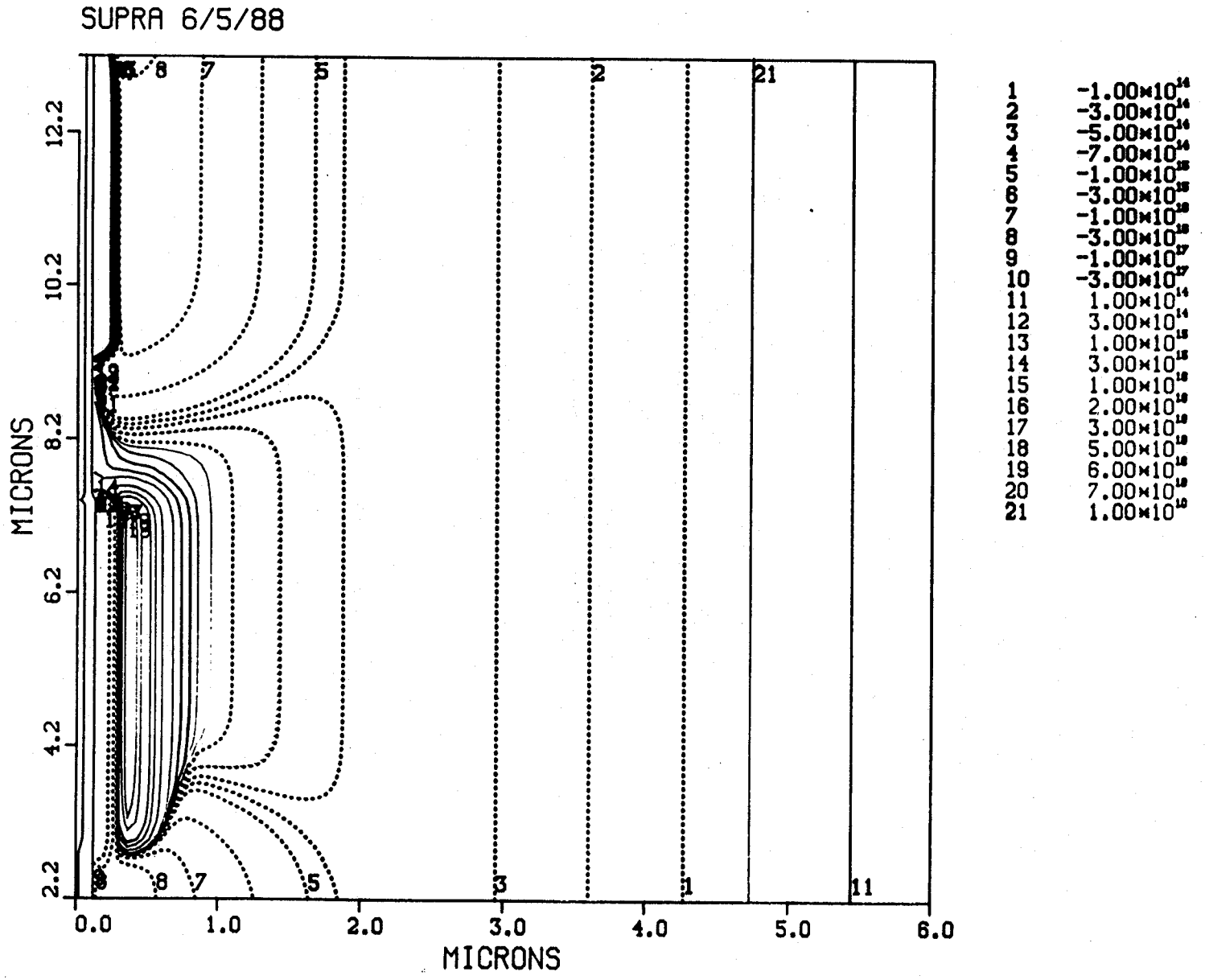
Yoshimitsu Hiroshima, Kenji Horii

Masushita Semiconductor Laboratory

Osaka, Japan



ISSCC 86


SUPRA 6/5/88
MICRONS
12.2
10.2
8.2
6.2
4.2
2.2
0.0
1.0
2.0
3.0
4.0
5.0
6.0
MICRONS
1 -1.00×10^14
2 -3.00×10^14
3 -5.00×10^14
4 -7.00×10^14
5 -1.00×10^15
6 -3.00×10^15
7 -1.00×10^16
8 -3.00×10^16
9 -1.00×10^17
10 -3.00×10^17
11 1.00×10^14
12 3.00×10^14
13 1.00×10^15
14 3.00×10^15
15 1.00×10^16
16 2.00×10^16
17 3.00×10^16
18 5.00×10^16
19 6.00×10^16
20 7.00×10^16
21 1.00×10^17

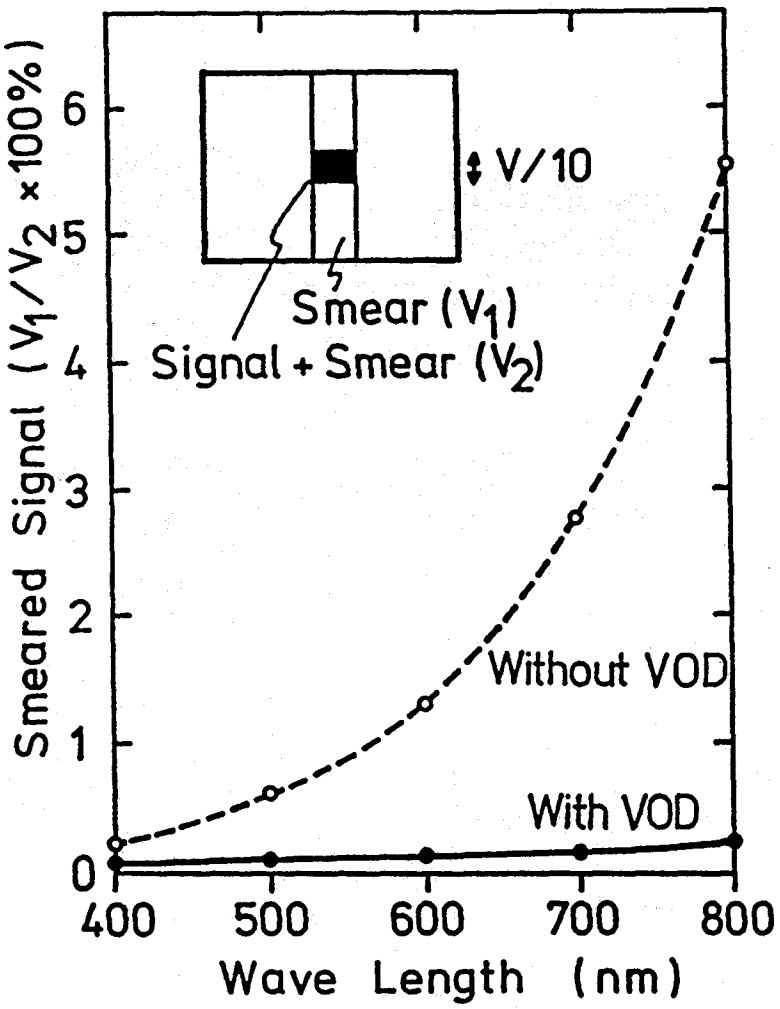


FIGURE 5—Percentages of smeared signal as a function of incident light wavelength.

Ishihara / NEC

ISSCC 82

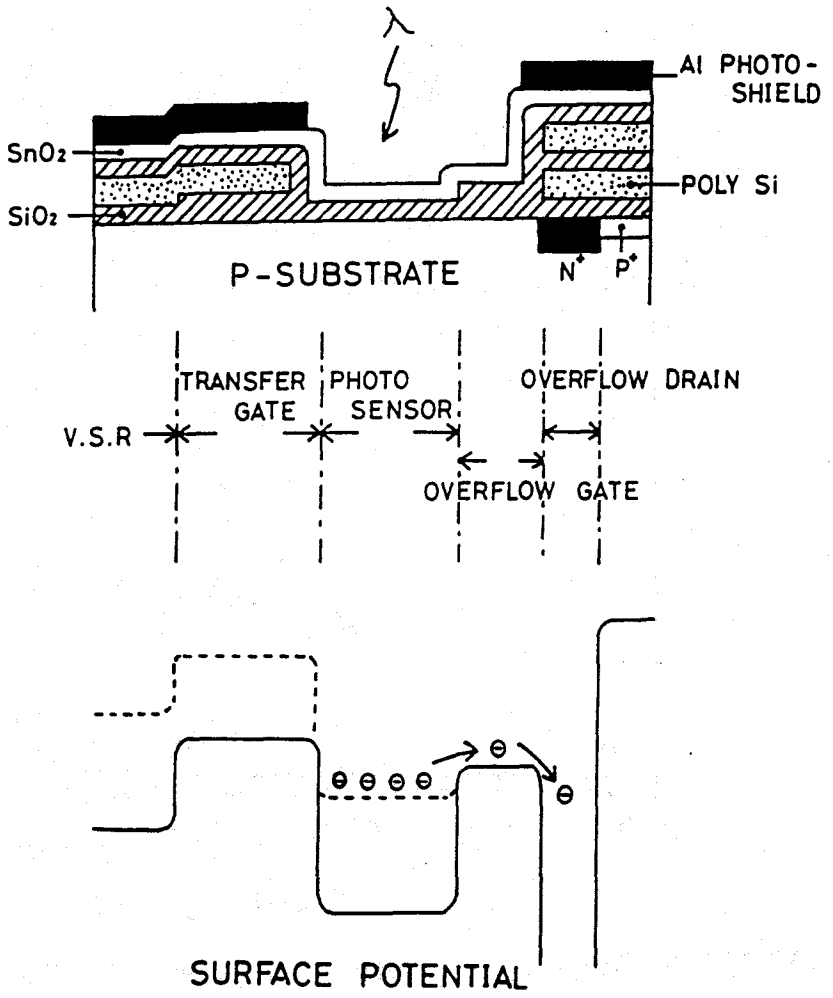


FIGURE 3—Cross sectional view and surface potential of antiblooming system.

Matsumoto et al / SONY

ISSCC 1978

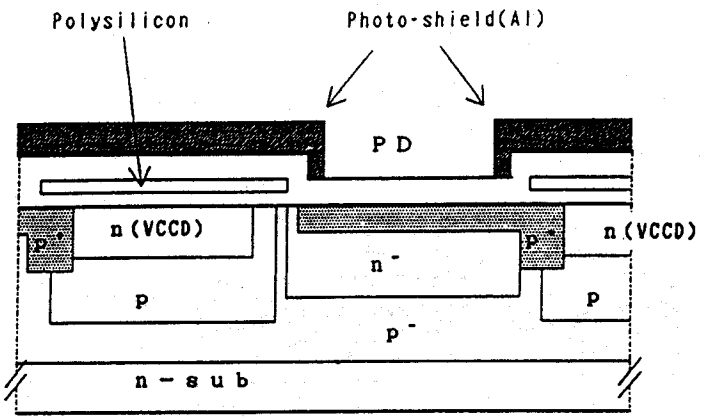


Fig. 5. Cross-sectional view of a unit cell.

Kuriyama et al

IEEE Trans

ED-38

May 1991

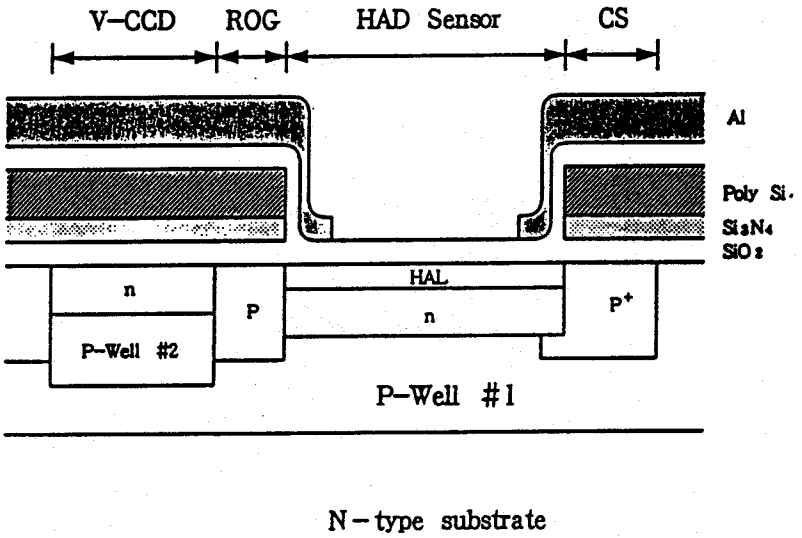


Fig. 3. Schematic cross-sectional view of the unit cell.

Hojo etal

IEEE Trans

ED-38

May 1991

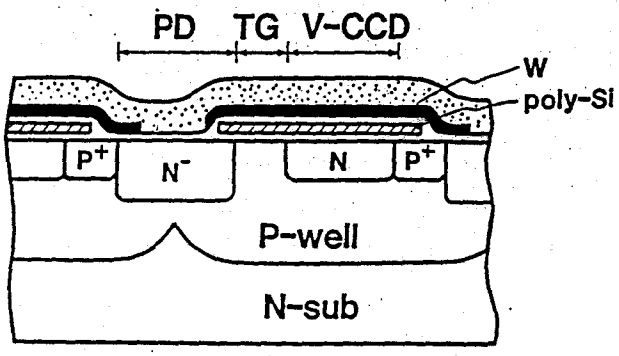
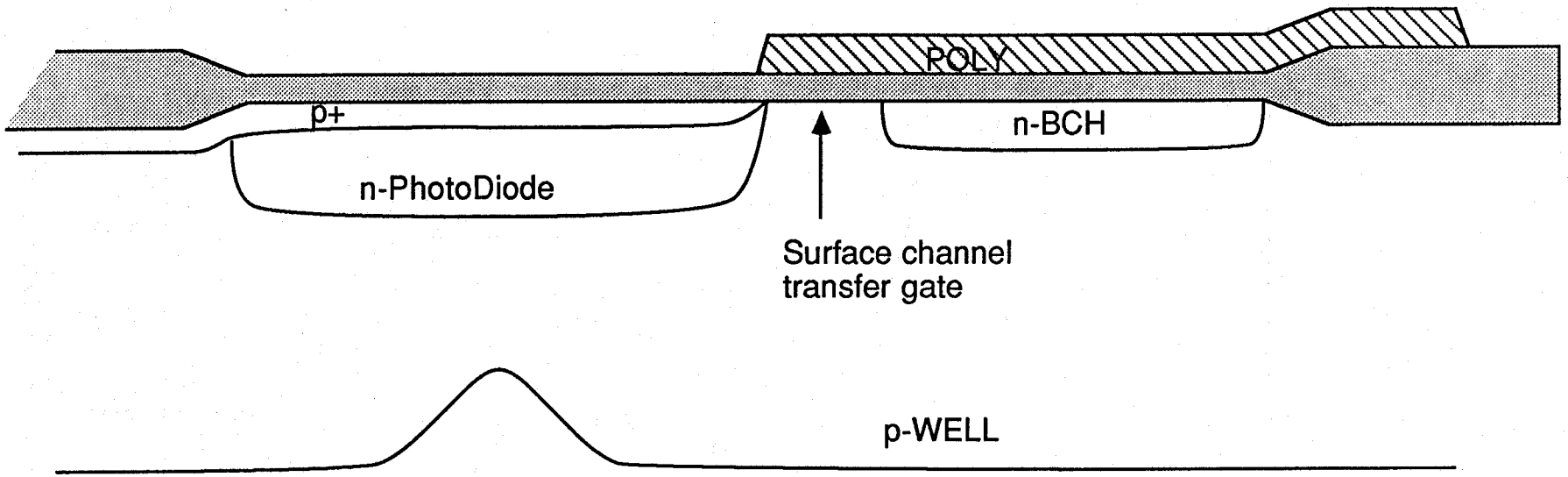


Fig. 5. Cross-sectional view of a unit pixel.

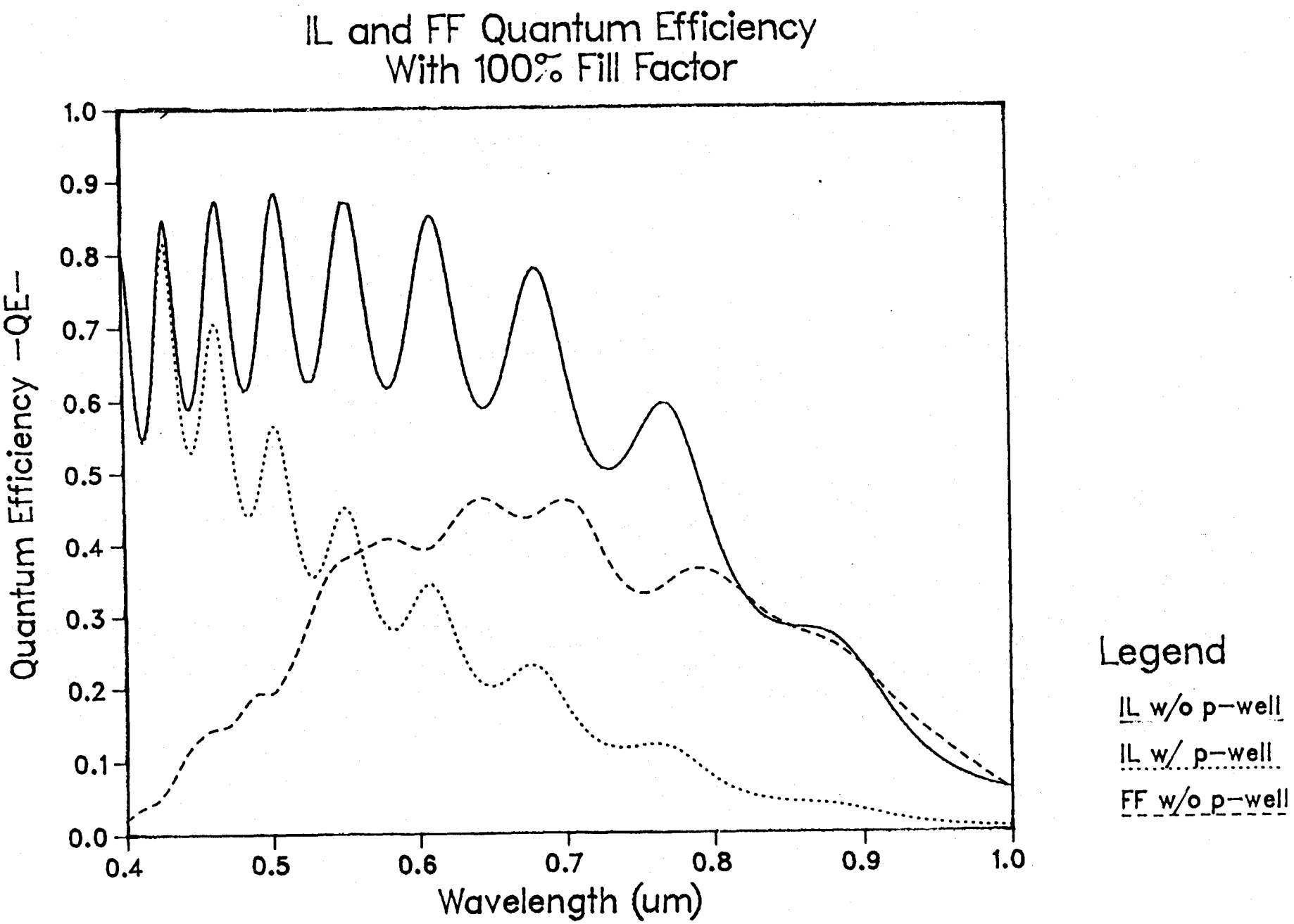
Toyoda et al

IEEE Trans ED-38

May 1991

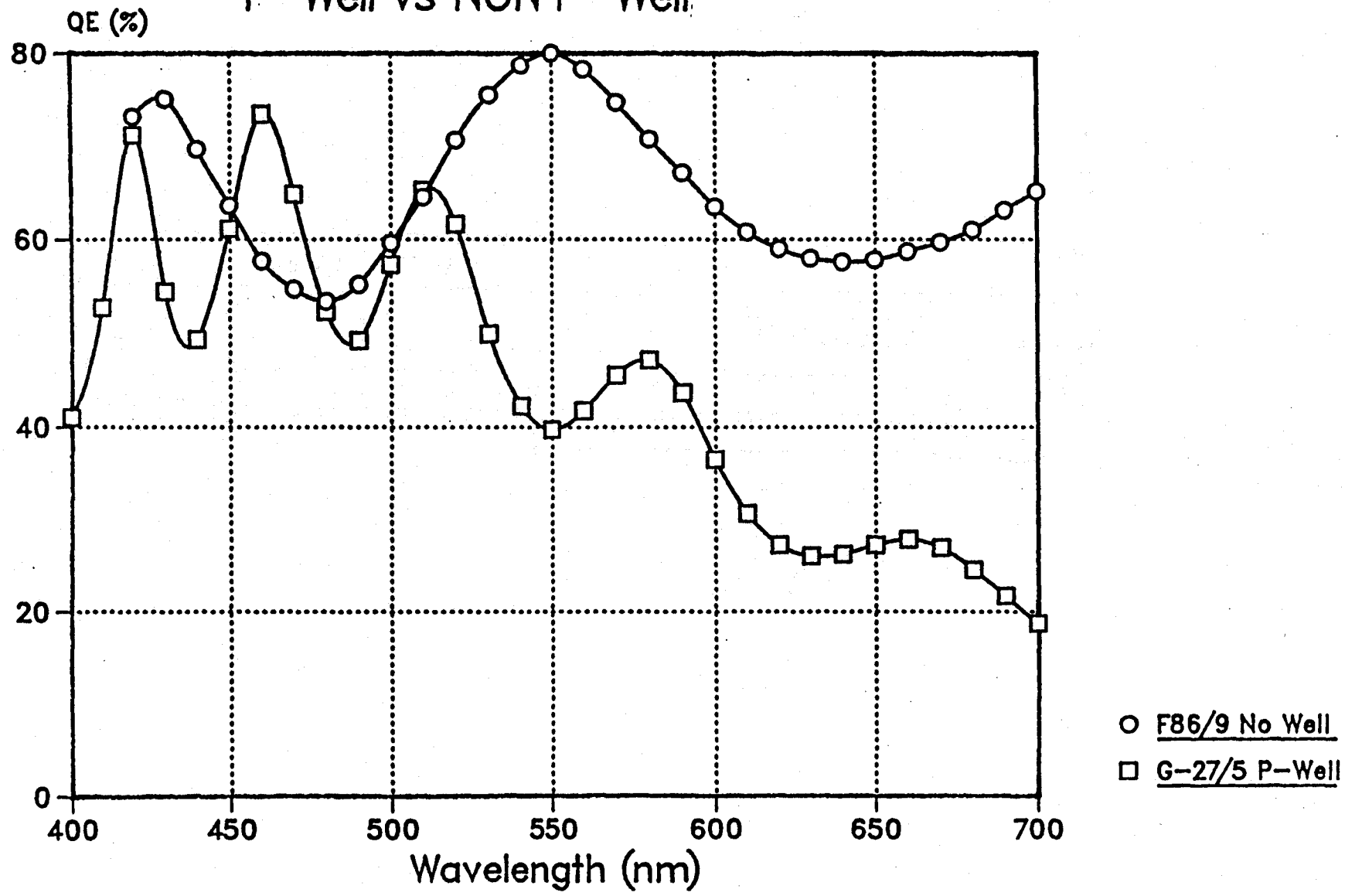


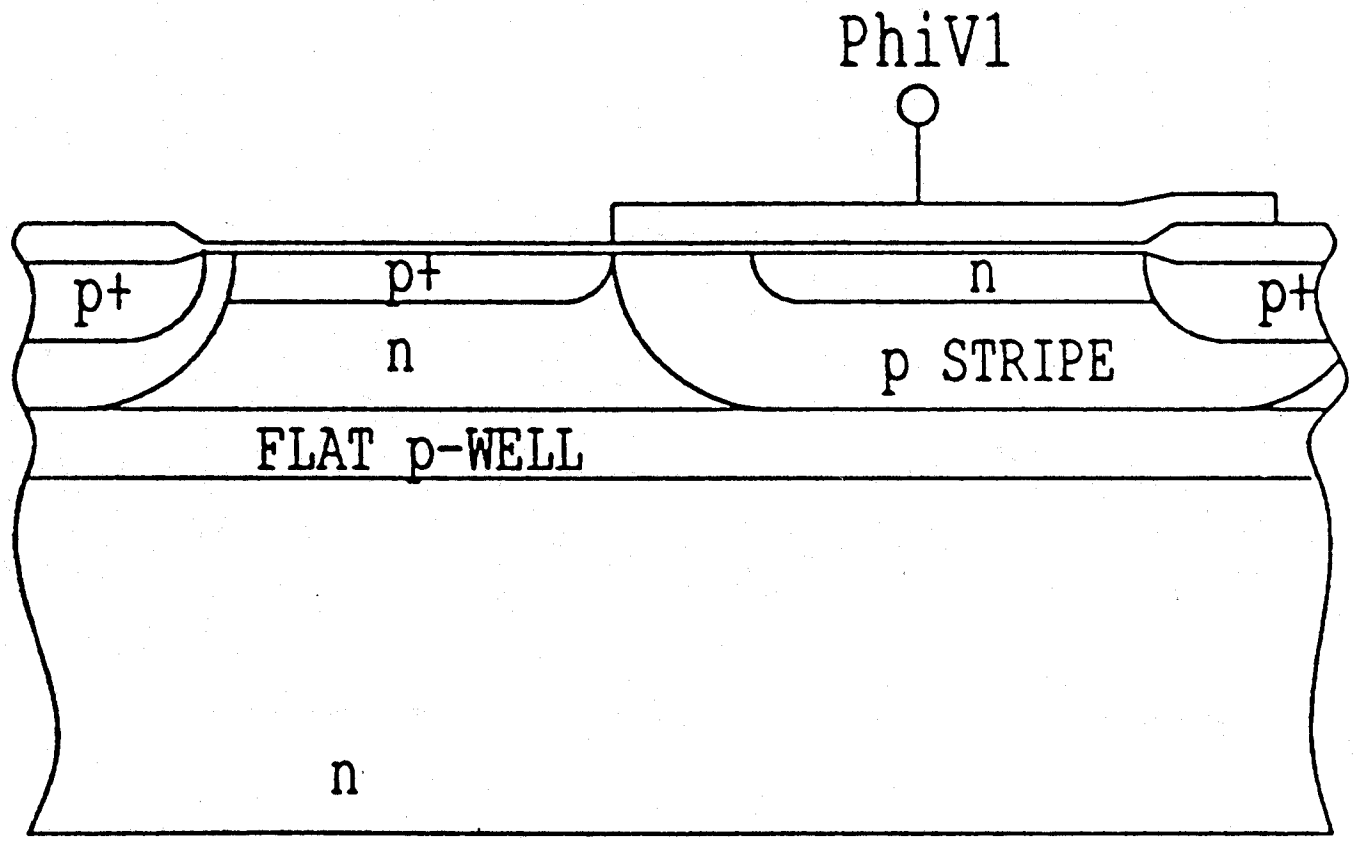
PIXEL CROSS-SECTION OF INTERLINE CCD WITH VOD

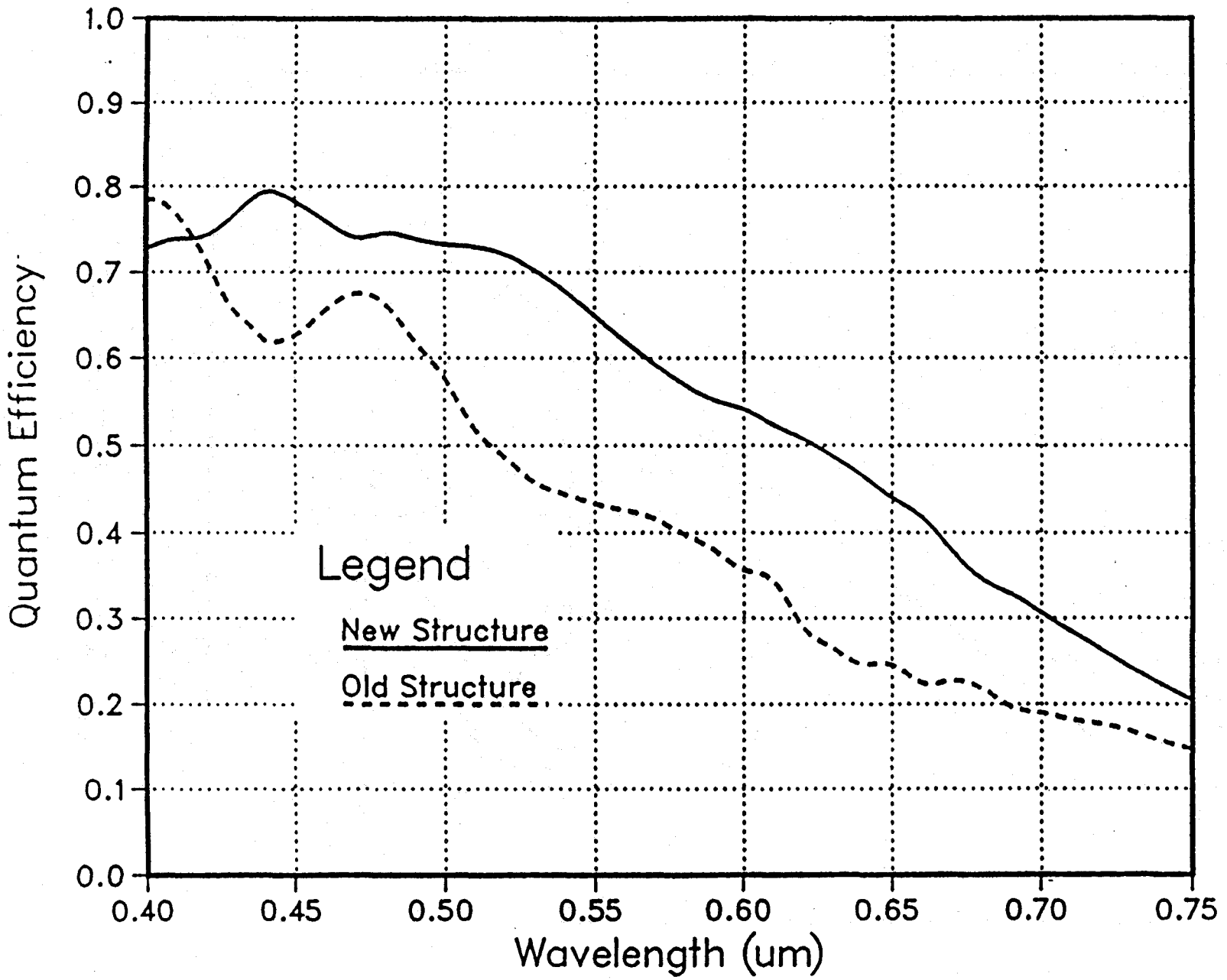

IL and FF Quantum Efficiency
With 100% Fill Factor
Quantum Efficiency -QE-
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Wavelength (um)
Legend
IL w/o p-well
IL w/ p-well
FF w/o p-well

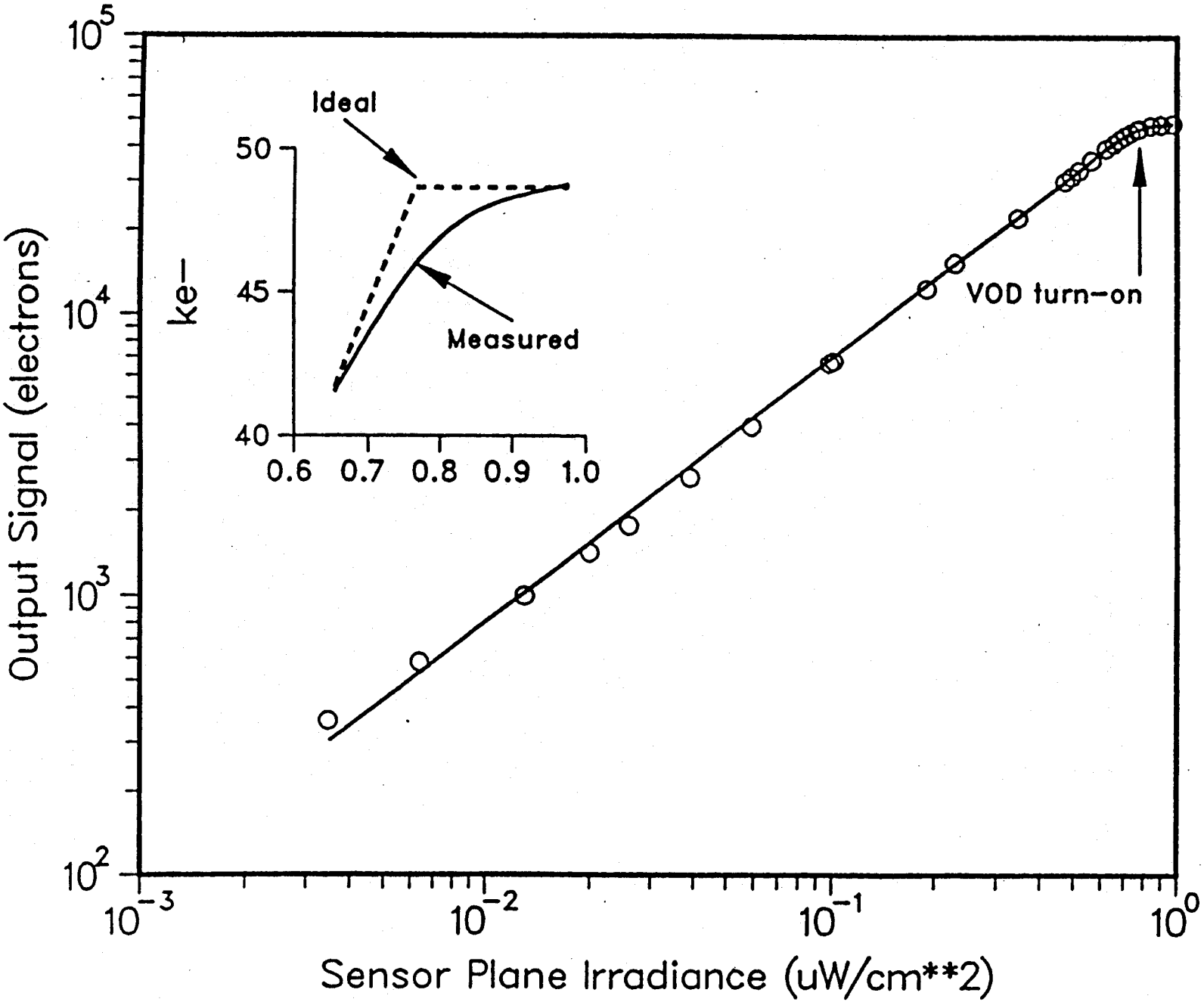
PHOTODIODE ABSOLUTE QUANTUM EFFICIENCY DATA 6/11/86

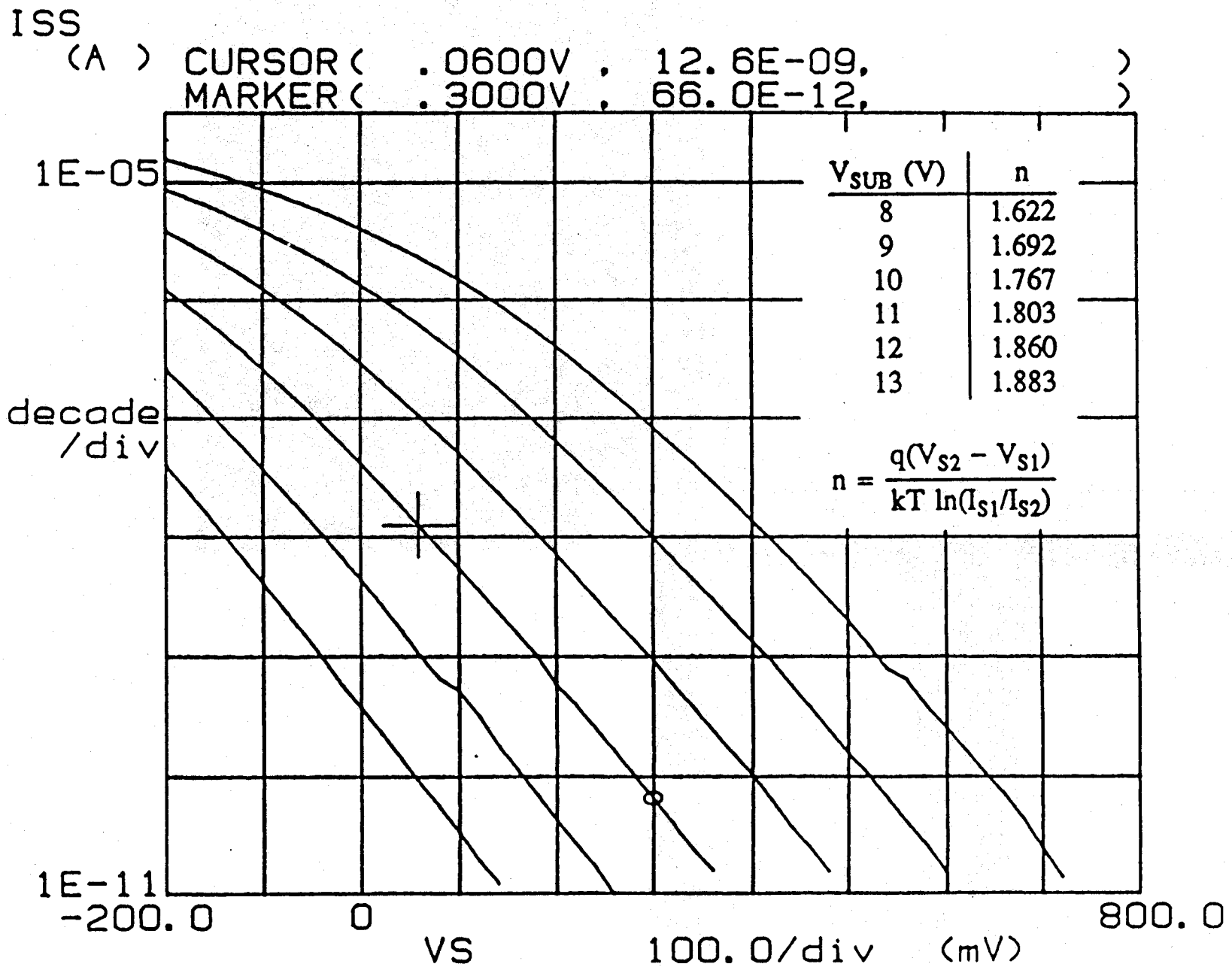
P–Well vs NON P–Well

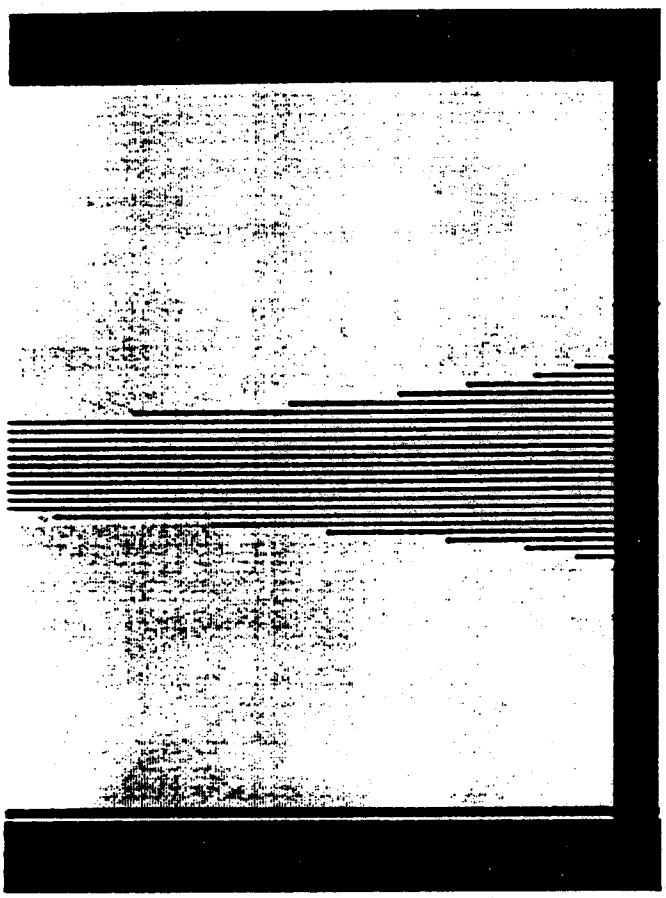



PhiV1
p+
p+
n
p+
n
p STRIPE
FLAT p-WELL
n


1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
Quantum Efficiency
0.40
0.45
0.50
0.55
0.60
0.65
0.70
0.75
Wavelength (um)
Legend
New Structure
Old Structure

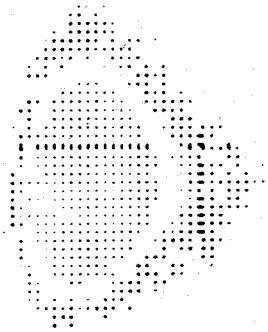

Output Signal (electrons)
10^5
10^4
10^3
10^2
10^{-3}
10^{-2}
10^{-1}
10^0
Sensor Plane Irradiance (uW/cm**2)
VOD turn-on
ke-
50
45
40
0.6
0.7
0.8
0.9
1.0
Ideal
Measured


ISS
(A)
CURSOR(.0600V , 12.6E-09,)
MARKER(.3000V , 66.0E-12,)
1E-05
decade
/div
1E-11
-200.0
0
800.0
VS
100.0/div (mV)
V_{SUB} (V) | n
8 | 1.622
9 | 1.692
10 | 1.767
11 | 1.803
12 | 1.860
13 | 1.883
$n = \frac{q(V_{S2} - V_{S1})}{kT \ln(I_{S1}/I_{S2})}$



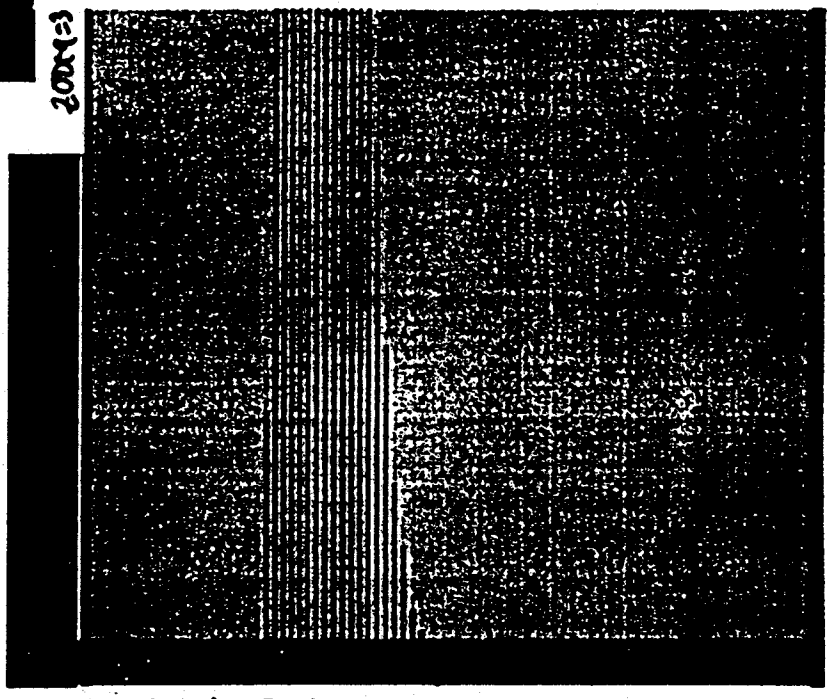
PD vs CCD DARK PATTERN CORRELATION 2/28

N298.I00 HISTOGRAM



PHOTODIODE DARK PATTERN 2/28/89

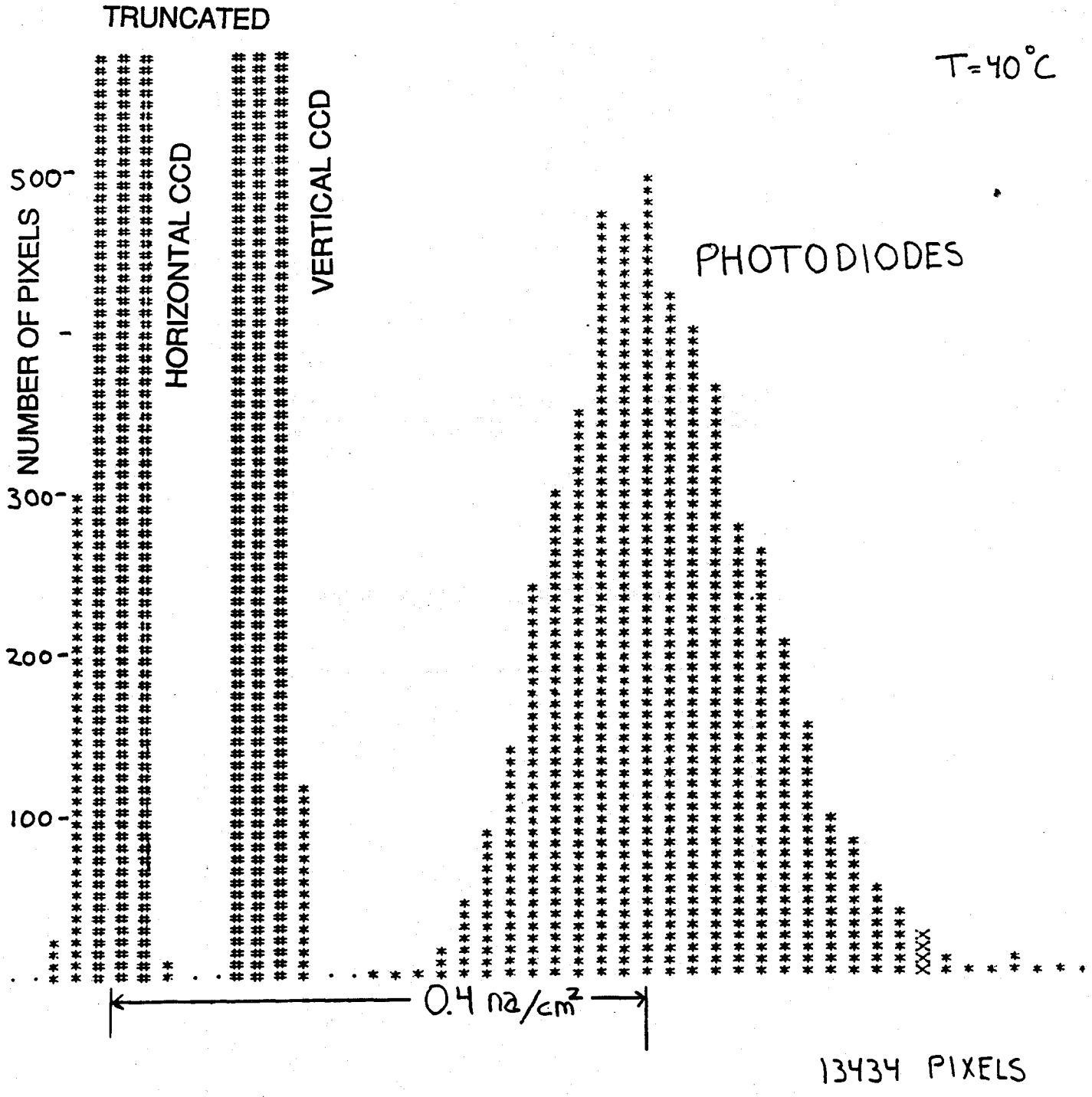
ZOOM=3



N29A.I00 HISTOGRAM

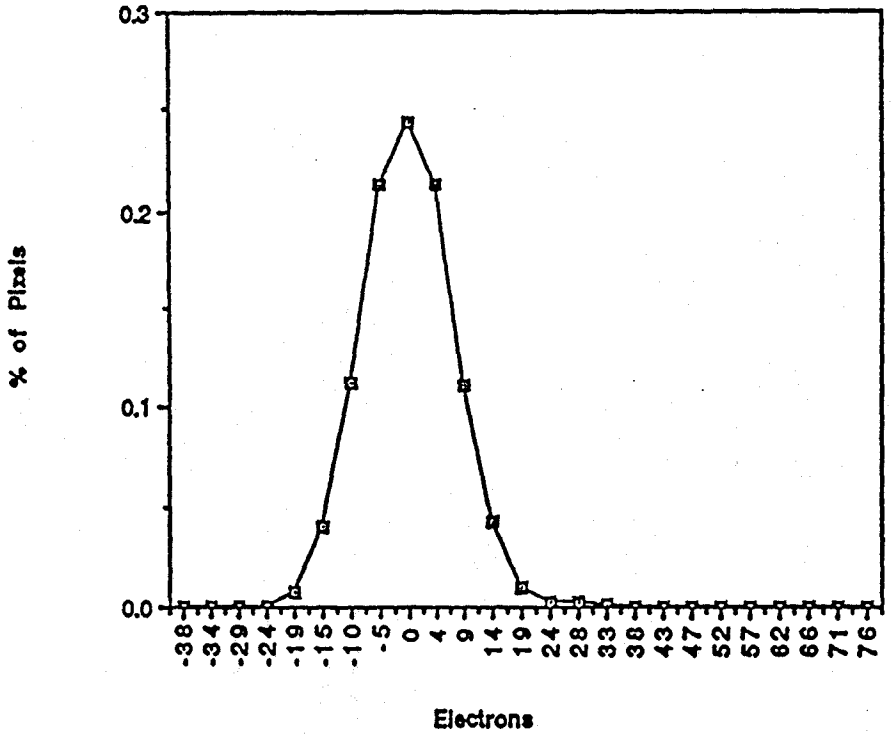
DARK CURRENT HISTOGRAM

NUMBER OF PIXELS WITH A GIVEN DARK CURRENT VERSUS DARK CURRENT



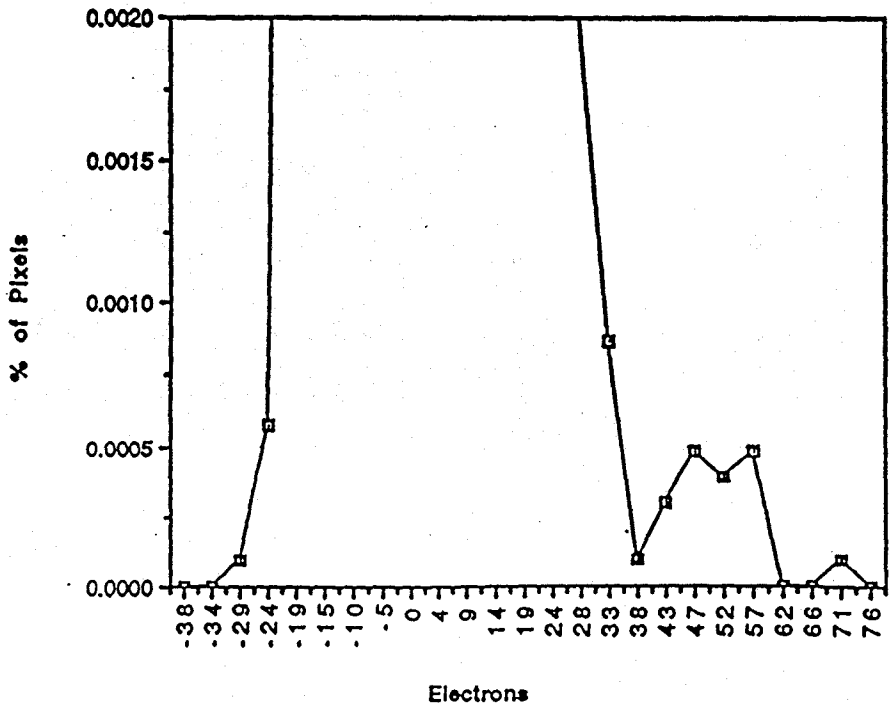
DARK CURRENT PATTERN NOISE

AT 40°C

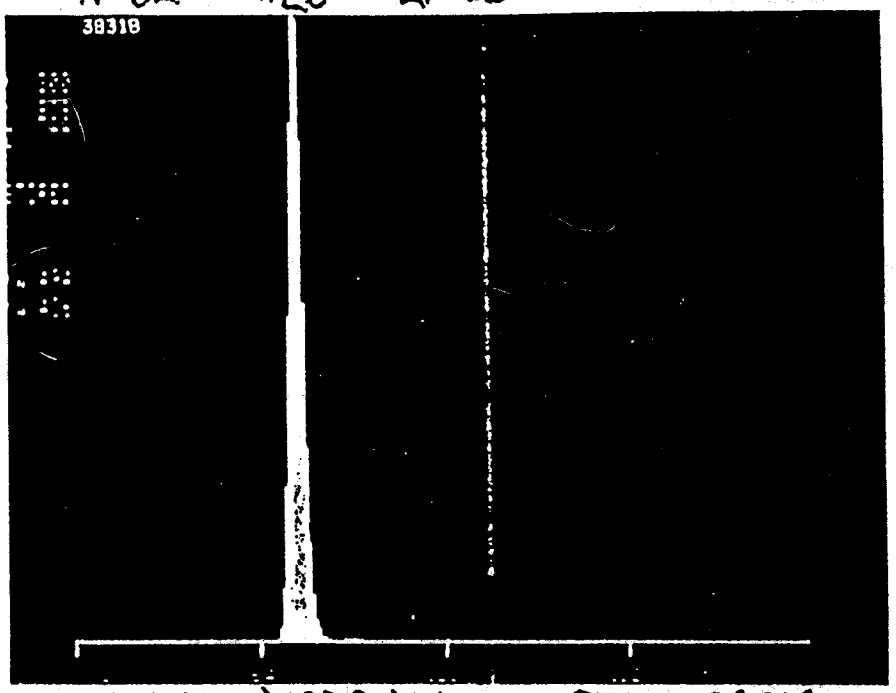


DARK CURRENT PATTERN NOISE

AT 40°C

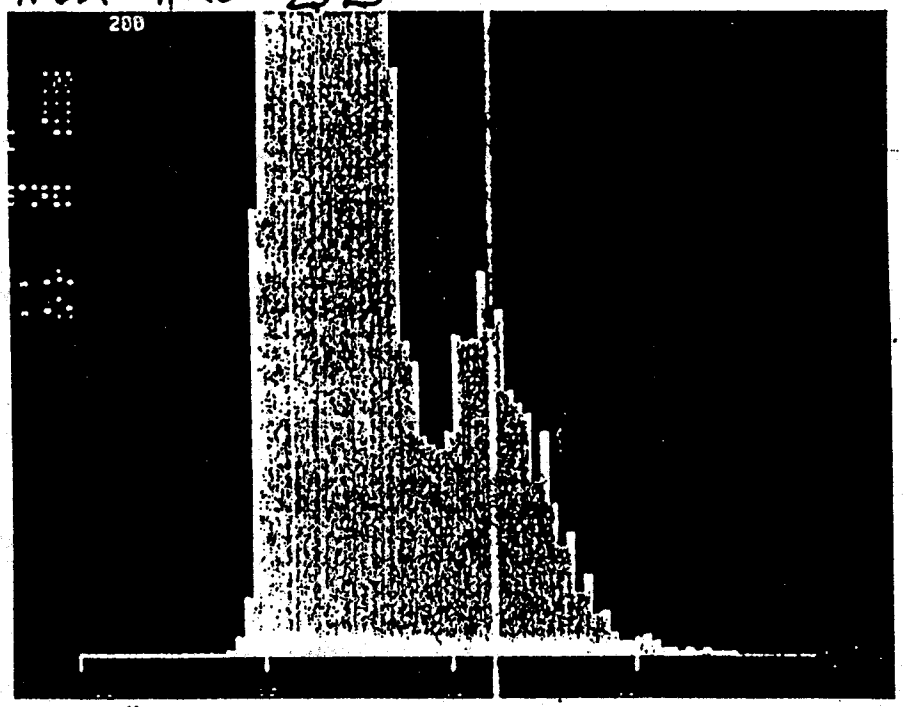


N-32 #20 25:25



- TOTAL DISTRIBUTION - PEAK = 38,318.

N-32 #20 23:23



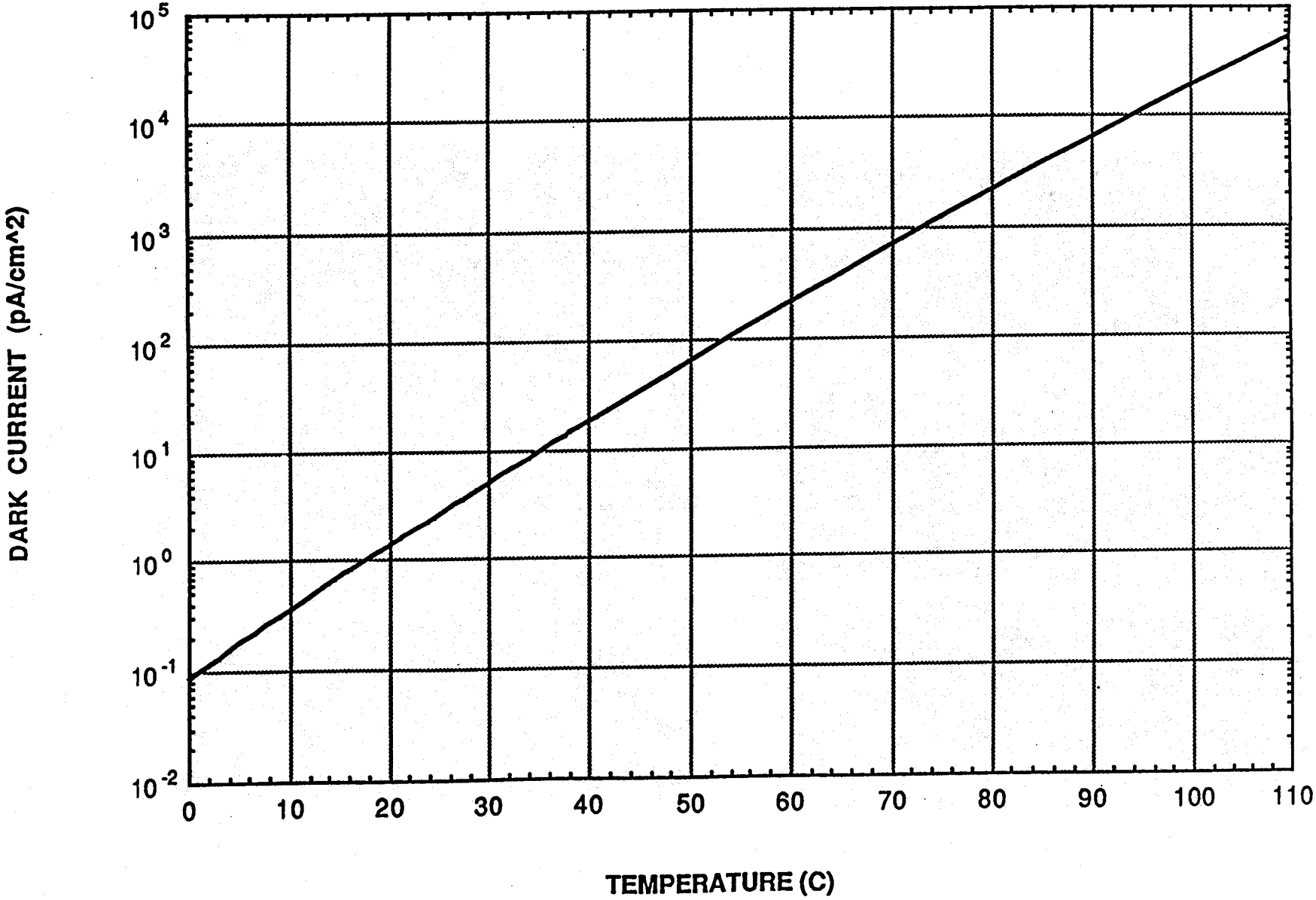
- "BLOW-UP" OF BASE - CLIPPED AT 200.

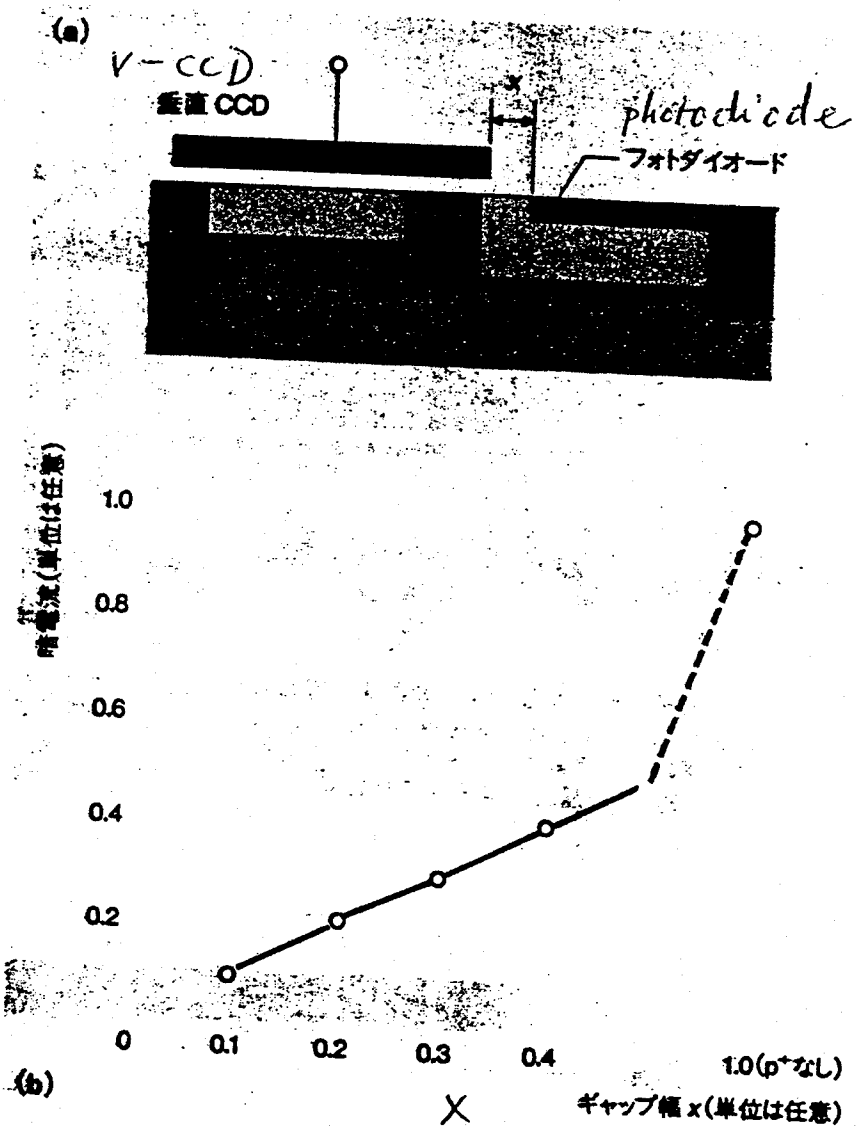
$J_b = 0.46 nA/cm^2$

PTS. = 110/1492

KAF-1400

DARK CURRENT vs TEMPERATURE





Hiroshima / Matsushita

Nikkei Microdevice Nov. 88

SUMMARY