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A Schottky-Barrier Image Sensor with 100% Fill Factor

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ABSTRACT

A new concept, the Direct Schottky Injection (DSI), is described for a 3-D construction of infrared imagers with a continuous Schottky-barrier-detector surface on one side of a thinned (10 to 25 μm) silicon substrate and p-type buried-channel CCD readout structure on the other side. The DSI structure provides a 100% fill factor, a large charge-handling capacity, and a high-density pixel design. The construction and operation are described for DSI imagers with frame-transfer CCD (FT-CCD) and interline-transfer CCD (IT-CCD) readout. The operation of the IT-CCD DSI imager was demonstrated with a 128 x 128 focal plane array (FPA) with 50-μm x 50-μm pixels.

1.0 INTRODUCTION

This paper describes new types of monolithic Schottky-barrier-detector imagers that are referred to as Direct Schottky Injection (DSI) imagers. The unique feature of the DSI construction is that it produces very high density monolithic focal plane arrays (FPAs) with 100% fill factor by virtue of a 3-D construction using a thinned silicon substrate with a continuous Schottky-barrier silicide layer on one side and a p-type buried-channel CCD readout on the other side [1].

In 1973, Shepherd and Yang, from RADC, Hanscom AFB, proposed silicide Schottky-barrier detector (SBD) arrays for infrared thermal imaging [2]. Infrared image sensors with 25 x 50 and 256 x 1 SBDs with thick PtSi film (~ 1000 Å) were demonstrated in 1978 [3, 4]. The major breakthrough in the improvement of the responsivity of PtSi SBDs by about two orders of magnitude came with the introduction of SBDs with optical cavity having a thin (20 to 50 Å) PtSi film [5-8]. This initial breakthrough was made in 1979 by the David Sarnoff Research Center, Princeton, NJ (formerly RCA Laboratories) as a result of the support and cooperation of RADC, Hanscom AFB.

The present state-of-the-art of the Schottky-barrier image sensors is represented by the following reported focal plane arrays (FPAs) [9-13]. A 320 x 244-element 2:1 vertical-interlaced interline-transfer-CCD FPA was developed at the David Sarnoff Research Center [9]. A 324 x 487-element 2:1 vertically interlaced interline-transfer-CCD FPA was developed at NEC [10]. A 256 x 244-element and a 488 x 512-element 2:1 vertically-interlaced interline-transfer-CCD FPAs were developed at Loral Fairchild [11]. A 512 x 512-element 2:1 vertically interlaced charge-sweep-device (CSD) FPA was developed at Mitsubishi [11]. A hybrid 256 x 256-element integrating-amplifier-type FPA with MOS readout developed at Hughes [13]. With the exception of the hybrid SBD FPAs [13] that can be constructed with 80 to 90% fill factor, the high-density monolithic SBD FPAs [9, 12] employ discrete Schottky-barrier detectors integrated with n-type buried-channel CCD readout multiplexer and are constructed with a fill factor of 30 to 40%. However, the 3-D construction demonstrated with the 128 x 128-element interline-transfer-CCD (IT-CCD) DSI FPA described in this paper, in addition to the 100% fill factor, allows a design of very high-density FPAs with large charge-handling capacity.

2.0 DSI CONCEPT

The Direct Schottky Injection (DSI) FPAs described in this paper represent a new type IR FPA with 100% fill factor [1]. The DSI FPA illustrated in Fig. 1 consists of a continuous PtSi or Pd_2Si Schottky-barrier electrode (DSI surface) formed on one surface of a thinned silicon substrate with the CCD readout registers formed on the other side of the thinned silicon substrate. During DSI FPA operation, the silicon substrate is depleted between the DSI surface and the charge collecting elements of the readout structure. Since the whole DSI surface (PtSi, IrSi, or Pd_2Si on p-type Si substrate) injects hot holes that drift along the electric field lines toward the collecting elements, the DSI FPA has a 100% fill factor and the charge readout is accomplished by a p-channel CCD multiplexer in the form of either a frame-transfer (FT) or an interline-transfer (IT) CCD structure.

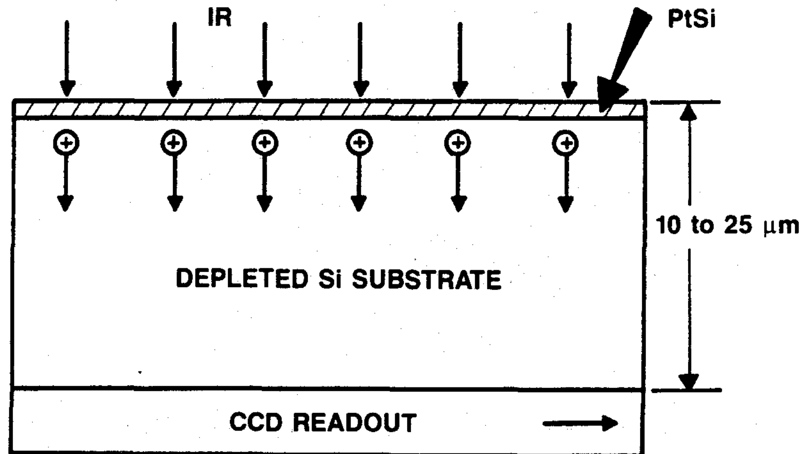


Figure 1. Direct-Schottky-Injection (DSI) FPA structure.

3.0 FRAME-TRANSFER-CCD DSI FPA

The concept of the frame-transfer-CCD DSI imager was originally described by J. E. Carnes [14]. The construction and operation of the FT-CCD DSI imager are illustrated in Fig. 2. As shown in Figs. 2(a) and (b), p-channel buried-channel-CCD readout registers are constructed on one side of about 10-μm-thick 100-ohm-cm n-type silicon substrate. A PtSi DSI surface is formed on an implanted p-type layer on the other side of the thinned silicon substrate. As part of the operation of the FT-DSI FPA, voltage pulses applied to the CCD gate deplete the whole p-n-p structure. During the optical integration time, the infrared radiation (signal) absorbed in the silicide layer generates hot holes that are injected over the Schottky barrier and drift into the p-type buried-channel CCD wells on the other side of the p-n-p silicon structure. Then, the CCD readout structure transfers the detected charge signal to output terminals.

The operation of a DSI imager with a frame-transfer (FT) CCD readout was demonstrated with a 100 x 100-element array with 50-μm x 50-μm pixels [15]. The main advantage of DSI imager with the FT-CCD readout is that it allows the construction of very high density staring infrared focal plane arrays (FPAs). The FT-CCD readout, however, has an inherent smear unless some form of shutter is used. The above limitation can be overcome by a DSI imager with an interline-transfer (IT) CCD readout described in the following sections.

4.0 INTERLINE-TRANSFER-CCD DSI FPA

4.1 STRUCTURE AND OPERATION

The architecture of the interline transfer CCD DSI imager is shown in Fig. 3. The overall construction of the IT-CCD DSI imager (shown in Figs. 4-6) is basically the same as that of the 160 x 244-element and 320 x 244 IT IR-CCD imager [9, 16]. However, the IT-CCD DSI imager has p-type buried-channel CCD (BCCD) registers formed in N-wells. Charge-collecting P^+ electrodes replace the PtSi

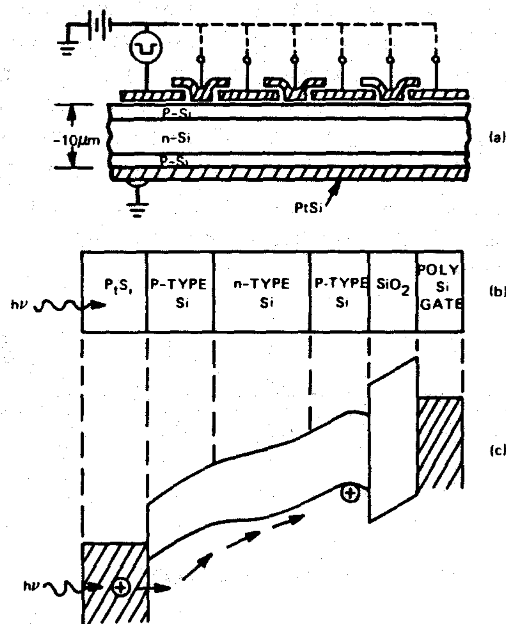


Figure 2. Construction and operation of an FT DSI-CCD imager.

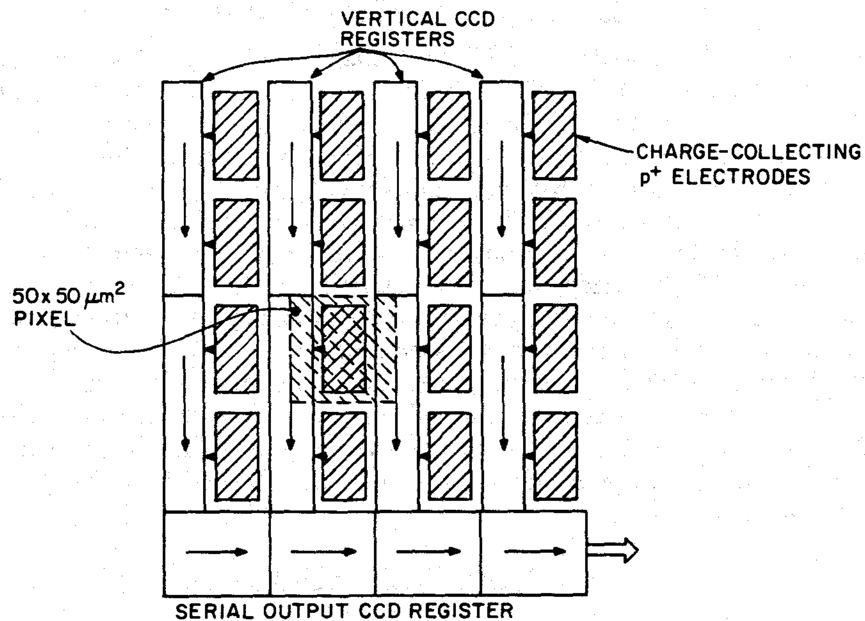


Figure 3. Architecture of the IT-CCD DSI imager.

Schottky-barrier detectors of a conventional IT IR-CCD imager, and the above structure rests on a P^{--} silicon substrate ($N_{sub} = 10^{13} cm^{-3}$) thinned to about 25 µm with the DSI PtSi surface formed on the backside. As illustrated in Fig. 5, the charge-collecting electrode gates serve the following functions:

(1) to increase the capacitance, or the charge-handling capacity, of the charge-collecting P^+ electrodes
(2) to form the blooming barrier for antiblooming overflow P^+ drains
(3) to define the channel stops for the p-type BCCD channels

Figure 4 shows the top view of the 128 x 128 IT-CCD DSI imager with 50-µm x 50-µm pixels. Figure 5 shows section A-A across the vertical BCCD channels. This section illustrates the pixel definition in the horizontal direction. Section B-B in Fig. 6 illustrates the pixel definition in the vertical direction. The construction of the N-wells can be visualized as a single large N-well with windows (openings) at the charge-collecting P+ electrodes containing the whole active area of the array. The IT-CCD DSI imager illustrated in Figs. 4 through 6 operates with a CCD readout of two vertically interlaced fields (each having 128 (H) x 64 (V) elements) per frame (with 128 x 128 elements). During the operation of the IT-CCD DSI imager, the difference of the potentials applied between the PtSi back surface (V_{BS}) and the charge-collecting P^+ electrodes depletes the P^{--} substrate. Therefore, the "hot holes" injected at the PtSi back surface as a result of IR signal follow the electric field lines (in the depleted P^{--} silicon substrate) toward the charge-collecting P^+ electrodes. The P^+ electrodes are, in turn, electrically isolated from each other by the N-wells that also act as potential barriers for the injected "hot" holes.

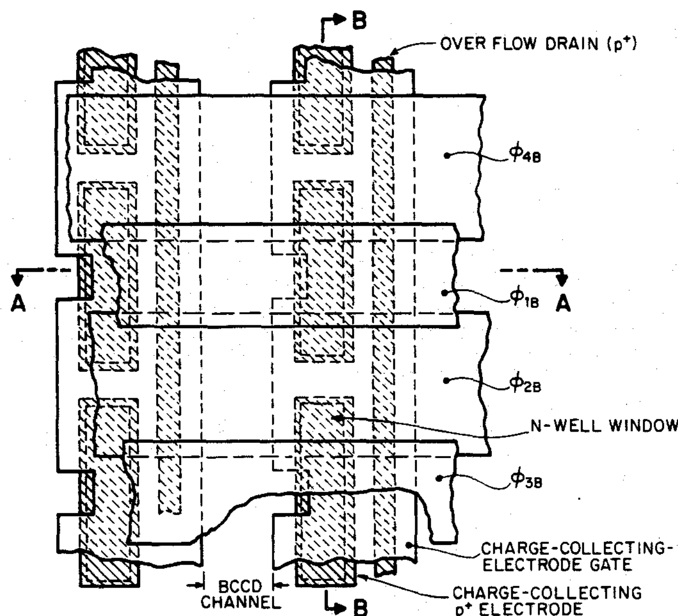


Figure 4. Top view of the IT-CCD DSI imager.

The charge readout from the P^+ charge-collecting electrode (CCE) to the p-type buried-channel CCD register is illustrated in Fig. 7. The BCCD channel and the surface-channel CCD (SCCD) transfer region are defined in the spaces between the DC-biased CCE gates. The biasing of the CCE-gates is adjusted to provide the overflow (blooming) barriers between the P^+ charge-collecting electrodes and the P^+ overflow drains. The SCCD channel stops under the DC-biased CCE gates isolate the BCCD channel on the right side from the CCEs (not shown in the cross-sectional view in Fig. 7(a)) and on the left side from the P+ overflow drains (see Fig. 7(a)). The potential profiles in Fig. 7(b) illustrate the readout of the detected charge signal (Q_D) and the control of blooming by charge overflow into the P^+ over-flow drain.

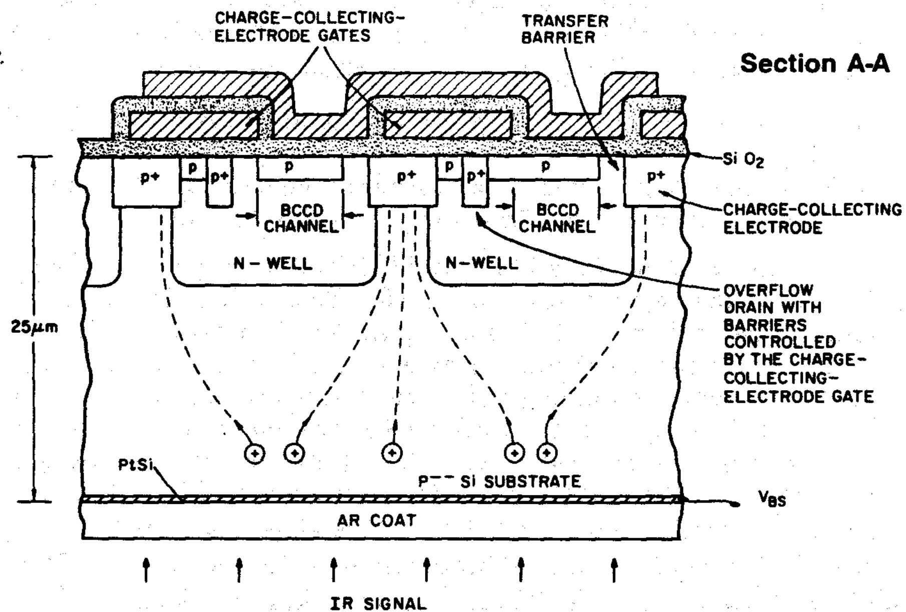


Figure 5. Cross-sectional view of the IT-CCD DSI FPA across the BCCD channels (Section A-A of Fig. 4).

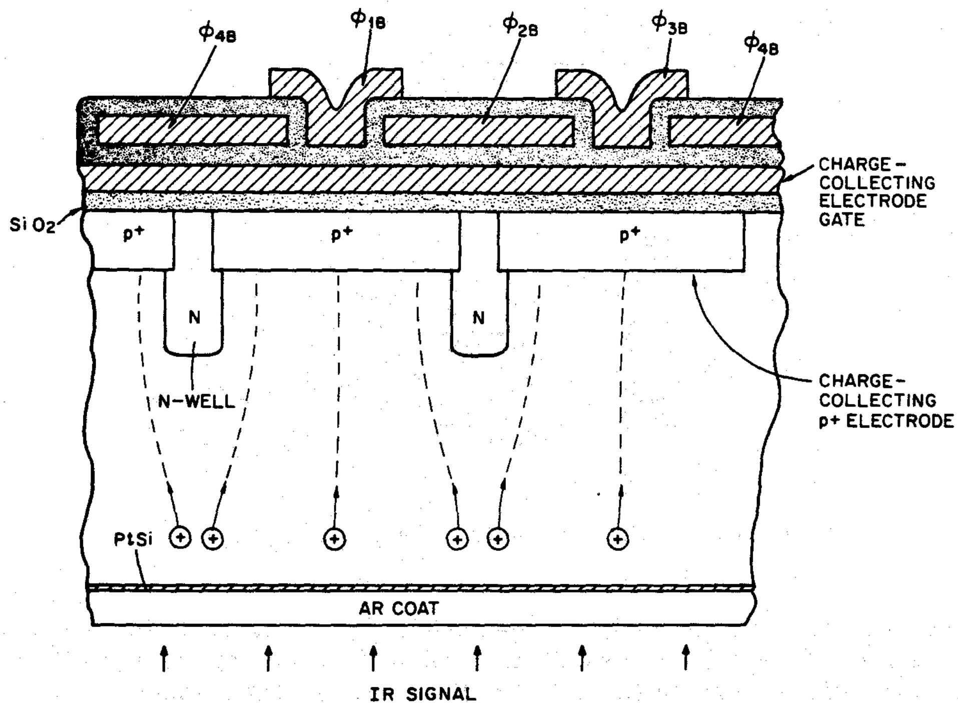


Figure 6. Cross-sectional view of the IT-CCD DSI FPA across the charge-collecting P^+ electrodes and parallel to the BCCD channels (Section B-B of Fig 4).

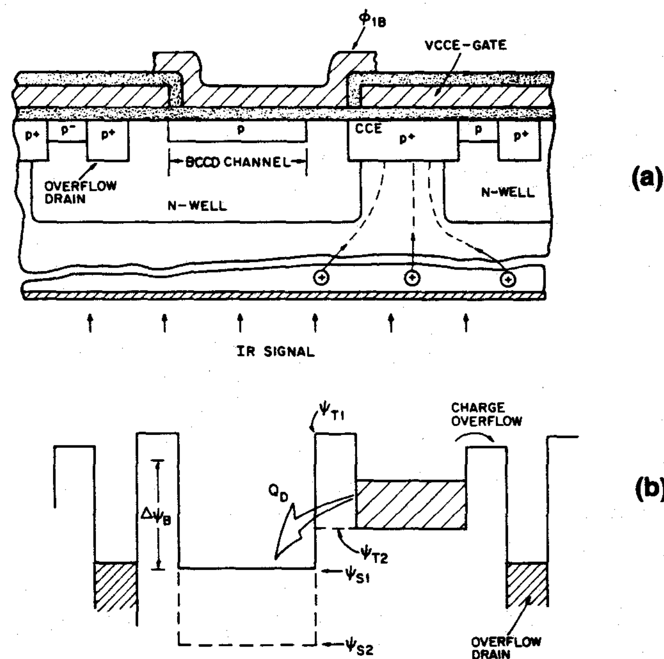


Figure 7. Operation of the IT-CCD DSI FPA showing a cross section of a pixel in (a) and the potential profiles in (b).

4.2 CONSTRUCTION OF 128 X 128 IT-CCD DSI FPA

The operation of the IT-CCD DSI imager has been demonstrated with a 128 x 128 imager with 50-µm x 50-µm pixels. The design and operation of this imager were illustrated in Figs. 3-6.

The initial demonstration of the IT-CCD DSI imager was made with SBD test devices made on a 1000-Ω-cm p-type silicon substrate that was thinned to about 25 µm. The test of these SBDs showed the same basic current characteristics as the typical Schottky-barrier detectors (SBDs) [16]. However, as the SBD voltage was increased to the value sufficient to deplete the 25-µm substrate up to the P^+ charge-collecting electrode, the SBD current started to increase sharply. Therefore, to prevent the formation of a complete depletion of the Si substrate (i.e., a punch-through from the silicide surface to the P^+ charge-collecting electrode) and also to maximize the charge collection efficiency, an additional p-type implant was used in the construction of the 128 x 128 IT-CCD DSI FPA that provides a more graded doping profile for the charge collecting electrode. The final computed doping profiles for the N-well implant in the original P^{--} substrate, the P-type implant profile, and the N-well doping profile in the P implant are shown in Fig. 8. The sketches of the resulting charge collecting electrode structures are illustrated in Fig. 9. The structure in Fig. 9(a) was made with a uniform p-type implant which partially compensated the N-well implant and resulted in a 4-µm deep N-well. The structure in Fig. 9(b) was formed by defining the p-type implant over the P^+ charge-collecting-electrode area. The 128 x 128 DSI imager for which the experimental data is given in Section 4.3 was made with the p-type implant profile shown in Fig. 9(a).

The 128 x 128 IT-CCD DSI arrays were fabricated by completing the CCD process on the top of the wafers, including the definition of aluminum. The <100> 1000-ohm-cm p-type silicon wafers were thinned from the back-side to a final thickness of 25 µm. Then, a layer of Pt was deposited and sintered on the thinned surface forming the PtSi DSI surface. The finished wafers were sawn into chips and the 25-µm-thick 128 x 128 IT-CCD DSI arrays were found to be sufficiently rigid for mounting in a ceramic package designed for operation with back-side (through the PtSi side) illumination through a window. A photomicrograph of the output section of the 128 x 128 IT-CCD DSI imager is shown in Fig. 10.

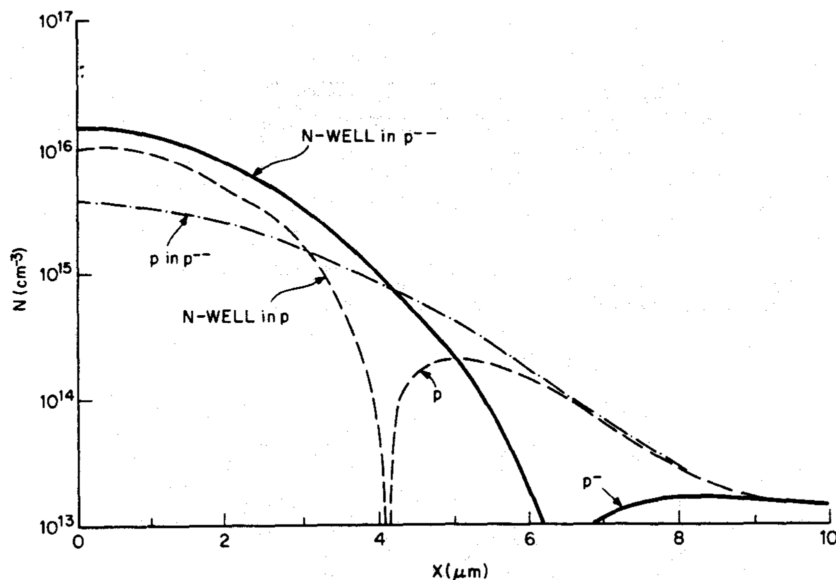


Figure 8. Computed implant profiles for the 128 x 128 IT-CCD DSI imager.

4.3 EXPERIMENTAL RESULTS FOR 128 X 128 IT-CCD DSI FPA

The measurements of the DSI test structures, fabricated on the same wafer with the 128 x 128 IT-CCD DSI FPAs, gave Schottky-barrier detector responsivities characterized by C_1 coefficient of 0.07 to 0.10 eV^{-1} and Ψ_{ms} of 0.21 eV. The above result is consistent with the reduction of the C_1 coefficient due to the absence of the optical cavity in the tested DSI structure [16]. For the typical operation with 15 V between the P^+ charge-collecting electrode and the PtSi surface, the dark current at 77K was in the range of 2 to 3 nA/cm^2.

The 128 x 128 IT-CCD DSI imager was operated at 30 frames/s with f/1.2 cold shield. The thermal imaging illustrated in Fig. 11 was obtained using a 12-bit uniformity corrector that subtracts a 300K background signal (in the form of 16 averaged frames) from the video output [15]. The 128 x 128 image was then converted to the standard 488-line TV format by means of a frame converter.

The imager output was detected with a two-stage floating-diffusion on-chip amplifier. The first stage of the amplifier was operated as an inverter and the second stage of the amplifier was operated as a source follower. The floating diffusion amplifier had a charge-to-voltage conversion ratio of 3600 electrons/mV.

The output signal was 1.1 x 10^6 electrons/pixel for operation with 300K background. At this background level the measured temporal output noise was 1100 rms electrons/pixel. The responsivity of this imager was measured to be 2.9 x 10^4 electrons/pixel/K. The saturation signal level for this imager was measured as 3 x 10^6 electrons/pixel.

The fill factor and the cross-talk between pixels were measured by projecting on the focal plane a 30-μm-wide line signal with a blur spot of about 30 μm. The scope traces obtained by scanning such vertical line across the 50-μm pixels in the horizontal direction are shown in Fig. 12(a) for the line projected at the center of a pixel and in Fig. 12(b) for the line projected at the border between two pixels. The detected signal for two adjacent pixels for scanning a vertical line across the 50-μm x 50-μm pixels in the horizontal direction is shown in Fig. 13(a) and for the case of the vertical scanning with a horizontal line in Fig. 13(b). An inspection of the data in Figs. 12 and 13 shows that the 128 x 128 IT-CCD DSI has a crosstalk between two pixels of less than 20% and that the fill factor of this imager is 100%.

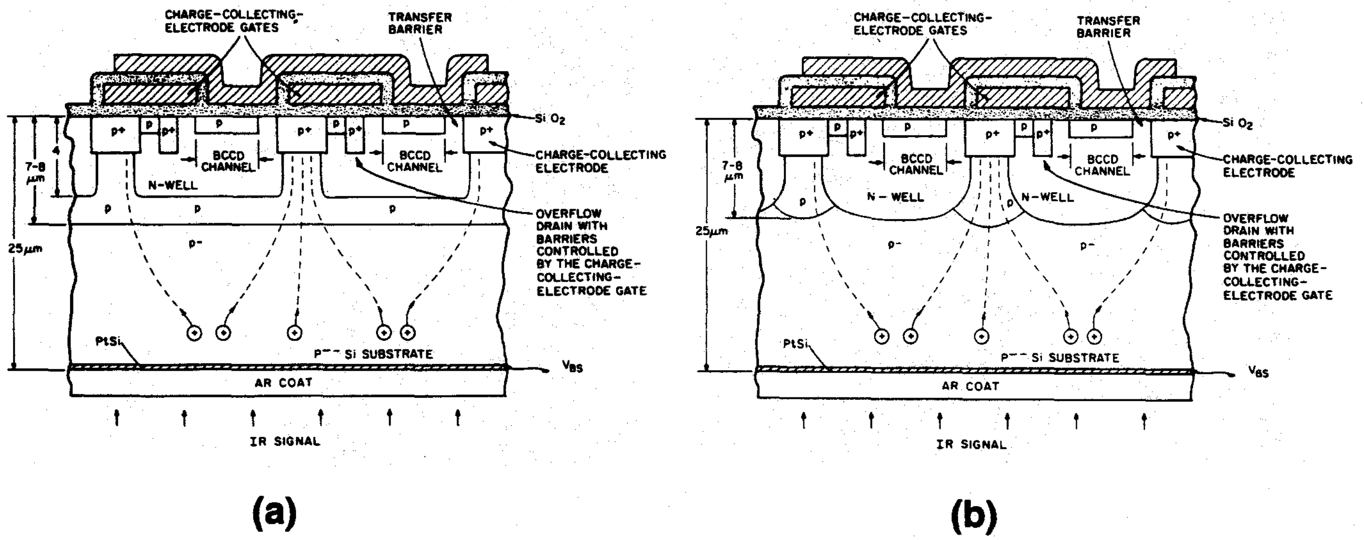


Figure 9. Sketches illustrating the two types of charge-collecting-electrode constructions for the 128 x 128 IT-CCD DSI array.

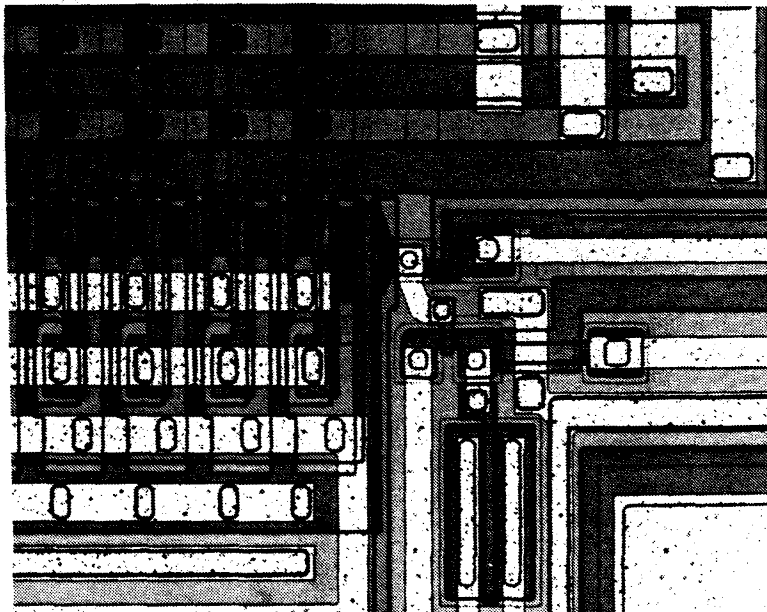


Figure 10. Photomicrograph showing the output section of the 128 x 128 IT-CCD DSI imager.

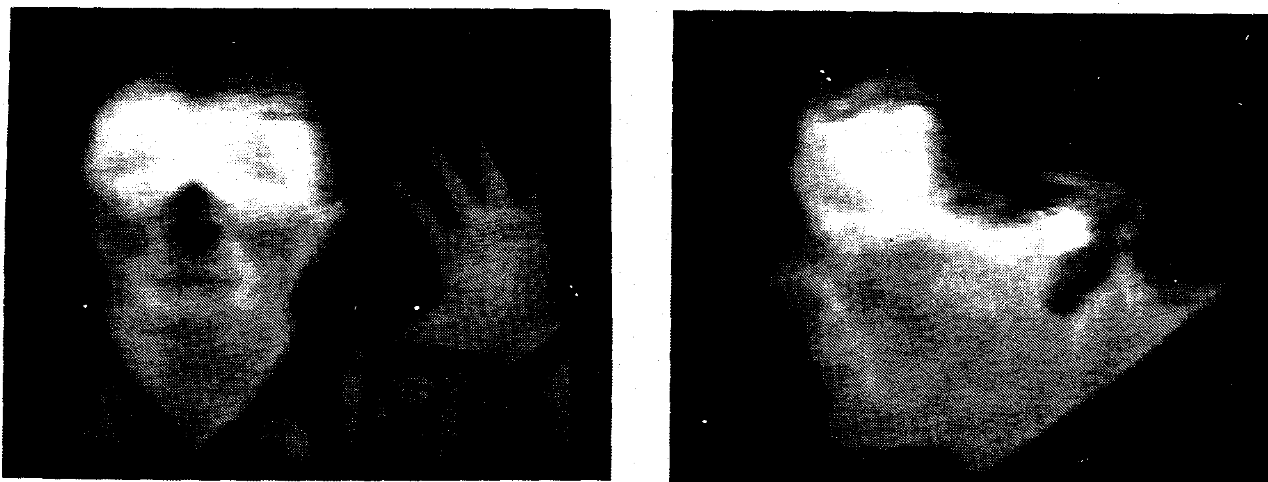
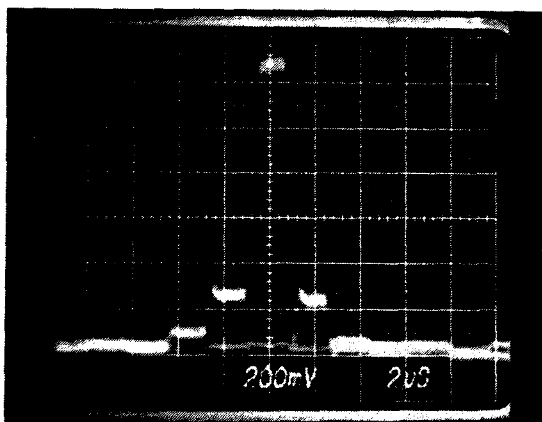
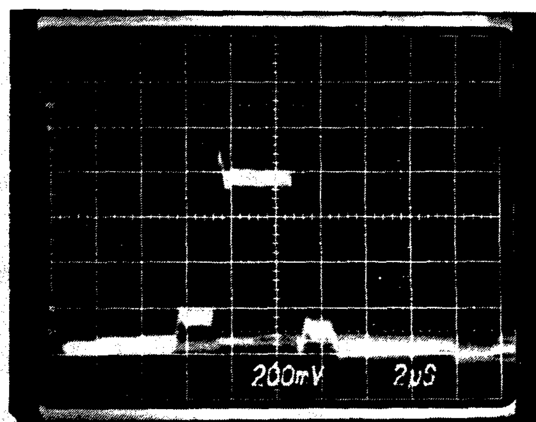


Figure 11. Thermal imaging with the 128 x 128 IT-CCD DSI imager operating at 30 frames/s, f/1.2 optics, one-point uniformity corrector, and a frame converter to a standard 488-line TV format.





Line at Center of Pixel
(a)

Line Between Two Pixels
(b)

Figure 12. Scope traces for the 128 x 128 IT-CCD DSI focal plane array illuminated by a 30-μm-wide vertical line at the center of the 50-μm pixel in (a) and at the border between two pixels in (b).

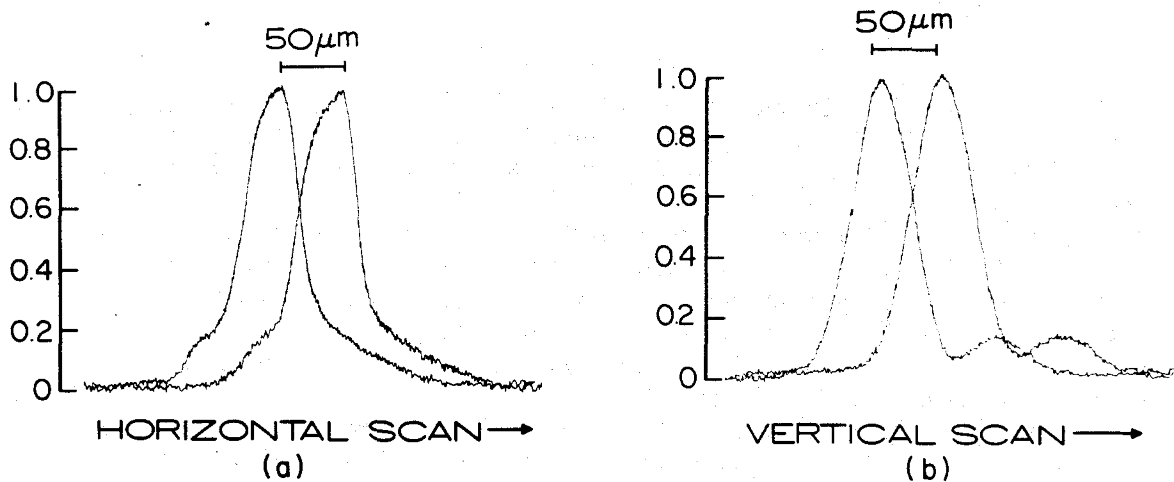


Figure 13. Response of the 128 x 128 IT-CCD DSI imager to a horizontal scan in (a) and vertical scan in (b) by 30-μm lines illuminating the focal plane with a 30-μm blur spot.

5.0 CONCLUSION

A new concept of Direct Schottky Injection was described for a 3-D construction of infrared imagers in the form of a continuous Schottky-barrier-detector surface on one side of a thin (10 to 25 μm) p-type silicon substrate and a p-channel CCD readout formed in N-wells on the other side.

The operation of a 128 x 128-element DSI imager with interline-transfer CCD readout was demonstrated at 30 frames/s and f/1.2 optics. Good quality thermal imaging was obtained with a noise equivalent temperature (NEΔT) of less than 0.1K. The tests also demonstrated that this IT-CCD DSI imager has 100% fill-factor and a cross-talk between pixels of less than 20%.

In addition to 100% fill factor, the DSI imager offers large charge handling capacity due to large capacitance of the charge collecting electrodes. The unique feature of the DSI construction is that it does not require defining or etching of the silicide photodetecting surface that may be an advantage for construction of IrSi FPAs [16].

As a back-illuminated device the PtSi DSI sensor is potentially useful imaging over wide spectral range, including UV (< 0.4 μm), visible (0.4 to 0.7 μm), and MWIR (3 to 5 μm) bands. A smear, however, is expected in the near IR (0.7 to 1.0 μm) band due to the long absorption length of radiation in silicon that would lead to some generation of holes in the N-wells containing the p-channel CCD readout structure.

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