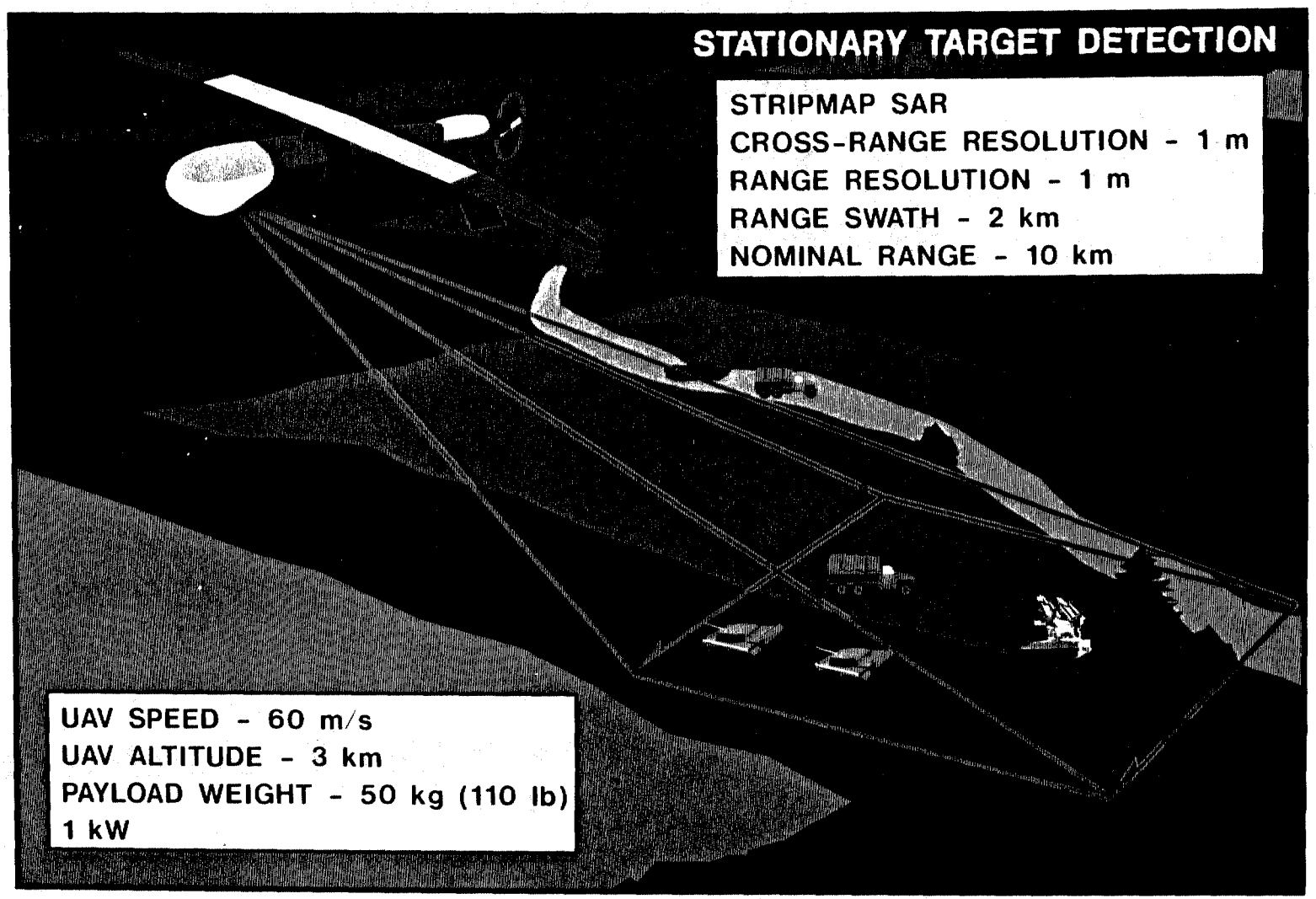
APPLICATION OF CCD TECHNOLOGY
TO
HIGH SPEED SAMPLED ANALOG SIGNAL PROCESSING

J. Strombosky, R. Whiting, C. Christensen,
D. McClure, R. Wixted
Lincoln Laboratory, M.I.T.
Lexington, MA

OUTLINE

- APPLICATIONS AND EXAMPLES
- SYSTEM REQUIREMENTS
- CRITICAL DESIGN ISSUES
- EXPERIMENTAL RESULTS
- TECHNOLOGY DEVELOPMENT

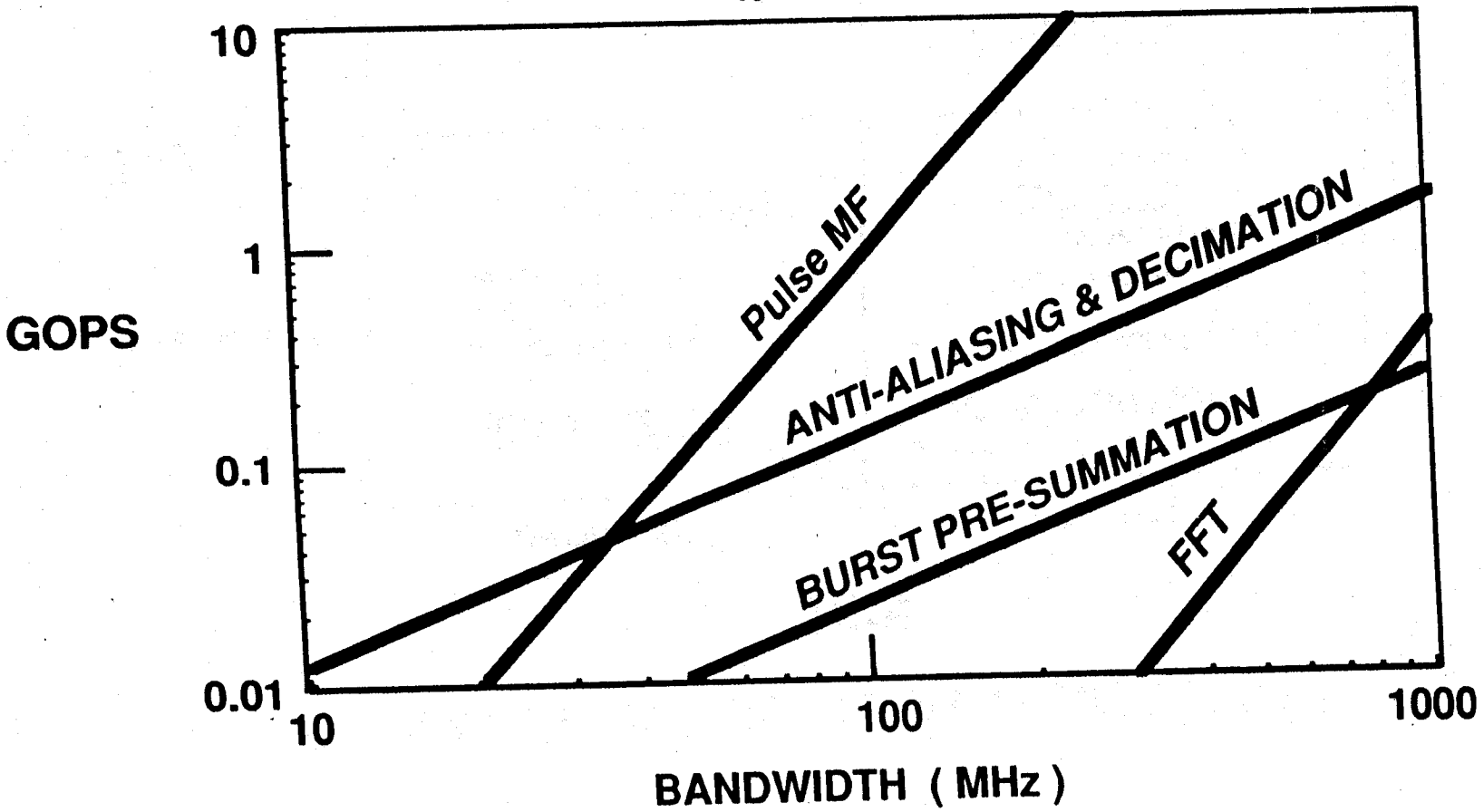
UAV SYNTHETIC APERTURE RADAR MODE



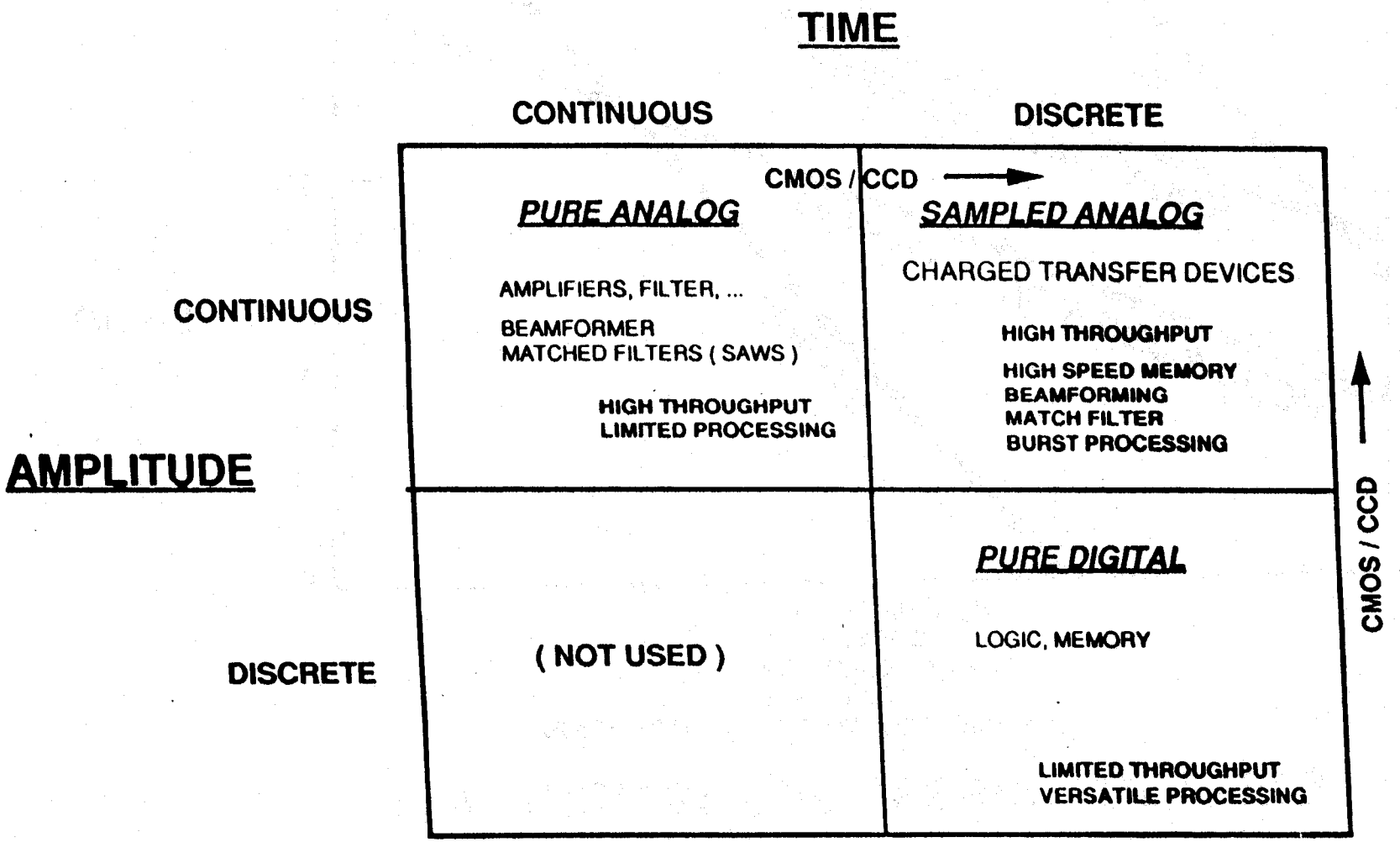
179231-1

UAV - DIGITAL PROCESSING OPTIONS

Assumptions: 10 μ sec PULSEWIDTH
PRF = 4000
2 K RANGE SWATH
3K ALTITUDE
60 M/SEC VELOCITY



SIGNAL PROCESSING ALTERNATIVES



CCD SIGNAL PROCESSING CHARACTERISTICS

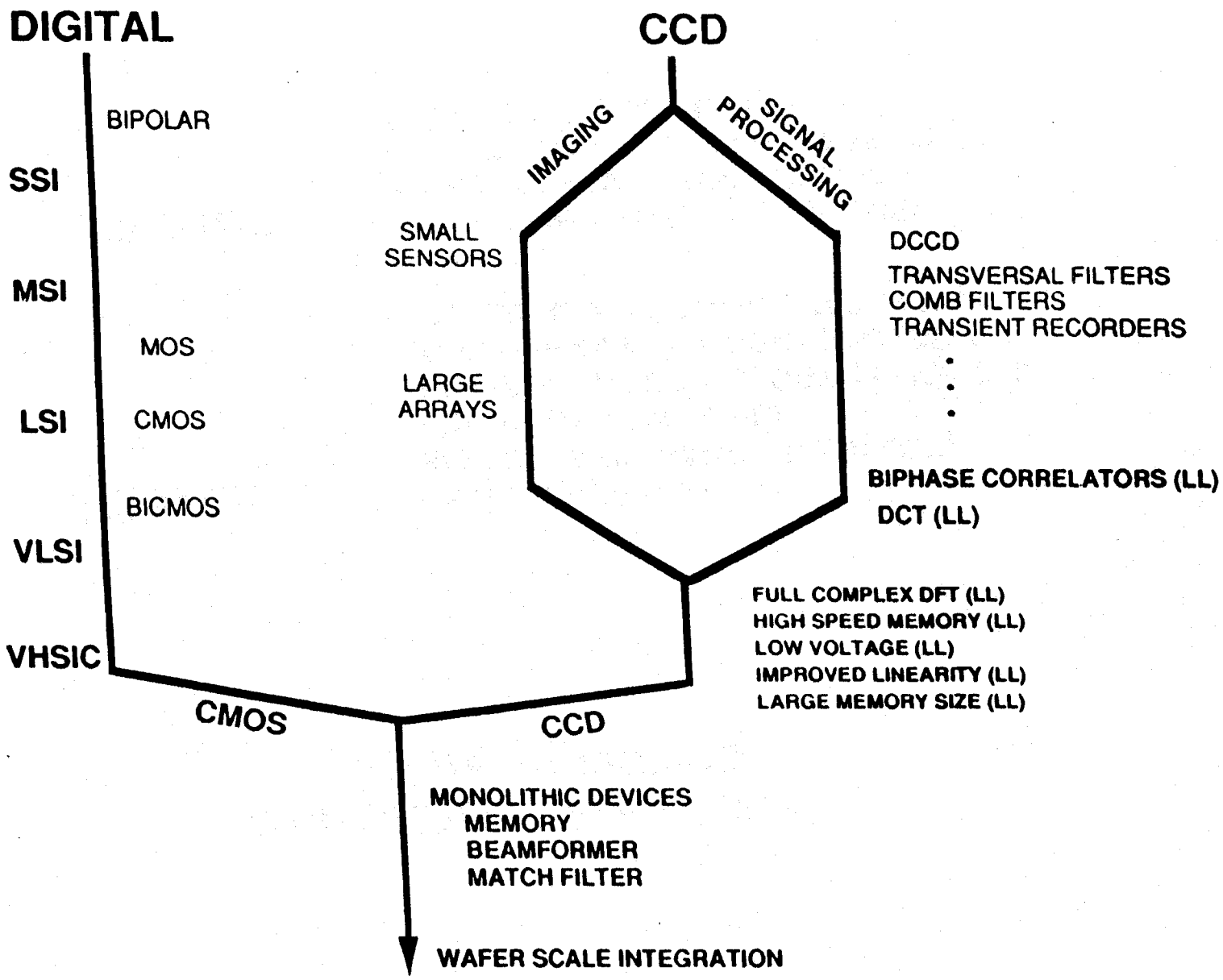
STRENGTHS:

- HIGH THROUGHPUT
- HIGH DENSITY (SAMPLED ANALOG)
- LOW POWER AND WEIGHT
- INTEGRATED TECHNOLOGY (CMOS/CCD)
- CONVENTIONAL SILICON PROCESSES
- COMMERCIALLY DRIVEN TECHNOLOGY

LIMITATIONS:

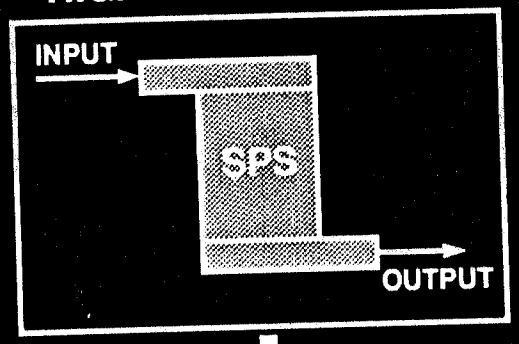
- LOW DYNAMIC RANGE AND LINEARITY
- SHORT SIGNAL STORAGE TIMES
- LIMITED MATHEMATICAL VERSATILITY
- MASK PROGRAMMABLE

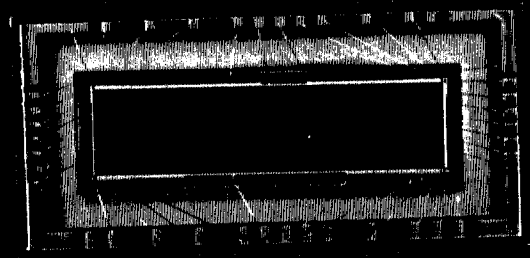
TECHNOLOGY EVOLUTION



CCD SIGNAL PROCESSING TECHNOLOGY

HIGH SPEED MEMORY

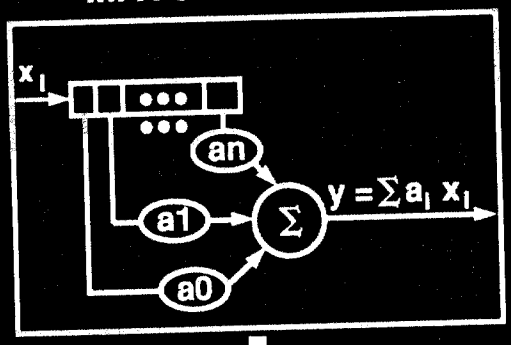


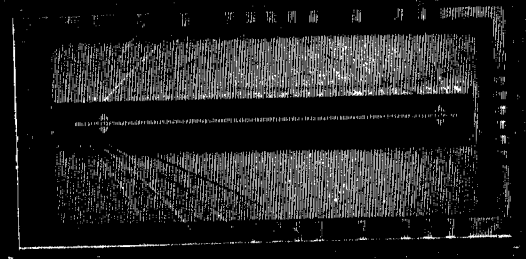


SERIAL PARALLEL SERIAL SHIFT REGISTER

- 150-200 MHz INPUT
- 64-K SAMPLE STORAGE
- > 55 dB DYNAMIC RANGE
- LINEARITY > 8 BITS (Full Diff)
- > 1-SECOND DWELL

MATCHED FILTER

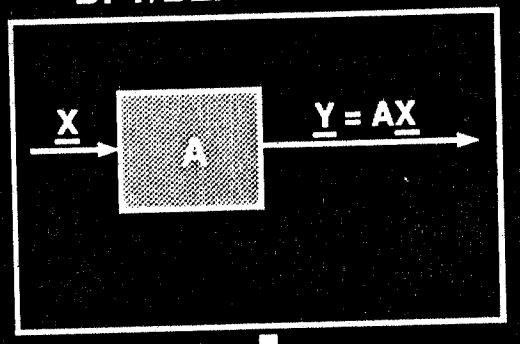


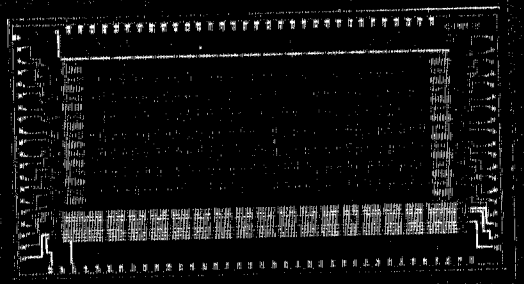


TRANSVERSAL FILTER

- BI-PHASE CORRELATOR
- CHIP LENGTH 512/1024
- 10-20 MHz/10-20 BOPS
- LINEARITY > 7 BITS
- CMOS CIRCUIT INTEGRATION

DFT/BEAMFORMER





VECTOR MATRIX PRODUCT

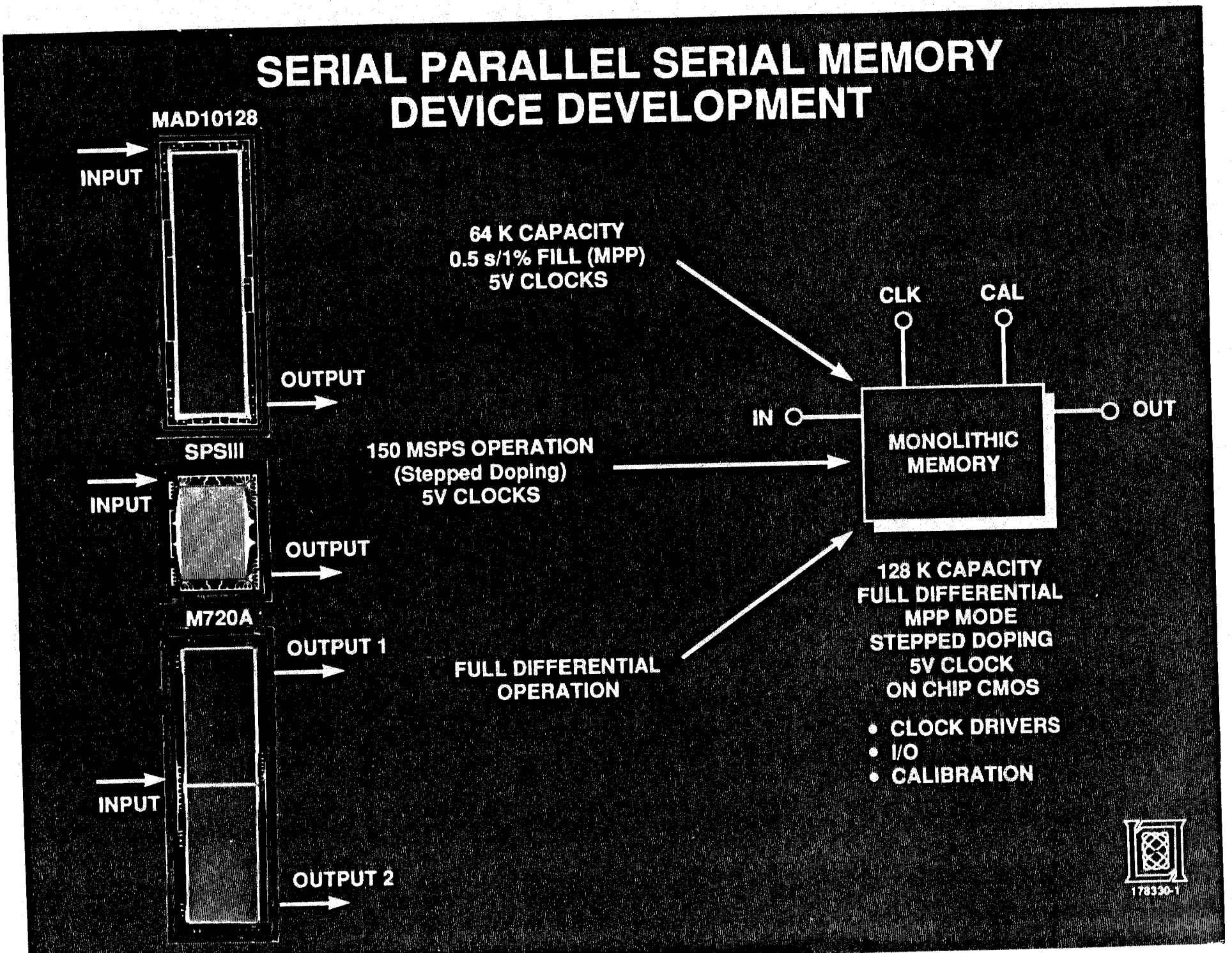
- FULL DIFFERENTIAL DFT
- 10-20 MHz/10-20 BOPS
- > 50-dB DYNAMIC RANGE
- LINEARITY > 8 BITS (Full Diff)
- CMOS CIRCUIT INTEGRATION

178586-3

SPS MEMORY REQUIREMENTS

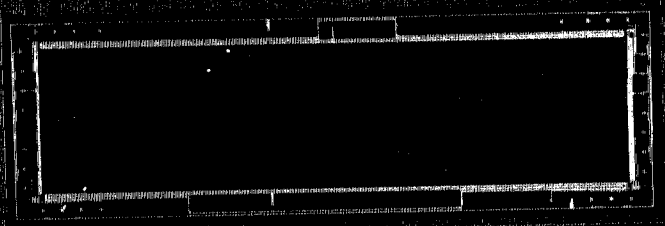
- LARGE STORAGE SIZE (>128K)
- 150-200MSPS INPUT RATE
- 10MSPS OUTPUT RATE
- >100mS DWELL-TIME (<1% FILL)
- > 50dB LINEAR RANGE
- LOW POWER
- SELF CONTAINED/MONOLITHIC

SERIAL PARALLEL SERIAL MEMORY DEVICE DEVELOPMENT

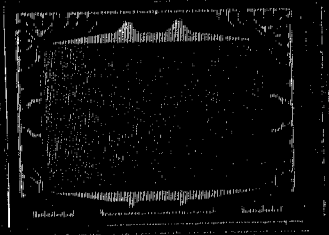


SERIAL PARALLEL SERIAL MEMORY DEVICES

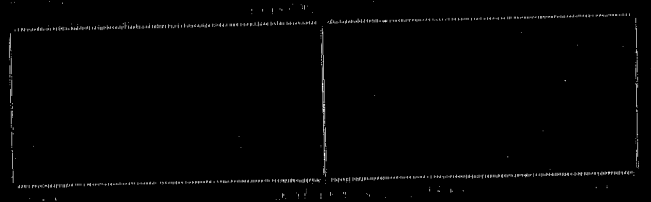
MAD20128



SPS III



M720A



MAD20128

- 64K CAPACITY
- 2 POLY
- SINGLE METAL
- BORON/PHOSPHORUS
- ON CHIP NMOS CLOCK DRIVERS

SPS III

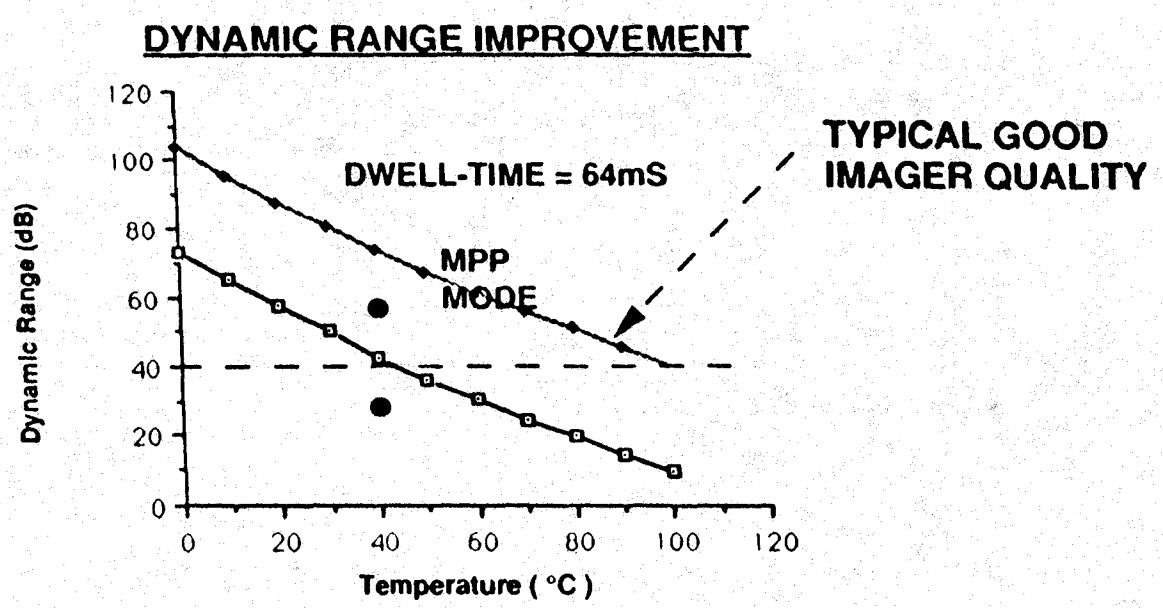
- 16K CAPACITY
- 3 POLY
- SINGLE METAL
- ALL PHOSPHORUS
- STEPPED DOPING
- ON CHIP NMOS CLOCK DRIVERS

M720

- 2 X 32K CAPACITY
- 2 POLY
- SINGLE METAL
- ALL PHOSPHORUS
- FULL DIFFERENTIAL

178586-4

HIGH-SPEED SPS BUFFER MEMORY
MULITPHASE-PINNED MODE OF OPERATION

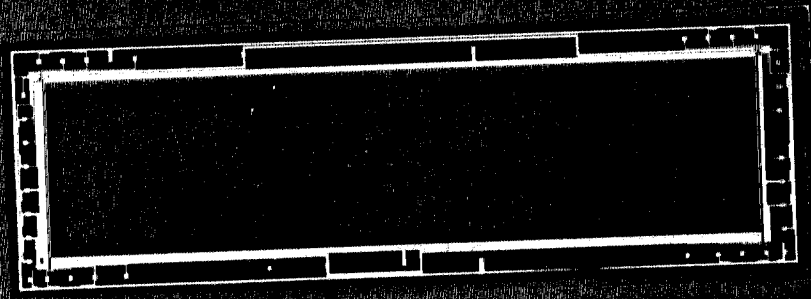


- SUBSTRATE TEMP RANGE INCREASE FROM 40 TO 100°C
- LOW STANDBY POWER VIA CMOS MPP CLOCK DRIVERS

HIGH SPEED MEMORY

REQUIREMENTS

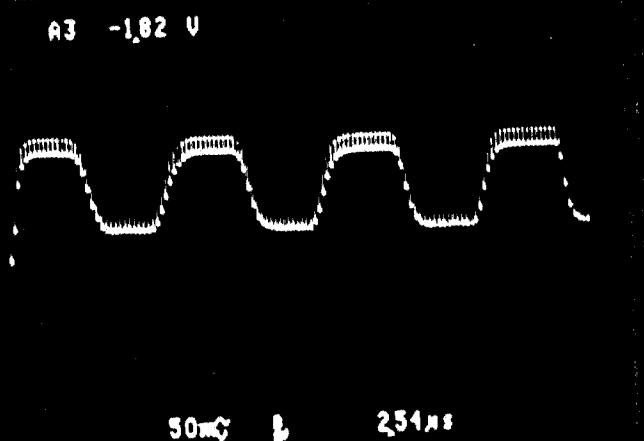
- 150 - 200 MHz SAMPLING
- 64K SINGLE CHIP
- MONOLITHIC STRUCTURE (Low Power)



64K MEMORY DIE

ACHIEVEMENTS

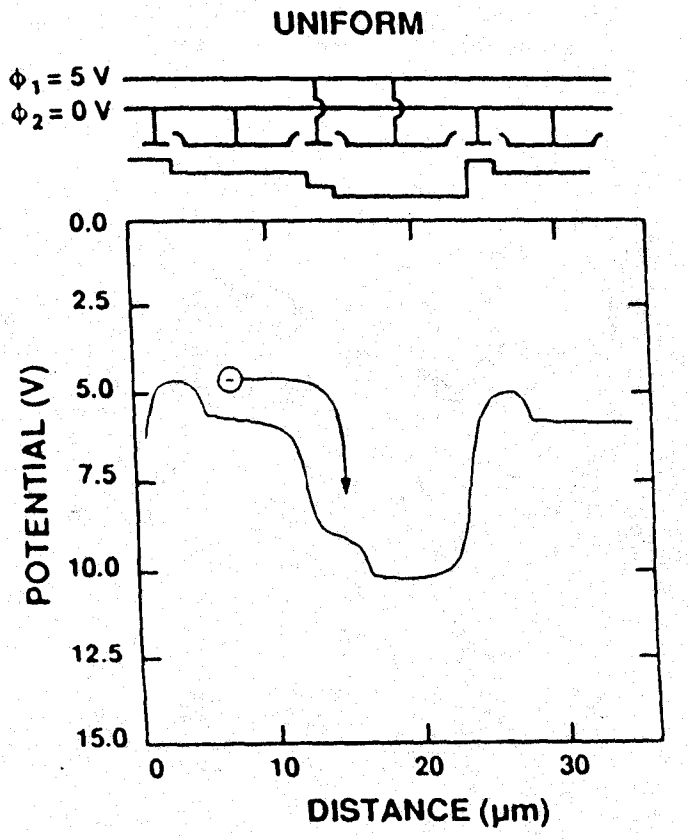
- 150 - 200 MHz SAMPLING
- 64K SAMPLES
- 35 dB SINGLE ENDED
- 45 dB FULL DIFFERENTIAL



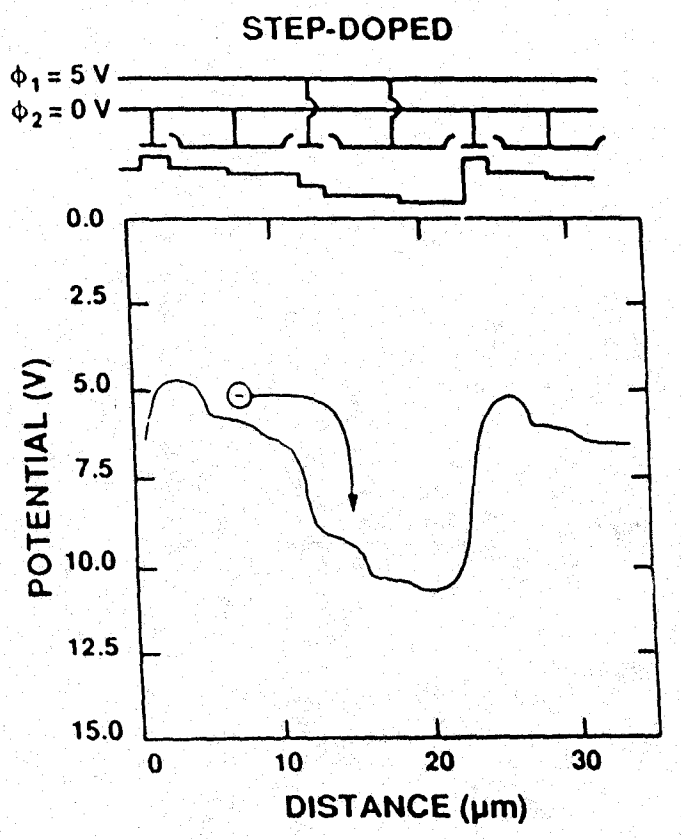
150 MSPS SAMPLING

178586-2

SHORT-GATE CCDs: L = 7 μm



SINGLE ELECTRON TRANSIT
TIME = 0.8 ns

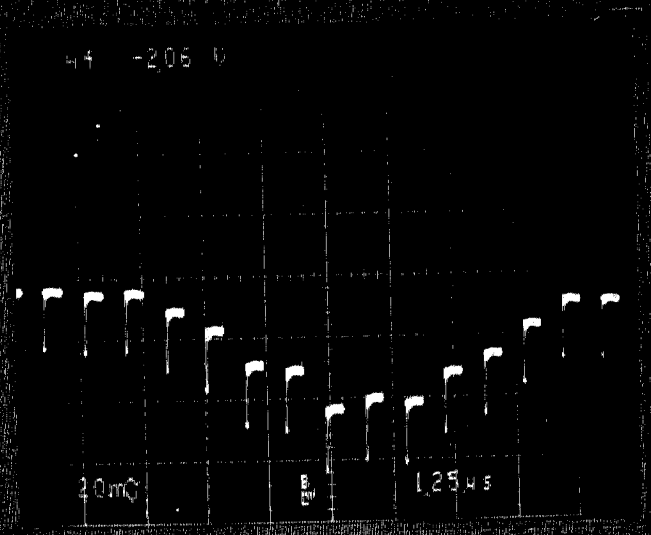


SINGLE ELECTRON TRANSIT
TIME = 0.45 ns

162575-1

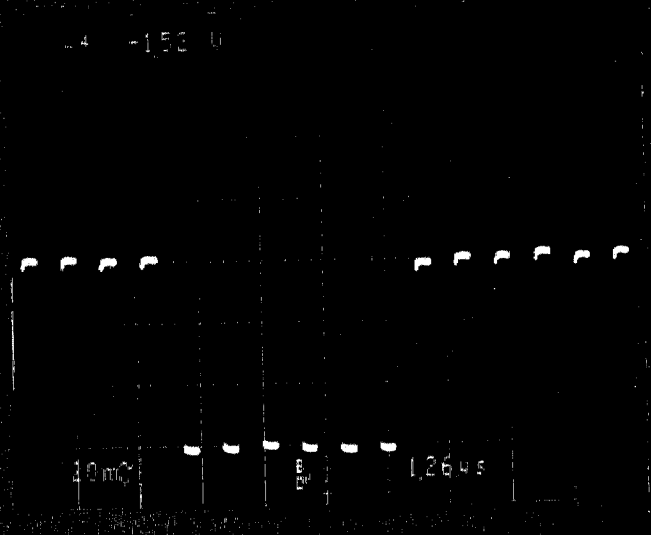
CCD BUFFER MEMORY SPEED ENHANCEMENTS

UNIFORM DOPING



(150MSPS, CTE = 0.95)

STEPPED DOPING

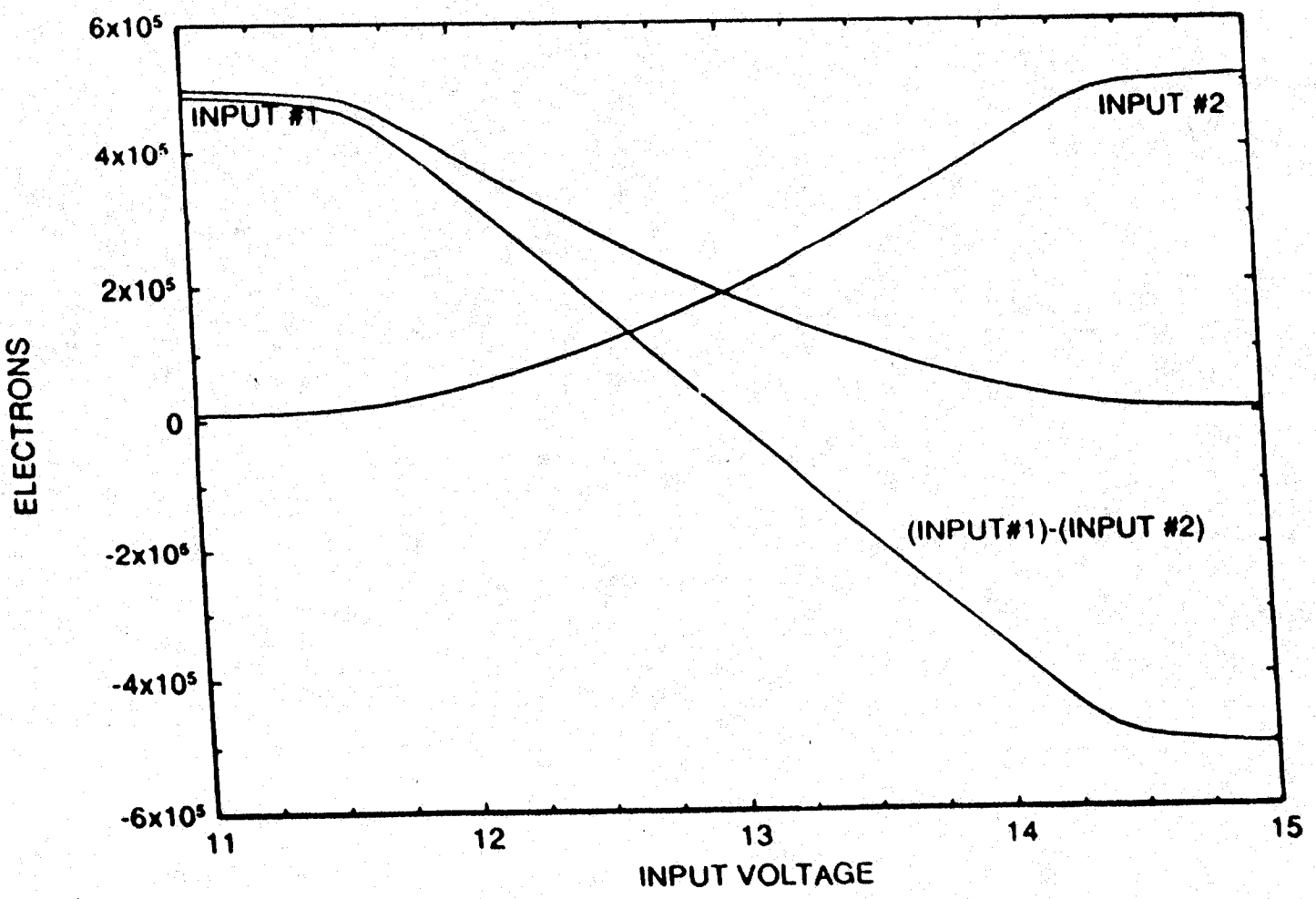


(150MSPS, CTE = 0.9999)

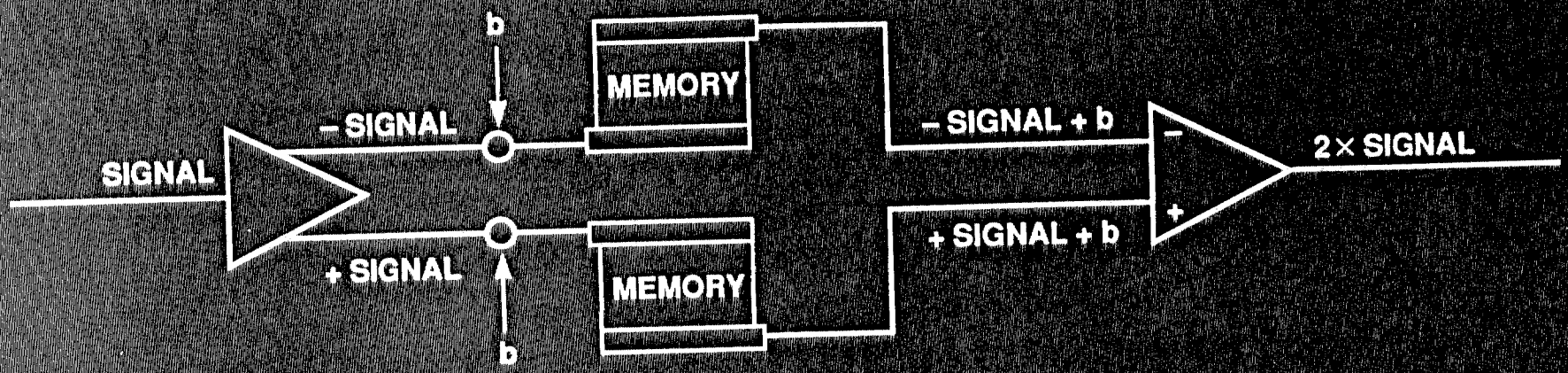
- IMPROVED CHARGE TRANSFER EFFICIENCY ACHIEVED USING NON-UNIFORM ION IMPLANTS
- DRIFT FIELD ENHANCEMENT ALLOWS FOR CMOS CLOCK LEVELS WHILE MAINTAINING REQUIRED SPEED

176586-1

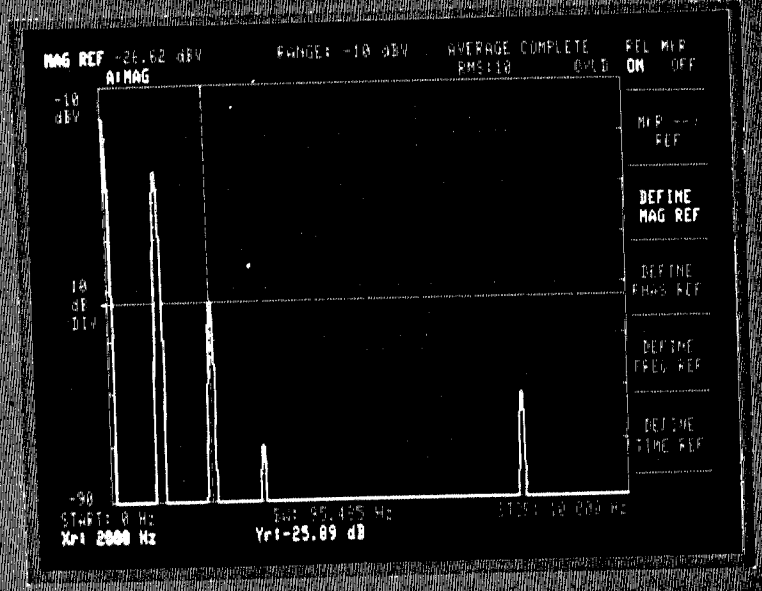
DIFFERENTIAL OPERATION LINEARITY ANALYSIS



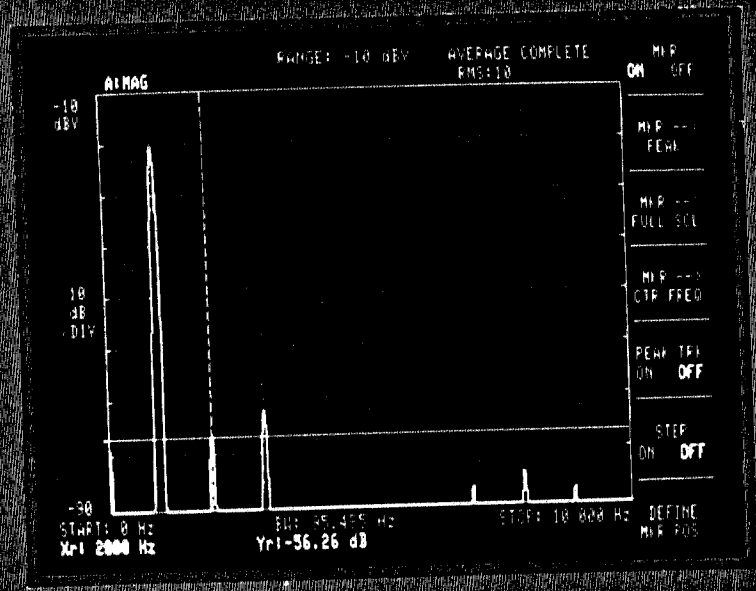
FULL DIFFERENTIAL SPS MEMORY ARCHITECTURE



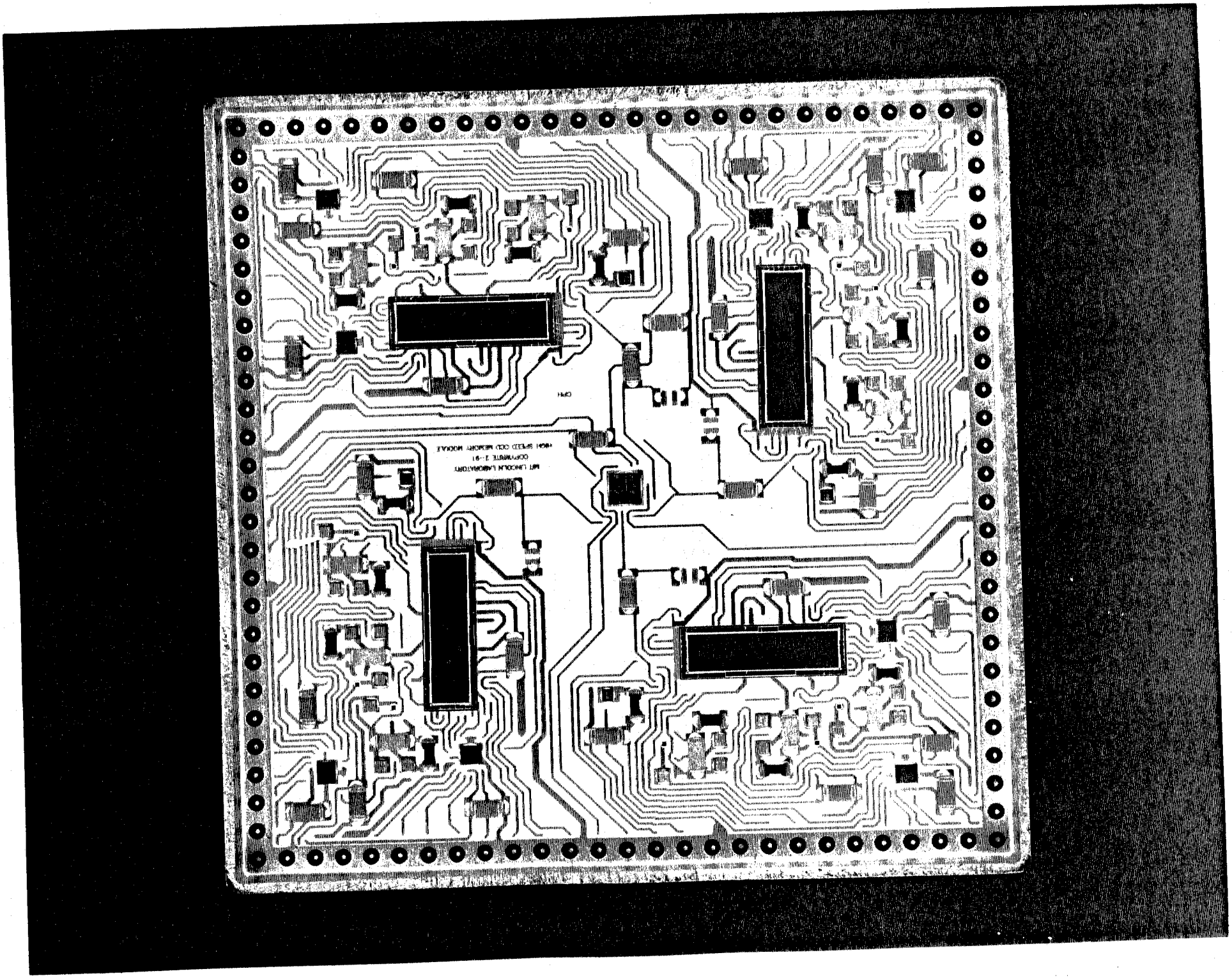
SINGLE ENDED SPS SPECTRUM



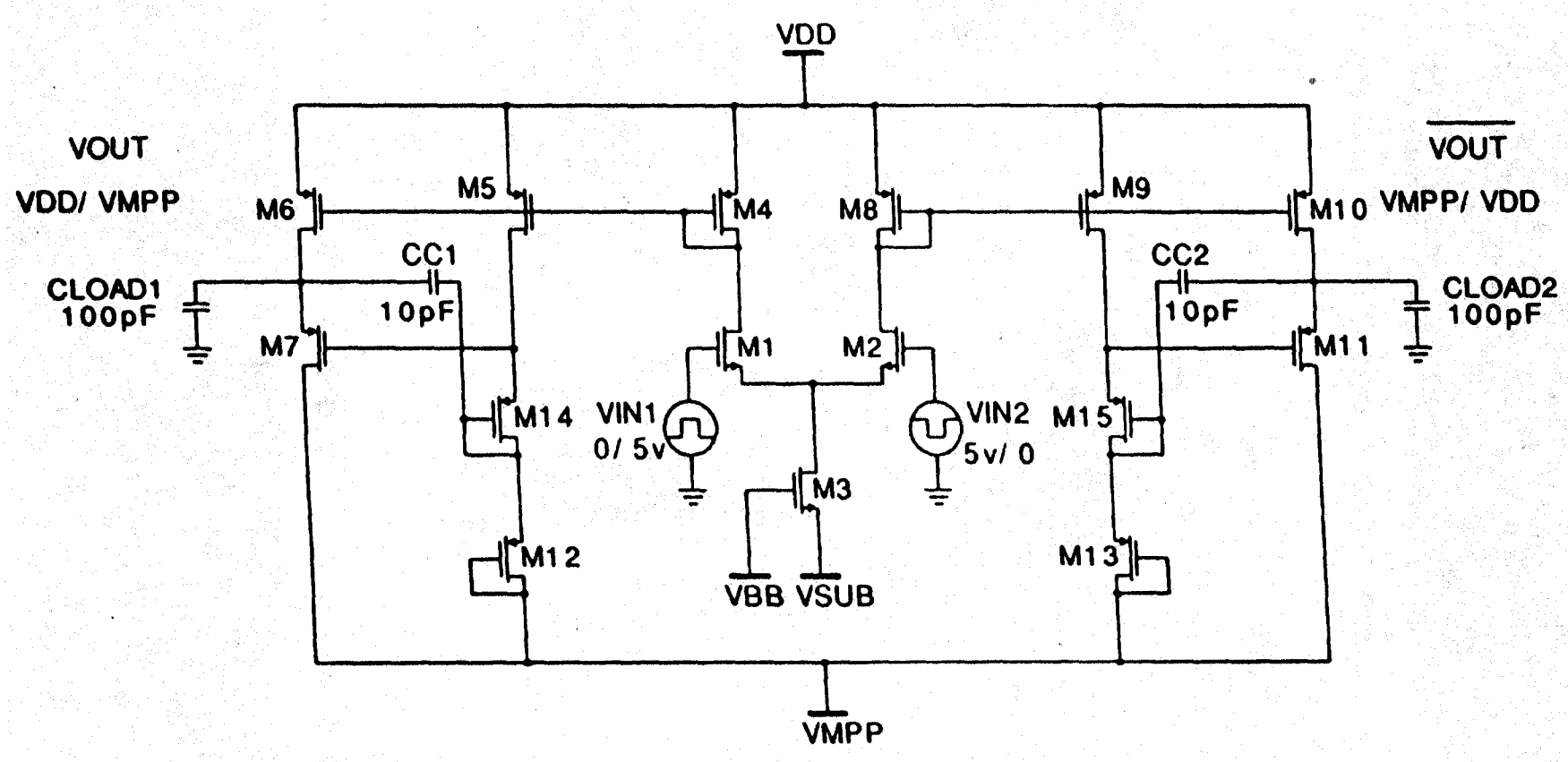
FULL DIFFERENTIAL SPS SPECTRUM



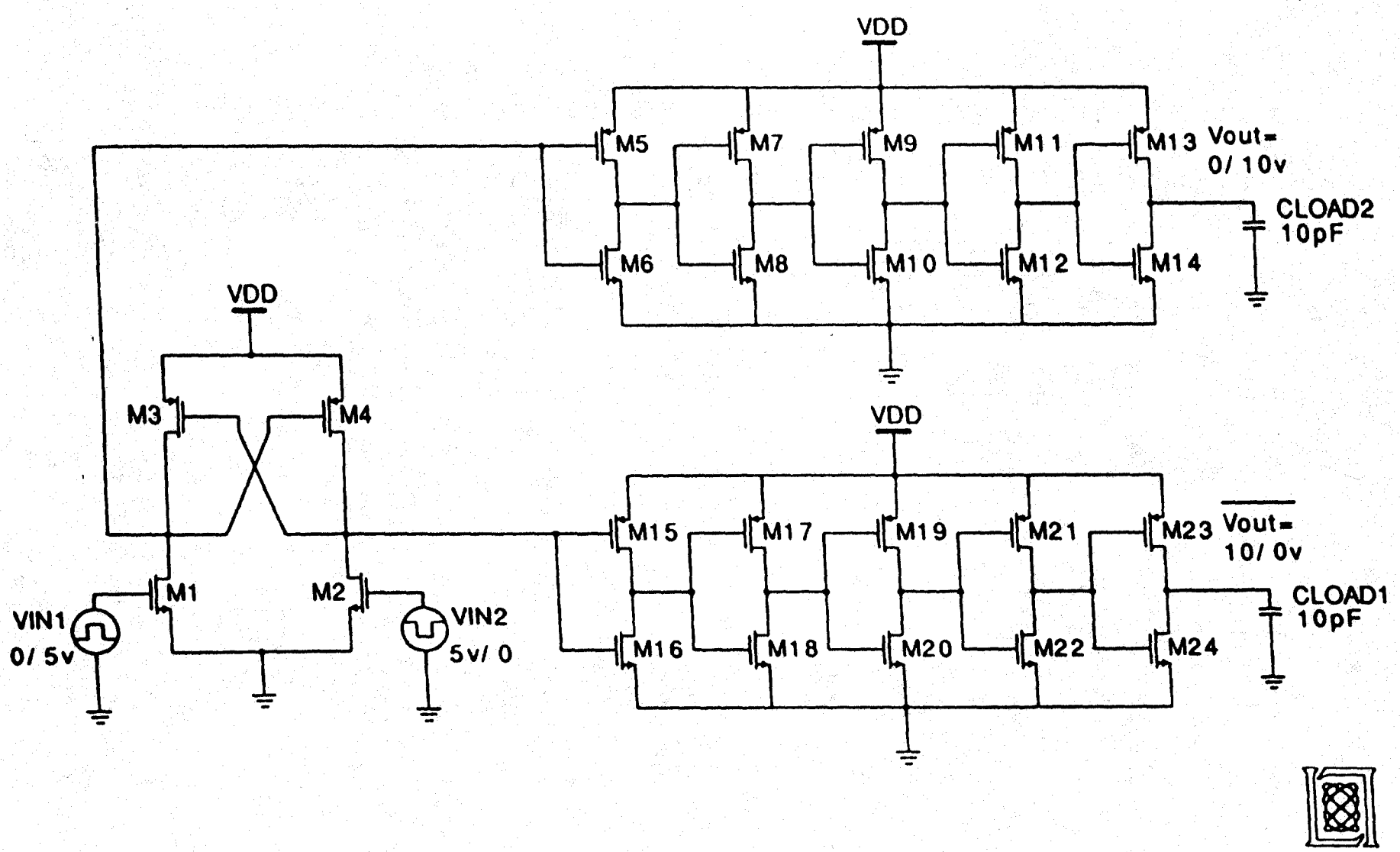
189605-2

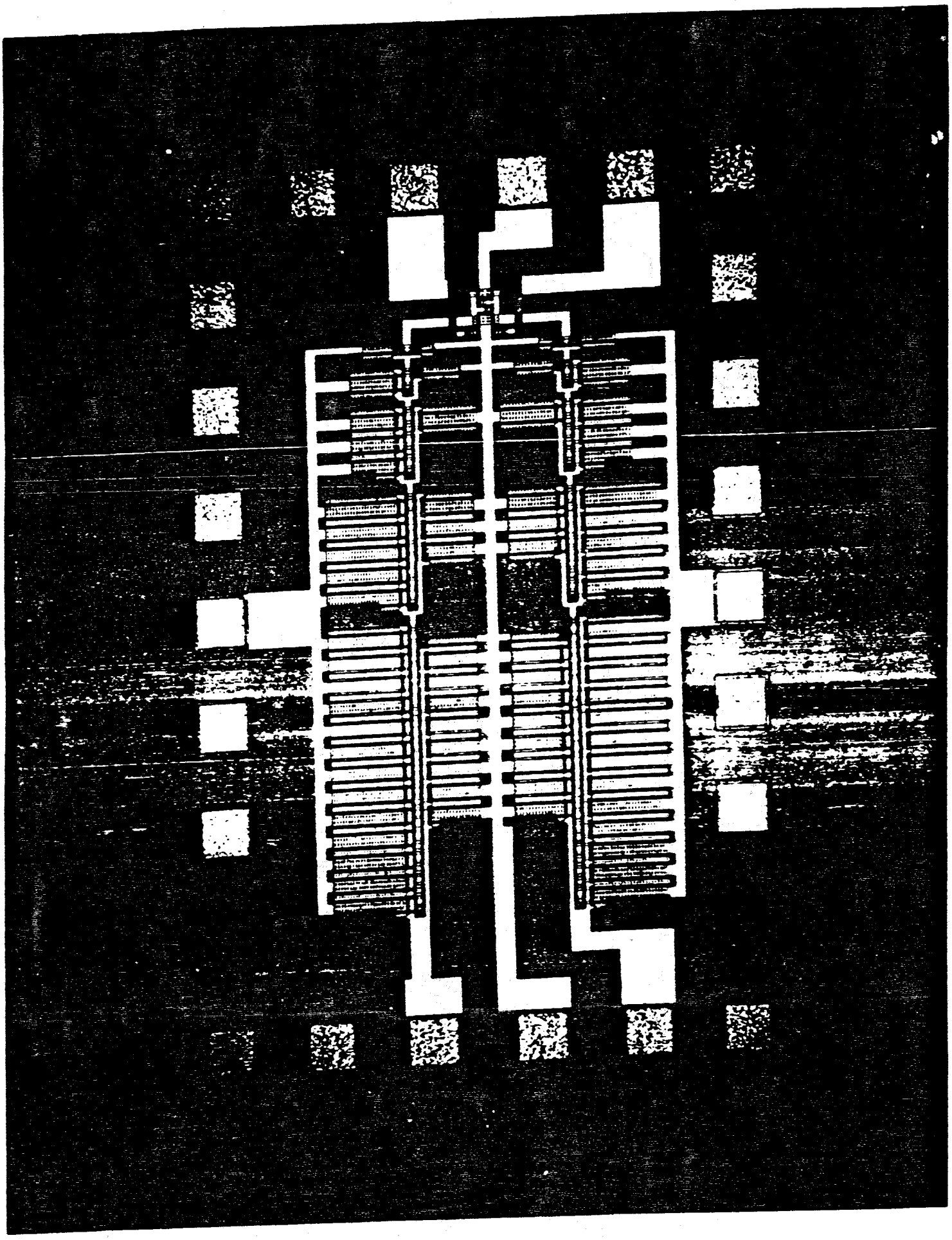


CMOS MPP DIFFERENTIAL CLOCK DRIVER

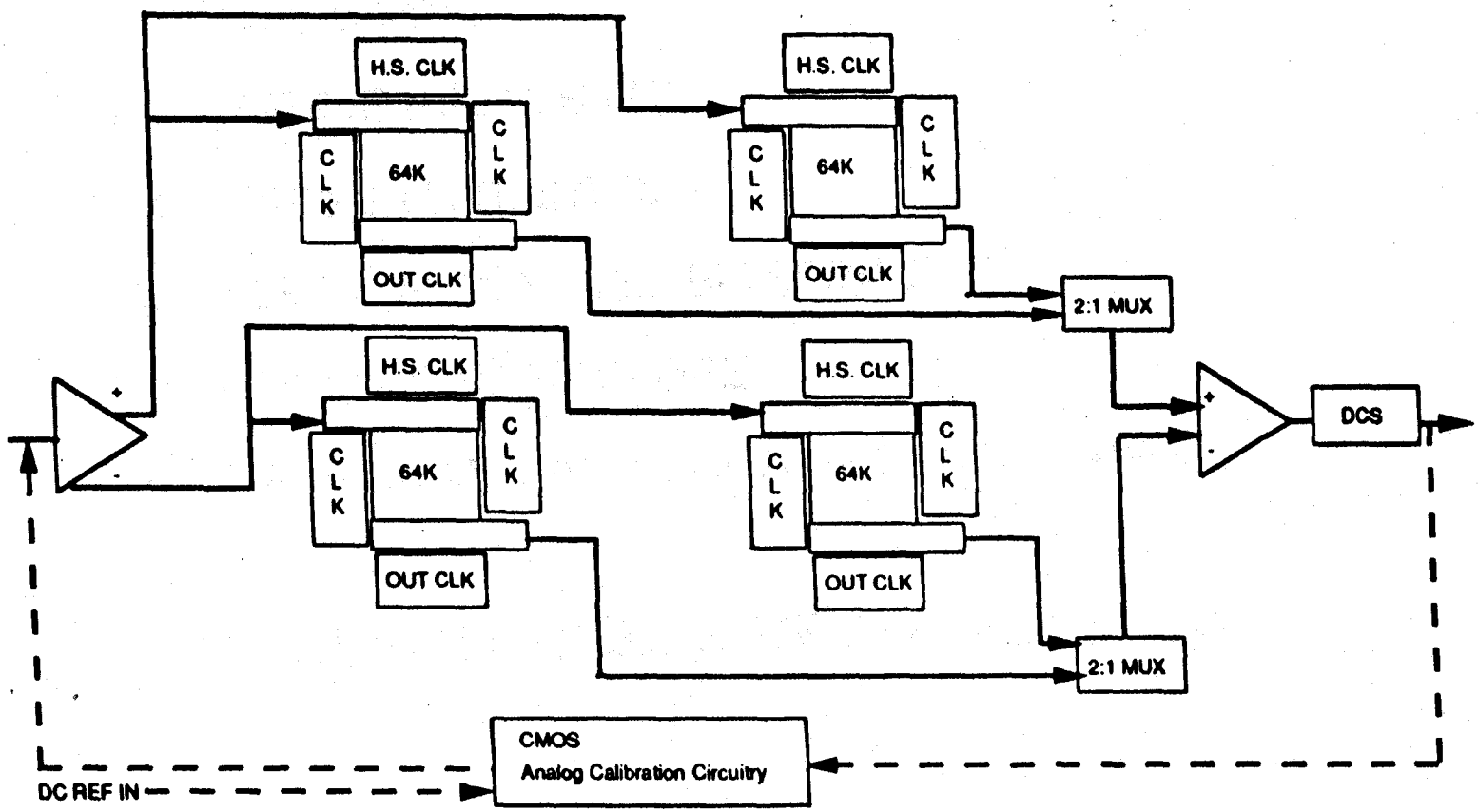


CMOS HIGH SPEED DIFFERENTIAL CLOCK DRIVER





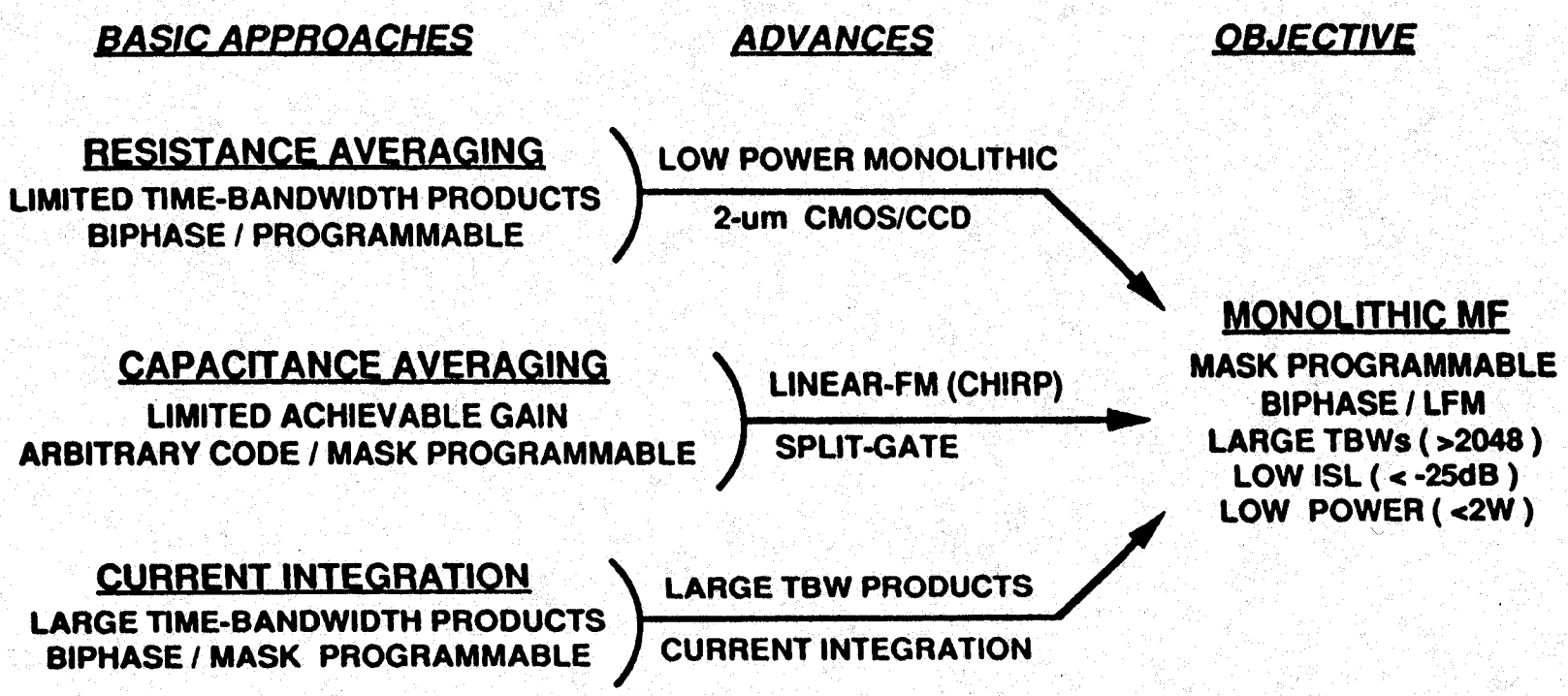
HIGH-SPEED SPS MONOLITHIC MEMORY



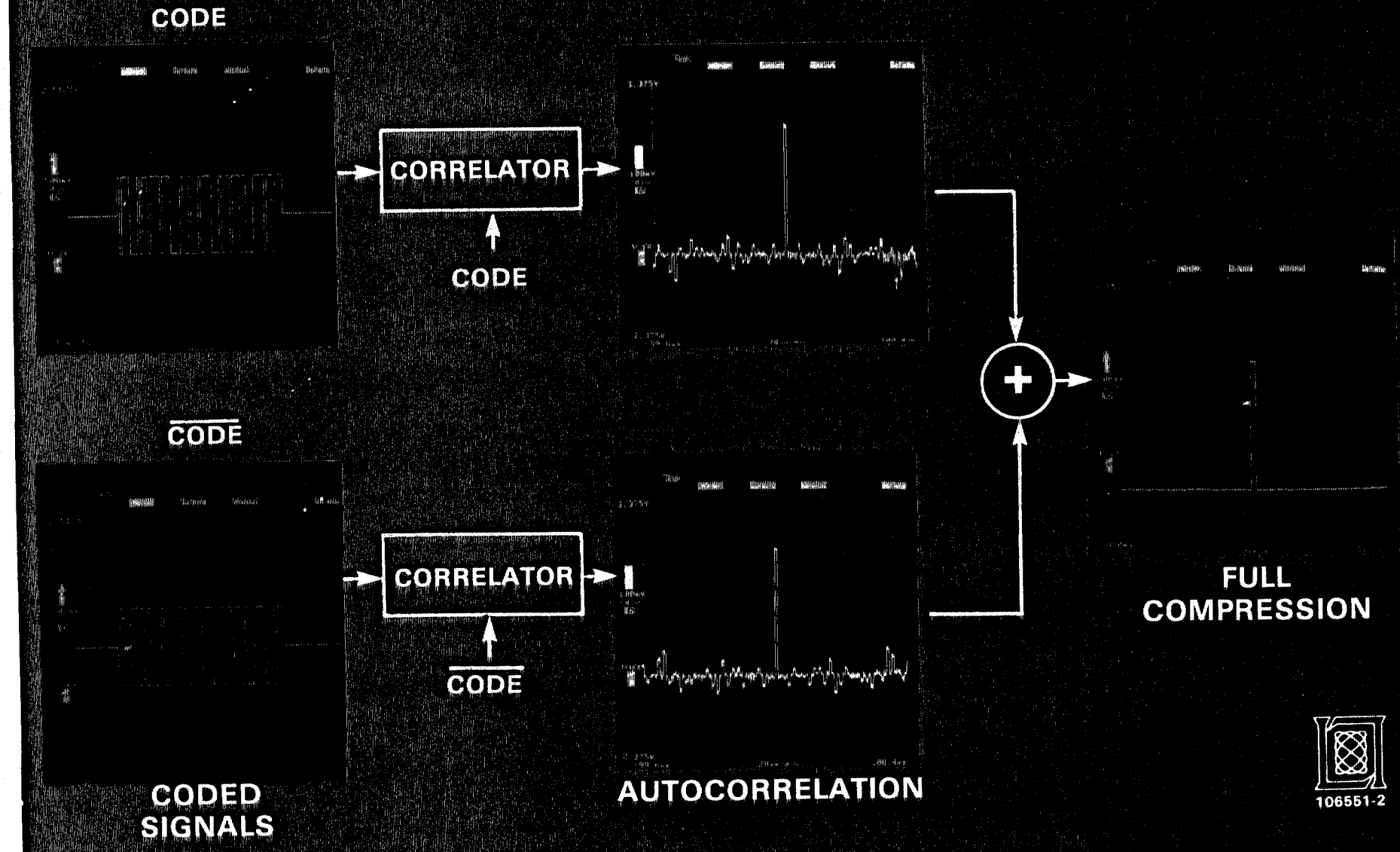
MATCHED FILTER REQUIREMENTS

- LARGE TIME-BANDWIDTH PRODUCT (>1024)
- > 50dB PEAK/SIDELOBE
- > 25dB INTEGRATED SIDELOBE
- LINEAR-FM/BIPHASE
- 10MSPS INPUT RATE
- LOW POWER
- SELF CONTAINED/MONOLITHIC

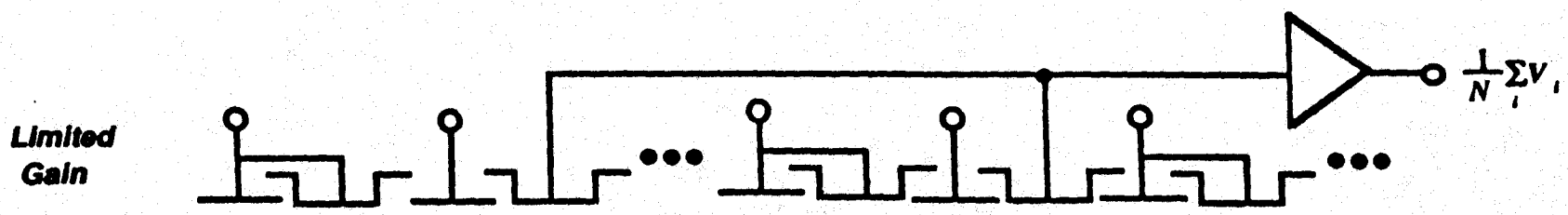
MATCHED FILTER DEVELOPMENT OVERVIEW



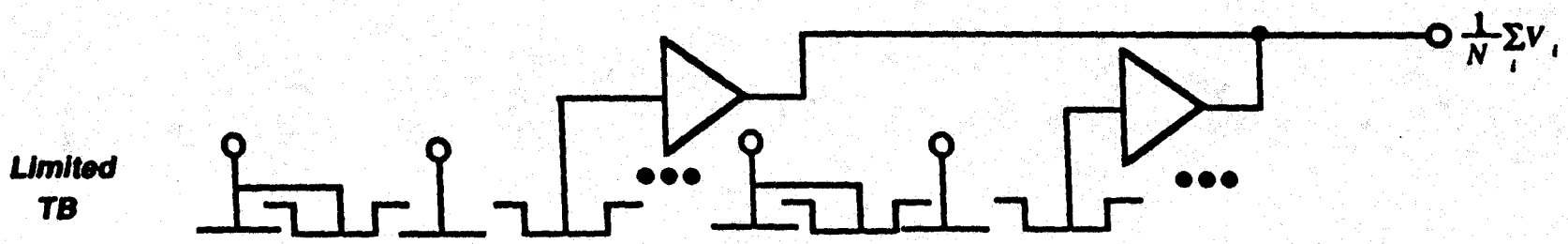
CCD ANALOG/BINARY MATCH FILTER



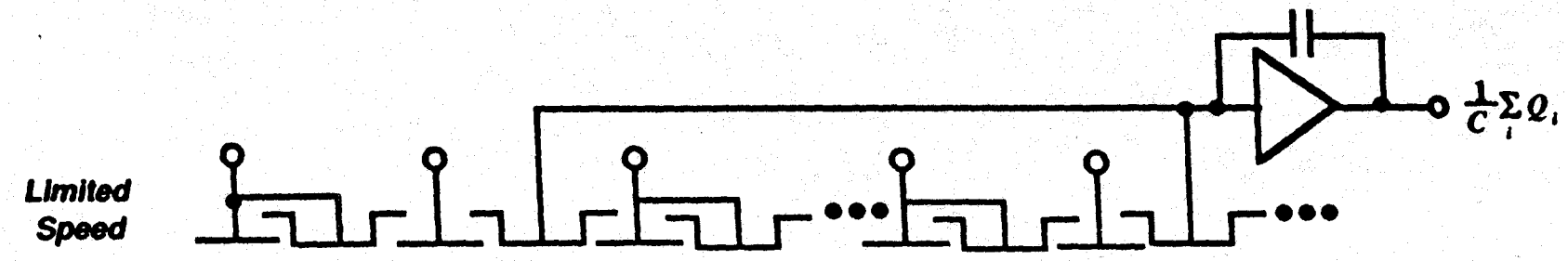
CCD TRANSVERSAL FILTER IMPLEMENTATIONS



(CAPACITIVE AVERAGING)

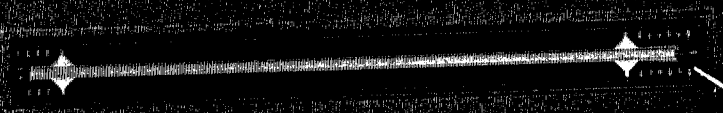


(TRANSCONDUCTANCE AVERAGING)

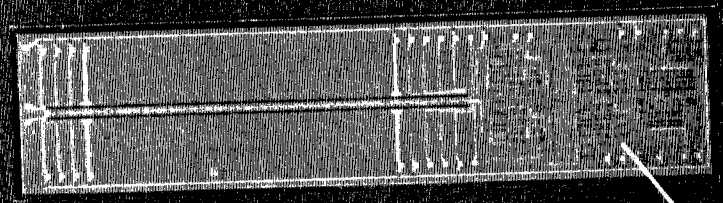


(DIRECT CURRENT INTEGRATION)

CCD BIPHASE MATCHED FILTERING

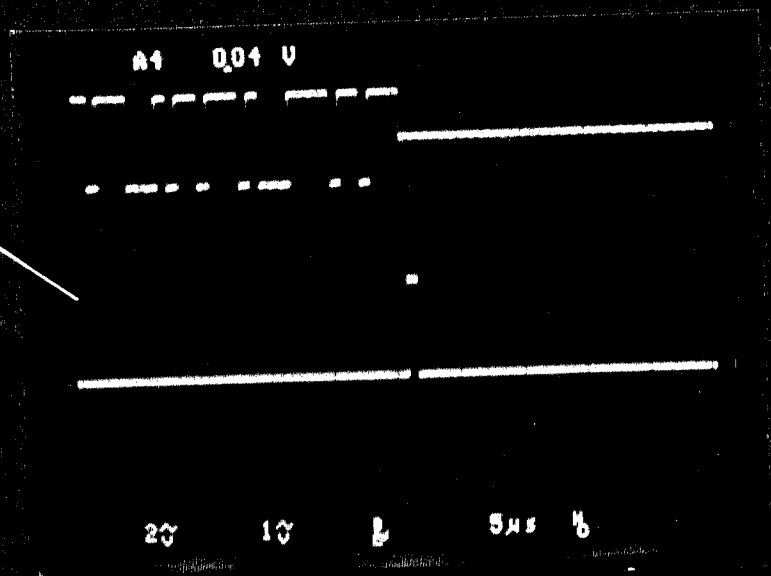


CCD/NMOS IMPLEMENTATION



CCD/CMOS IMPLEMENTATION

ON CHIP
CMOS ANALOG
CIRCUITRY



N = 512 GOLAY CODE MATCHED FILTER

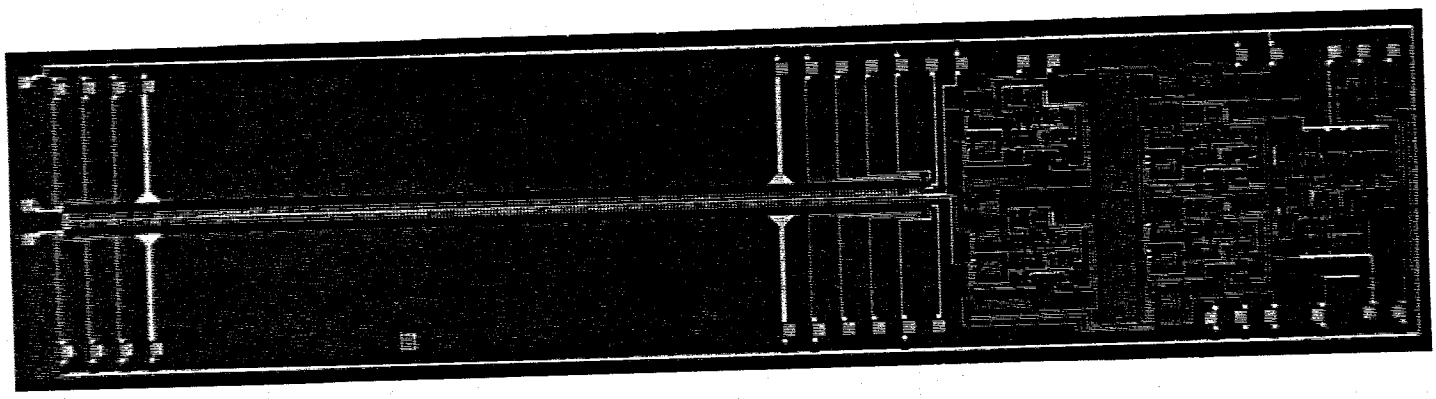
DESIGN APPROACH

- DIFFERENTIAL CURRENT SENSING
- FLOATING GATE/CURRENT MODE
- CONCEPT EXPANDABLE TO INCORPORATE LINEAR (Nonlinear) FM

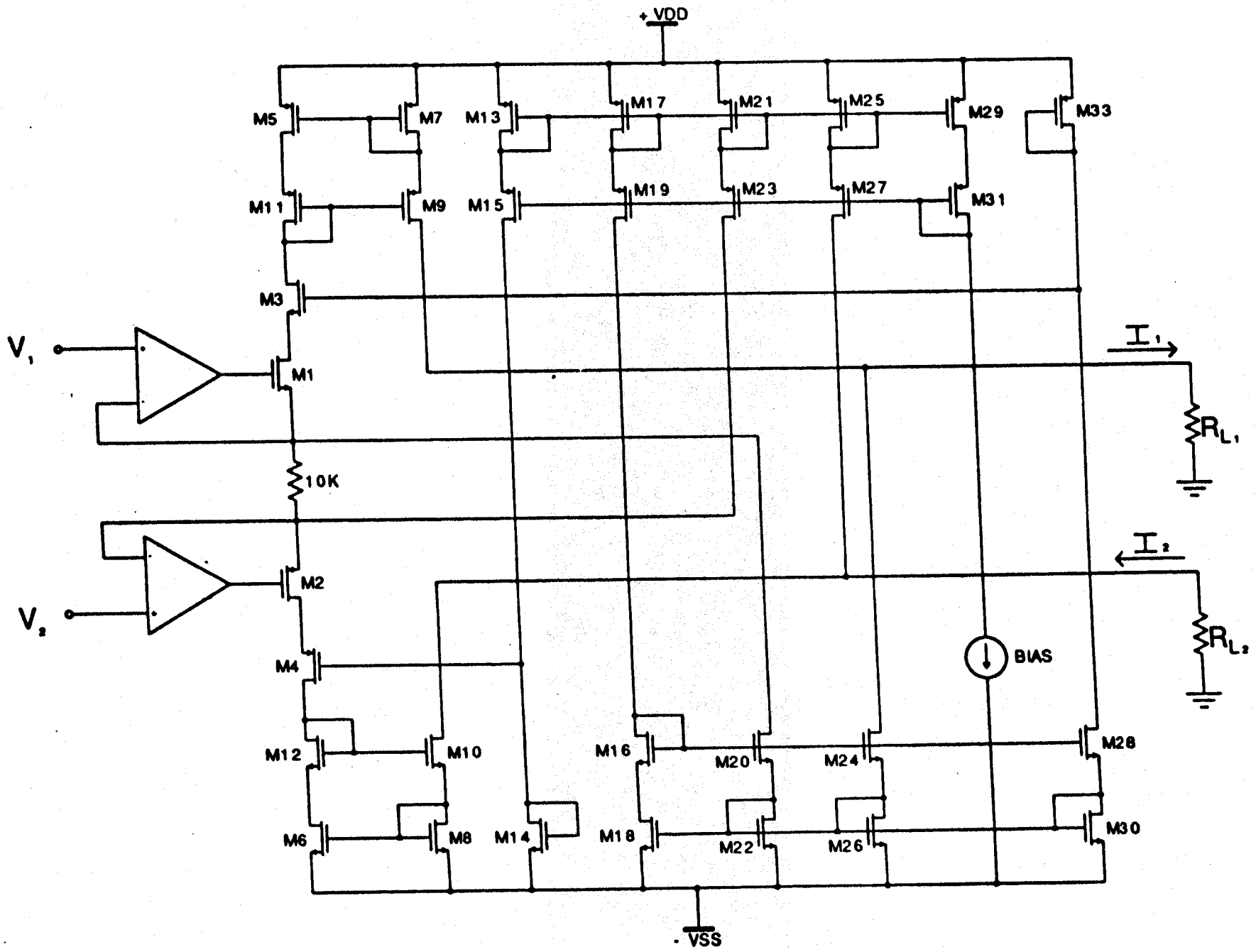
TEST RESULTS

- 50 dB S/N
- 40 dB LINEARITY
- 60 dB DYNAMIC RANGE
- 25 dB ISL

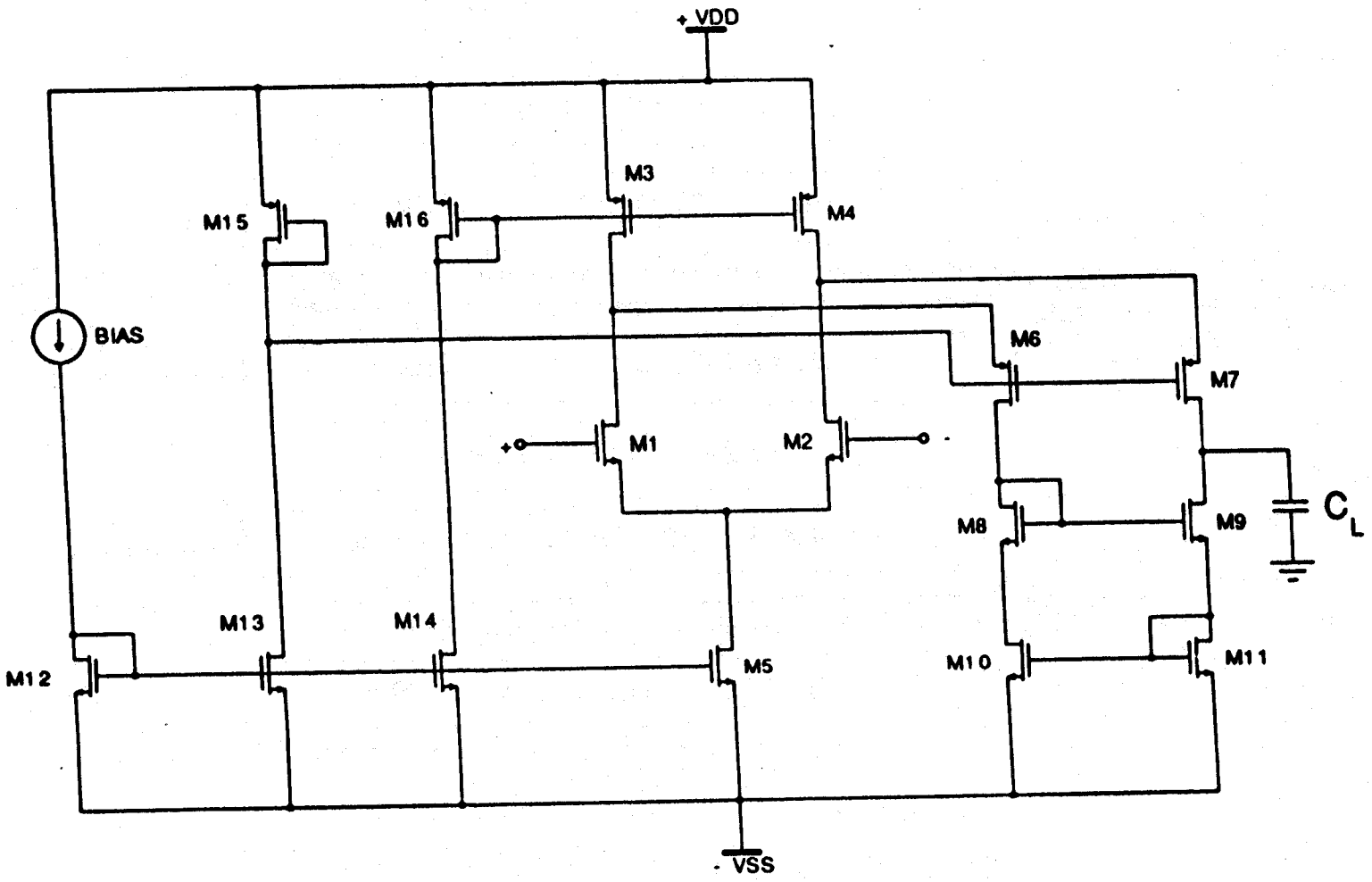
170087-3



CMOS INSTRUMENTATION AMPLIFIER

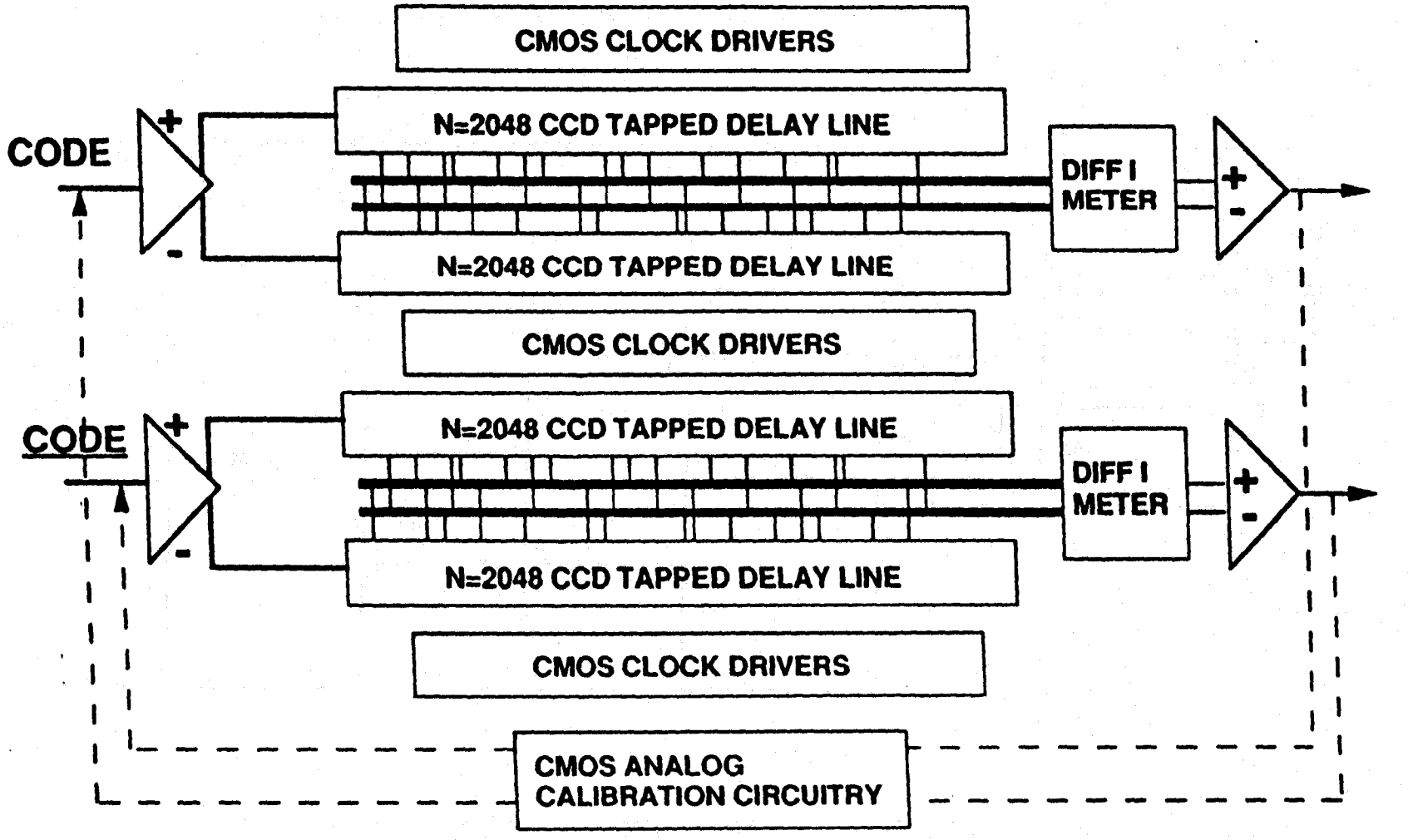


CMOS FOLDED- CASCODE OPAMP



UNCLASSIFIED

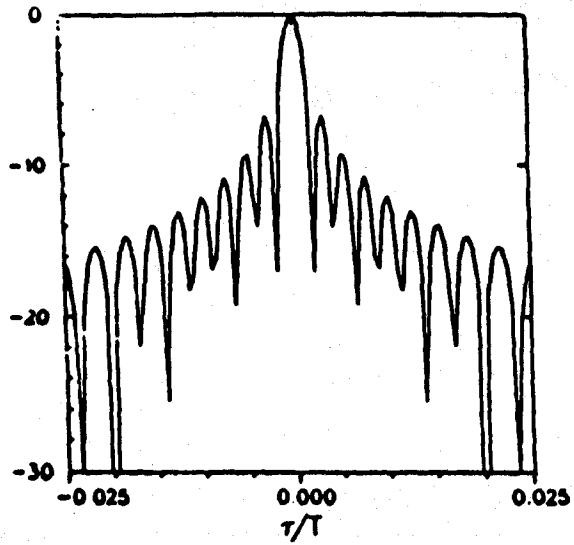
MONOLITHIC MATCHED FILTER



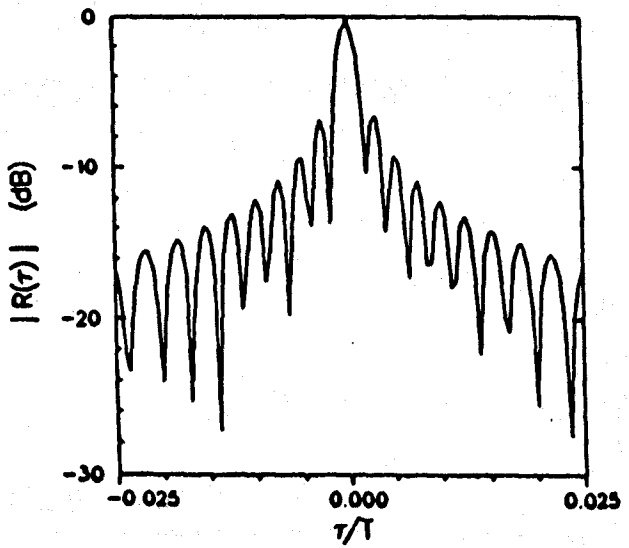
UNCLASSIFIED

2000 WELLS

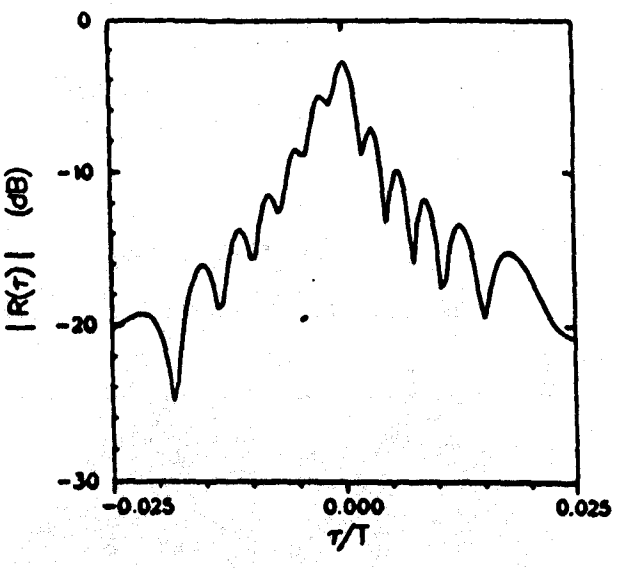
$\delta = 0.0$

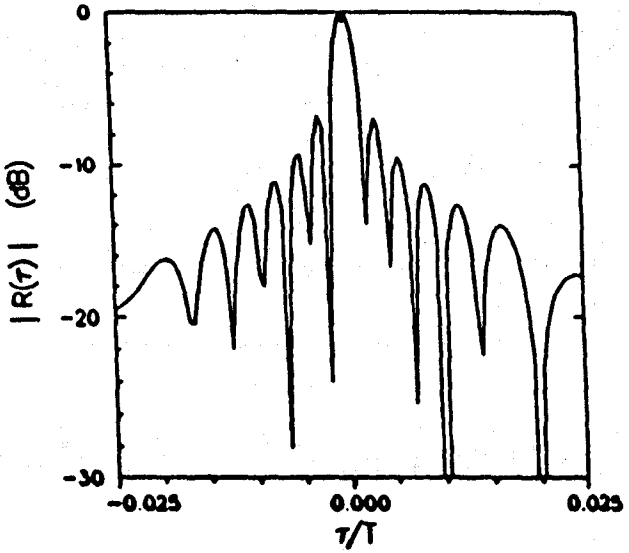


$\delta = 0.00025$



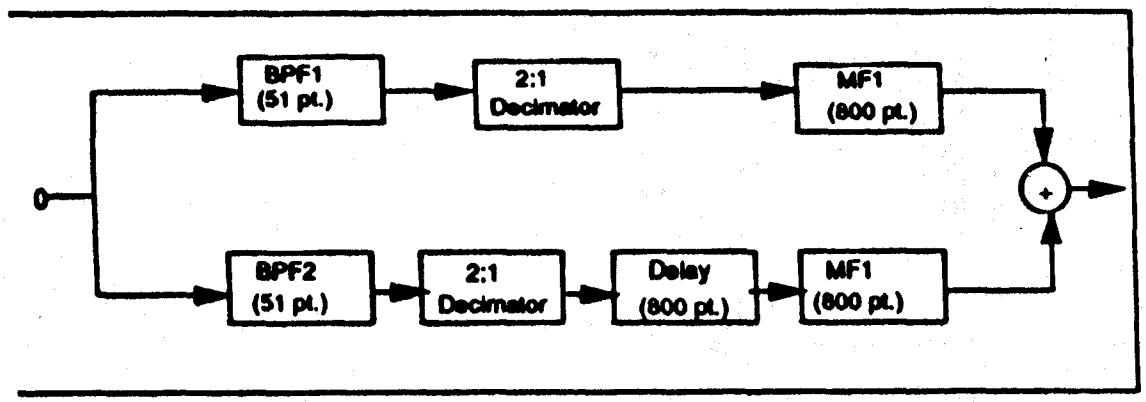
$\delta = 0.0025$



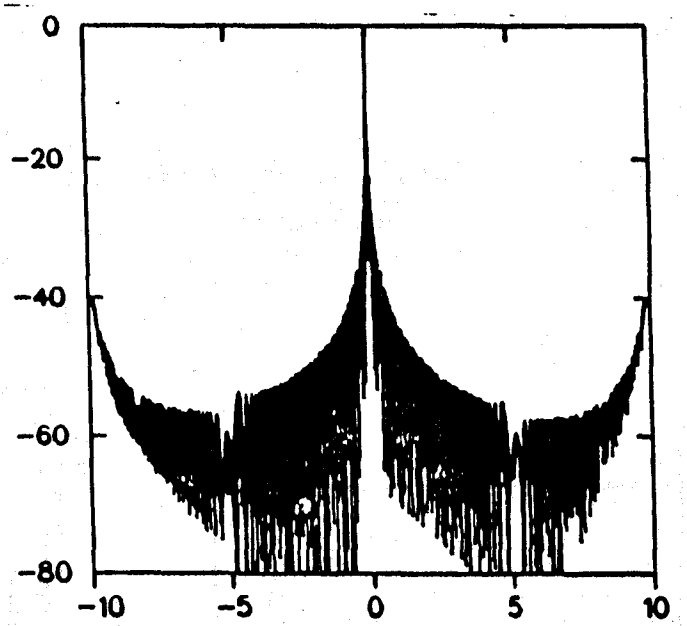


$\delta = 0.0025$
Modified Weights

MATCHED FILTER IMPLEMENTATION



PARALLEL ARCHITECTURE



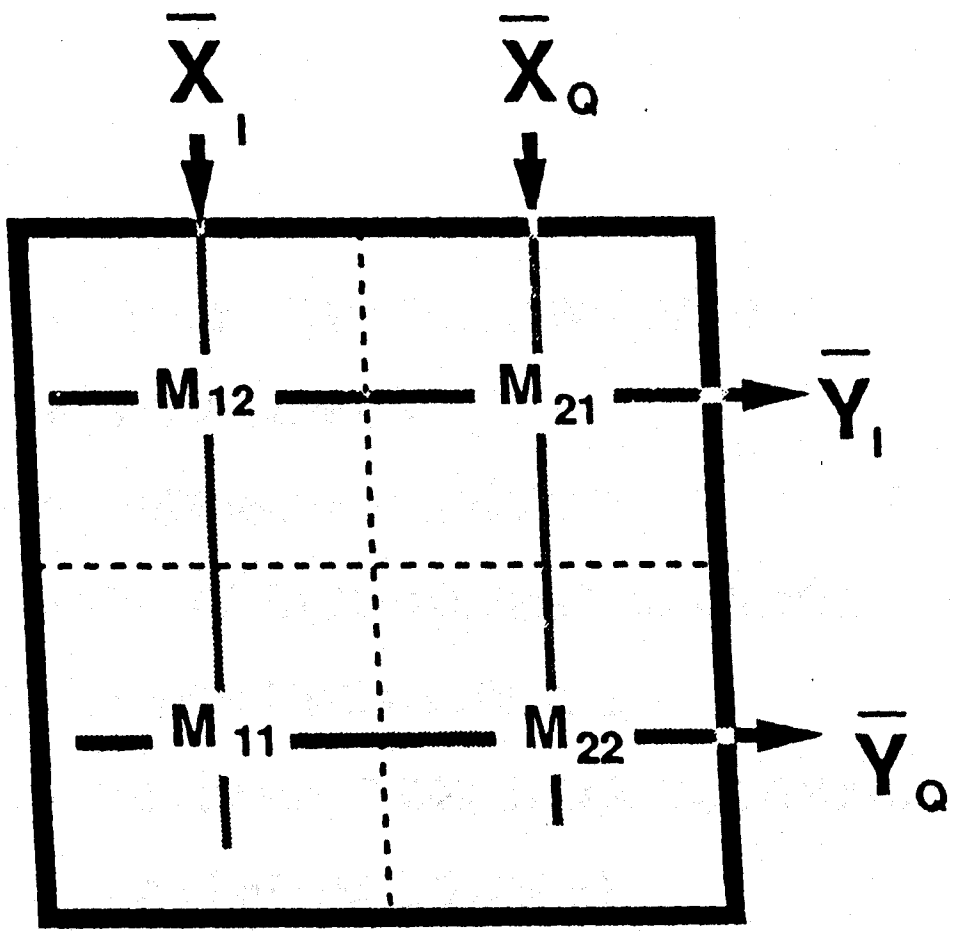
MATCHED FILTER RESPONSE
(N=3200 LFM)

- REQUIRED TIME-BANDWIDTH PRODUCT ACHIEVED USING AVAILABLE CMOS/CCD TECHNOLOGY
- APPLICABLE TO BI-PHASE/LINEAR (NON-LINEAR) FM
- INPUT BANDPASS FILTER CHOSEN TO MAXIMIZE PULSE COMPRESSION GAIN

DFT/BEAMFORMER REQUIREMENTS

- 16-32 POINT COMPLEX
- >50dB NULL DEPTH/1% ACCURACY
- >50dB LINEAR RANGE
- >60dB INSTANTANEOUS RANGE
- 10MSPS INPUT RATE
- LOW POWER
- SELF CONTAINED/MONOLITHIC

COMPLEX VECTOR MATRIX PRODUCT

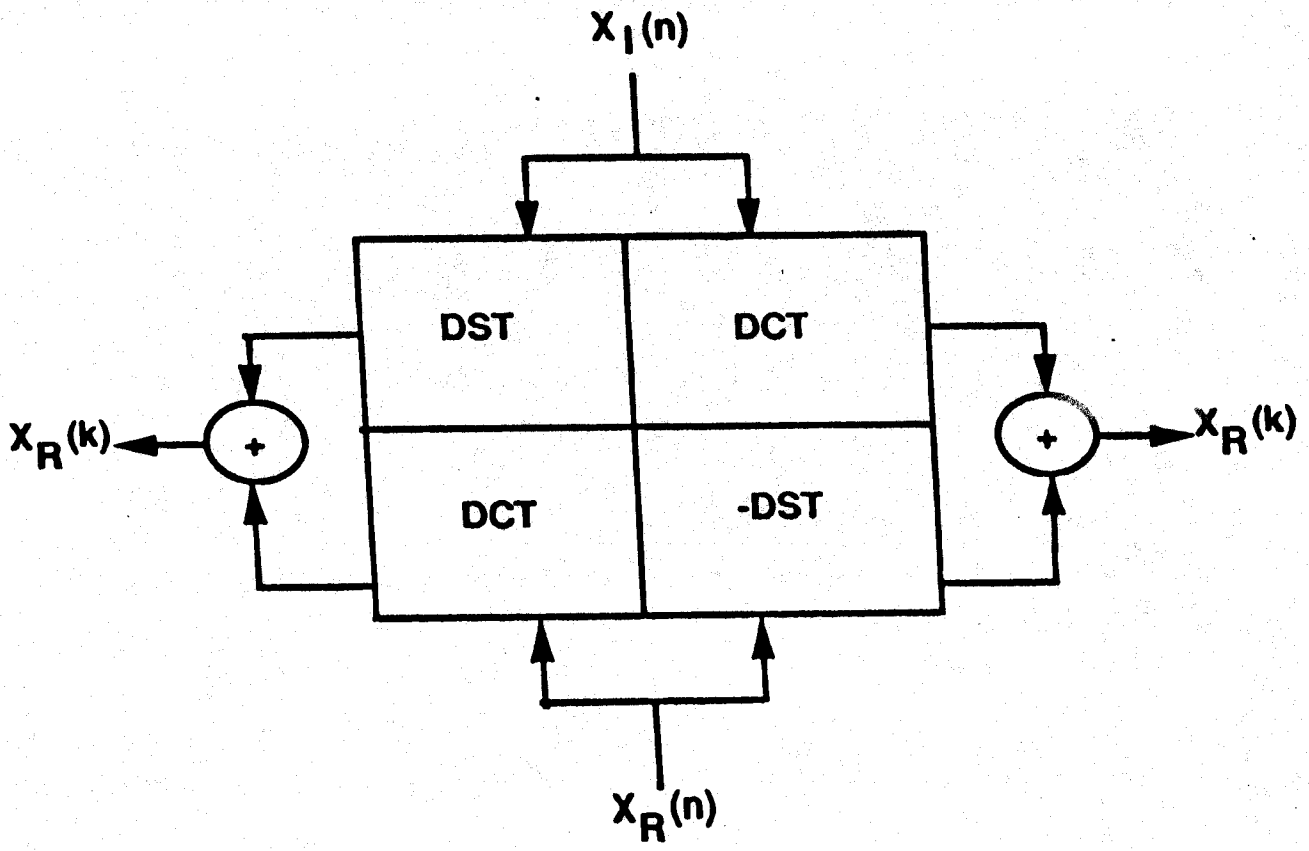


$$\begin{bmatrix} \bar{Y}_I \\ \bar{Y}_Q \end{bmatrix} = \begin{bmatrix} M_{12} & M_{21} \\ M_{11} & M_{22} \end{bmatrix} \begin{bmatrix} \bar{X}_I \\ \bar{X}_Q \end{bmatrix}$$

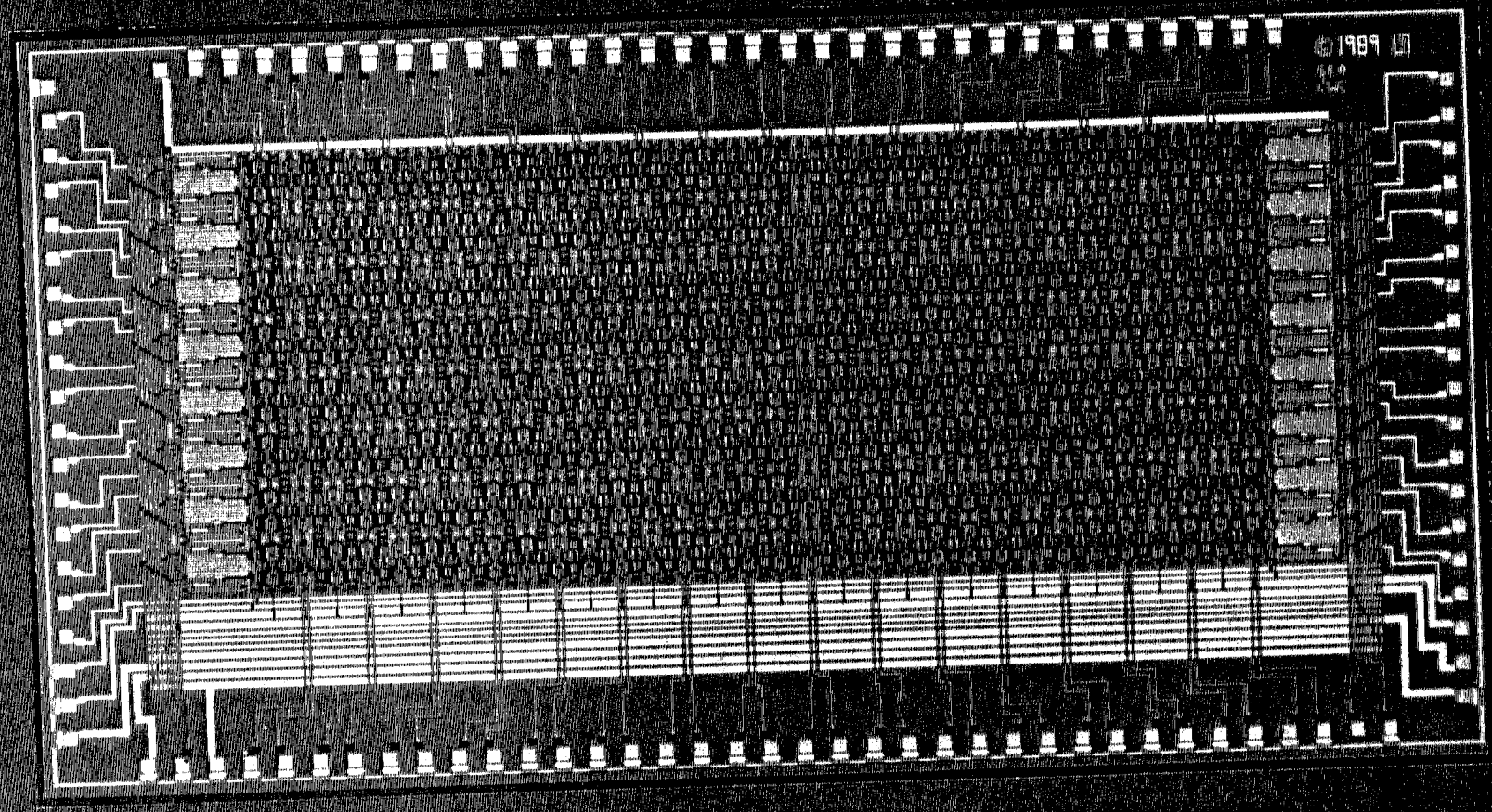
CCD DFT IMPLEMENTATION

$$X(k) = \sum_n x(n) e^{-j\frac{2\pi nk}{N}} = \sum_n [x_R(n) + jx_I(n)]\left[\cos\left(\frac{2\pi nk}{N}\right) - j\sin\left(\frac{2\pi nk}{N}\right)\right]$$

$$= \underbrace{\left[\sum_n x_R(n)\cos\left(\frac{2\pi nk}{N}\right) + \sum_n x_I(n)\sin\left(\frac{2\pi nk}{N}\right)\right]}_{X_R(k)} + j\underbrace{\left[\sum_n x_I(n)\cos\left(\frac{2\pi nk}{N}\right) - \sum_n x_R(n)\sin\left(\frac{2\pi nk}{N}\right)\right]}_{X_I(k)}$$



ADVANCED CCD DISCRETE FOURIER TRANSFORM (DFT) DEVICE



IMPROVEMENT FACTORS

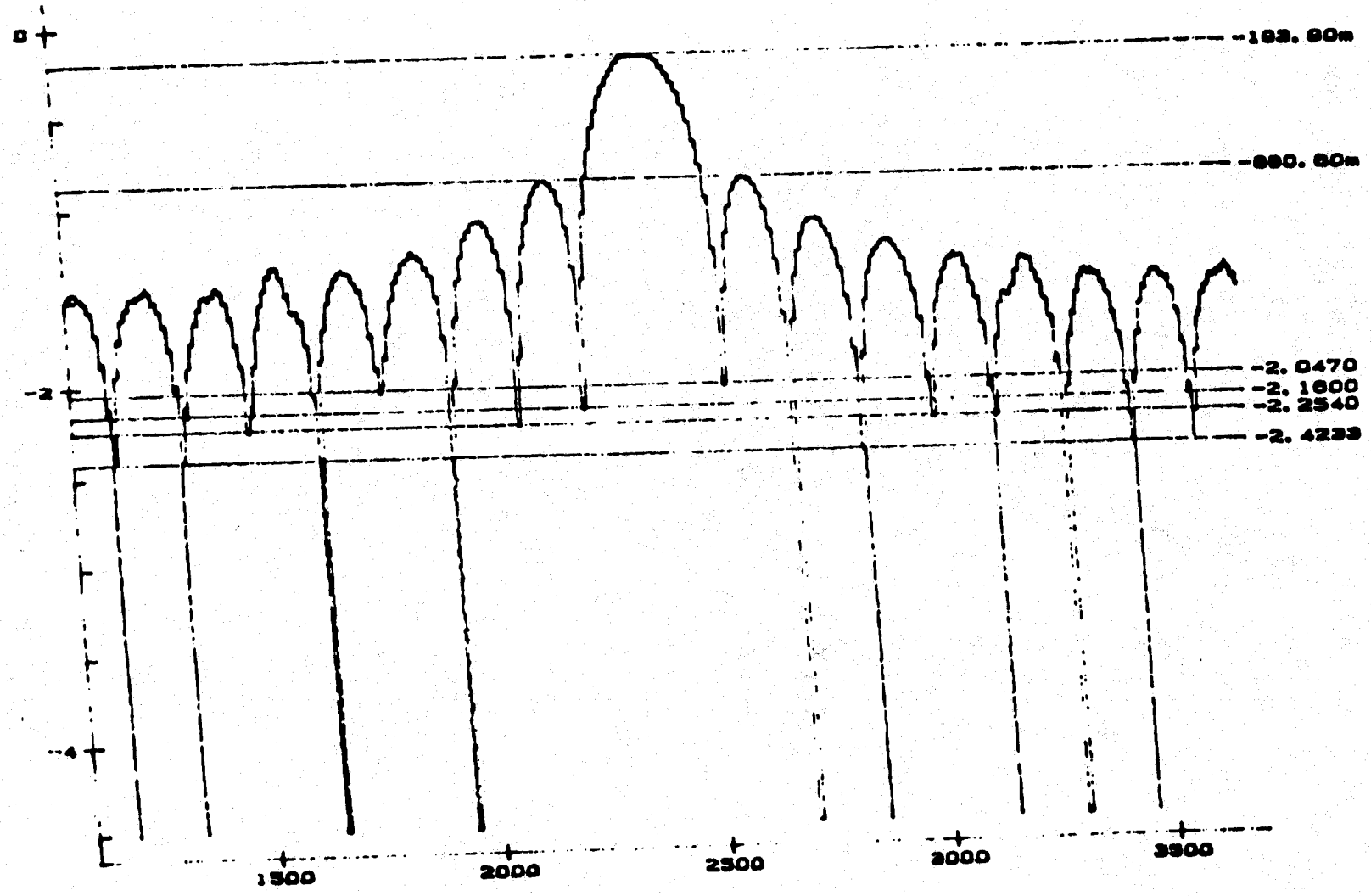
- INCREASED LINEARITY AND DYNAMIC RANGE
- ELIMINATE BIASES
- REDUCED CLOCK LOADING
- FULL SPEED THROUGHPUT

NEW DESIGN FEATURES

- SINGLE (+) WELL TYPE
- FULLY DIFFERENTIAL INPUT/OUTPUT
- DIODE CUTOFF INPUT
- FULL METAL STRAPPING REFINED OUTPUT BUFFERS AND RESETS

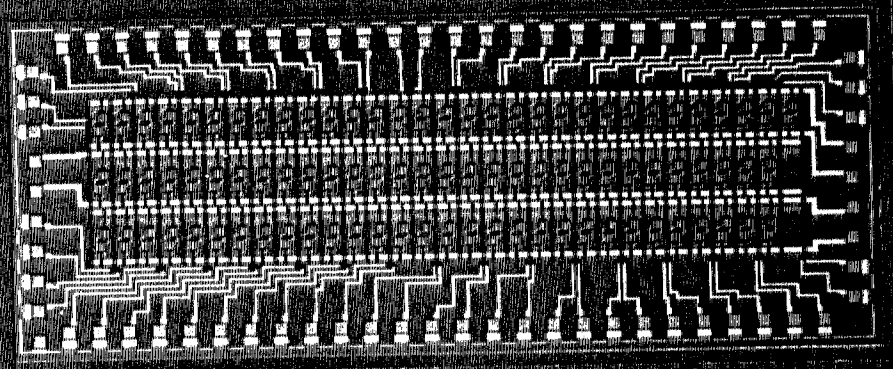
172979-1

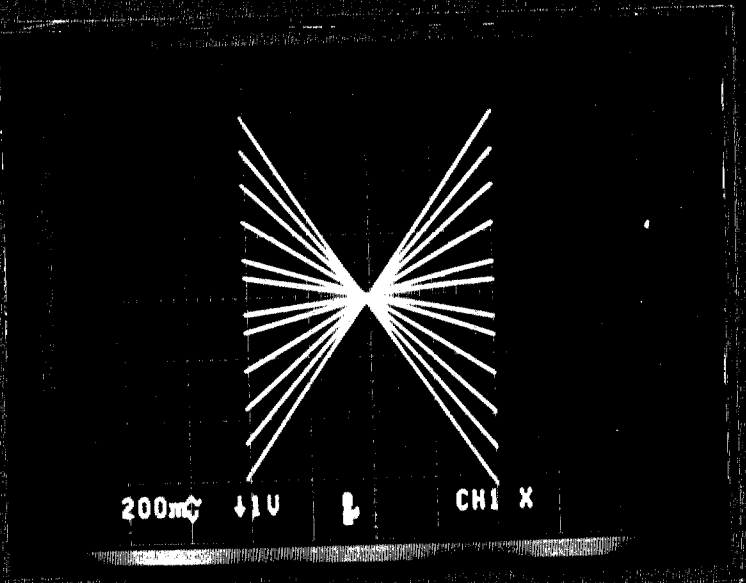
LOGXSQ

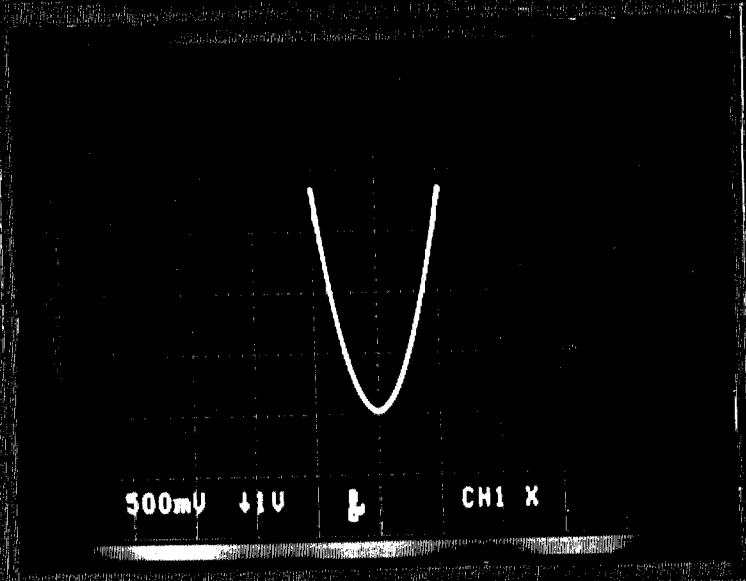

0
-2
-4
-163.60m
-880.60m
-2.0470
-2.1600
-2.2540
-2.4239
1500
2000
2500
3000
3500

Clkg

CMOS/CCD MULTIPLIER-SQUARING INITIAL TEST RESULTS







DESIGN GOALS:

- SQUARING FUNCTION
  (Full Spectral Processing)
- XY ANALOG MULTIPLICATION
  (Correlation)
- COMPATIBLE WITH CCD
  ARCHITECTURE
- FULL DIFFERENTIAL

172979-1