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III-V CCDs

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5. Summary

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Why III-V CCDs?
(GaAs, InGaAs, AlGaAs, InP, InAlAs)

Features

- High Speed
  - -High electron mobility
  - -Semi-insulating substrate
- Compatible with III-V E-O materials
  - -Franz-Keldysh
  - -MQW Stark Effect
- Compatible with III-V O-E devices
- Radiation-hard
  - -no oxide

Applications

- Fast-In, Slow-Out
  Signal Acquisition
- Multiplexer for
  IR detectors
- Demultiplexer for SLM
- Correlator
- High speed imager
  - -visible/UV
  - -x-ray

Taxonomy of III-V CCDs

Material(s)
- GaAs, AlGaAs, InGaAs, InP, InAlAs

Channel
- MESFET (buried-channel)
- 2 DEG (surface-channel)

Gate Structure
- Capacitive-gate
  - open gap
  - recessed-gap
- overlapping
- junction
- insulated

- Resistive-gate
  - semiconductor
  - cermet

Speed
- High Speed (>100MHz)
- Low Speed (<100MHz)

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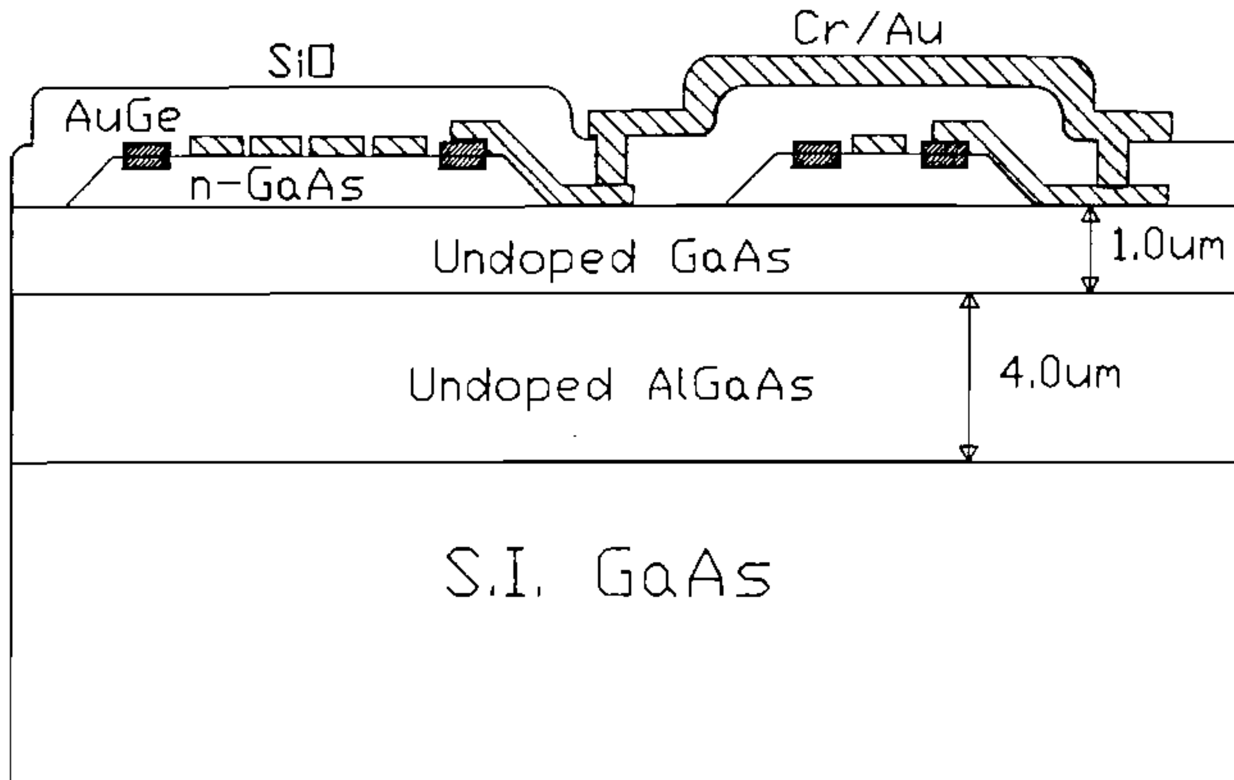
From R. Colbeth, 1989

Year	Group	Channel Layer Material	Gap Size (um)	Channel Thick-ness (um)	Doping ($/cm^3$)	Gate Length x Width (um)	Clock Freq-uency	CTE	Special Features
1977	Rockwell	GaAs	1.5	1.0	1.0×10^{16}	40x400	1MHz	>0.999	
1979	Siemens	GaAs	2.0	0.2	$\sim 2 \times 10^{17}$	5x	30MHz	0.99	CTE < 0.9 at 100MHz
1980	Hughes	GaAs	1.0	1.1	1.5×10^{16}	14x200	2.8KHz	0.99	Planar, Schottky channel stop
1980	Rockwell	GaAs	1.5	1.0	1.0×10^{16}	5x100	150MHz	>0.999	
1980	Rockwell	GaAs+ AlGaAs	1.0	1.0	1.0×10^{16}	10x100	~1MHz	>0.999	Proton isolation 3 phase
1980	Rockwell	AlGaAs	1.5	1.5	1.5×10^{16}	40x400		0.999	Backside illum-inated imager
1980	NOSC	InP	N/A	N/A	undoped	40x400	50MHz	>0.995	Surface channel, 1 stage
1980	Rockwell	GaAlAsSb /GaSb							Charge transfer at 77 K
1980	Siemens	GaAs	0.3	0.2	$\sim 10^{17}$	4x	1MHz	0.99	2-phase CCD
1981	NOSC	InP	N/A	N/A	7×10^{16}	10x120	1MHz	>0.998	Surface channel overlapping gate
1981	Rockwell	GaAs	1.0	1.0	5×10^{15}	5x100	1GHz	>0.994	CTE > 0.9999 at low frequency
1982	Rockwell	GaAs	2.0	1.0	undoped	40x400	83kHz	0.968	Mod-doped AlGaAs/GaAs
1984	Rockwell	GaAs	N/A	0.3	1×10^{17}	6x100	2.5GHz	0.99	Resistive-gate 0.1-4.2 GHz
1985	MIT LL	GaAs	0.5	1.3-2.5	5×10^{15}	9x	1MHz	0.9998	Gap size defined by dielectric
1986	MIT LL	GaAs	1.0	0.014	undoped	10x100	1MHz	>0.998	Quantum well AlGaAs/GaAs
1987	Univ. of Cinn.	GaAs	0.06	0.2	$\sim 10^{17}$	5x	100kHz	>0.999	Gap defined by anodic ox of Al
1988	Columbia	GaAs	1.0	0.9	7×10^{15}	2x100	1GHz	>0.999	

Capacitive-Gate GaAs CCDs



GaAs CGCCD cross-section (from Colbeth, Rossi, Song and Fossum 1989).

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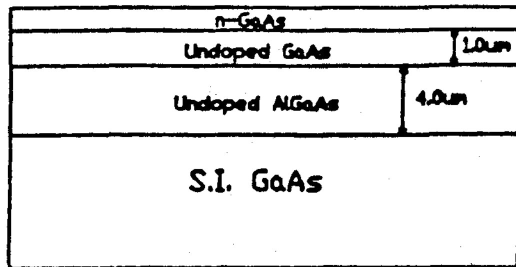
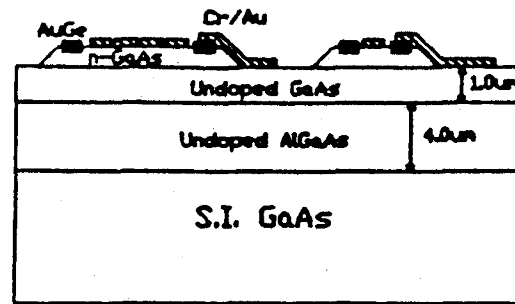
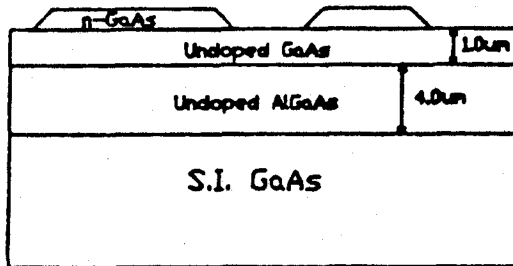
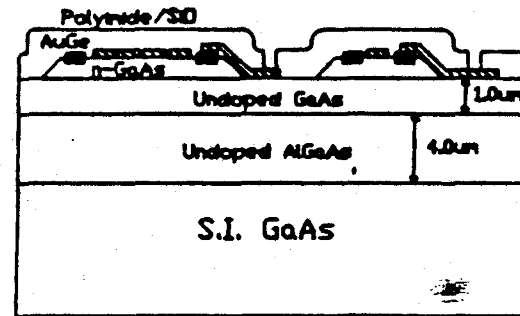
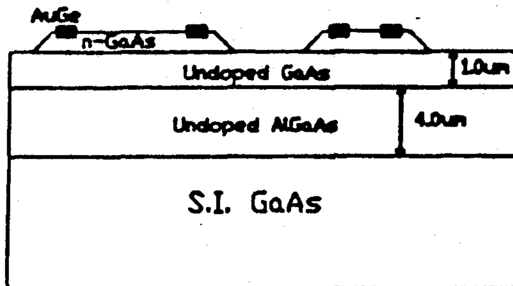
From R. Colbeth, 1989

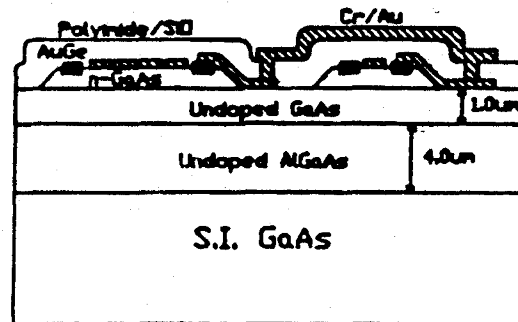












CGCCD fabrication sequence.

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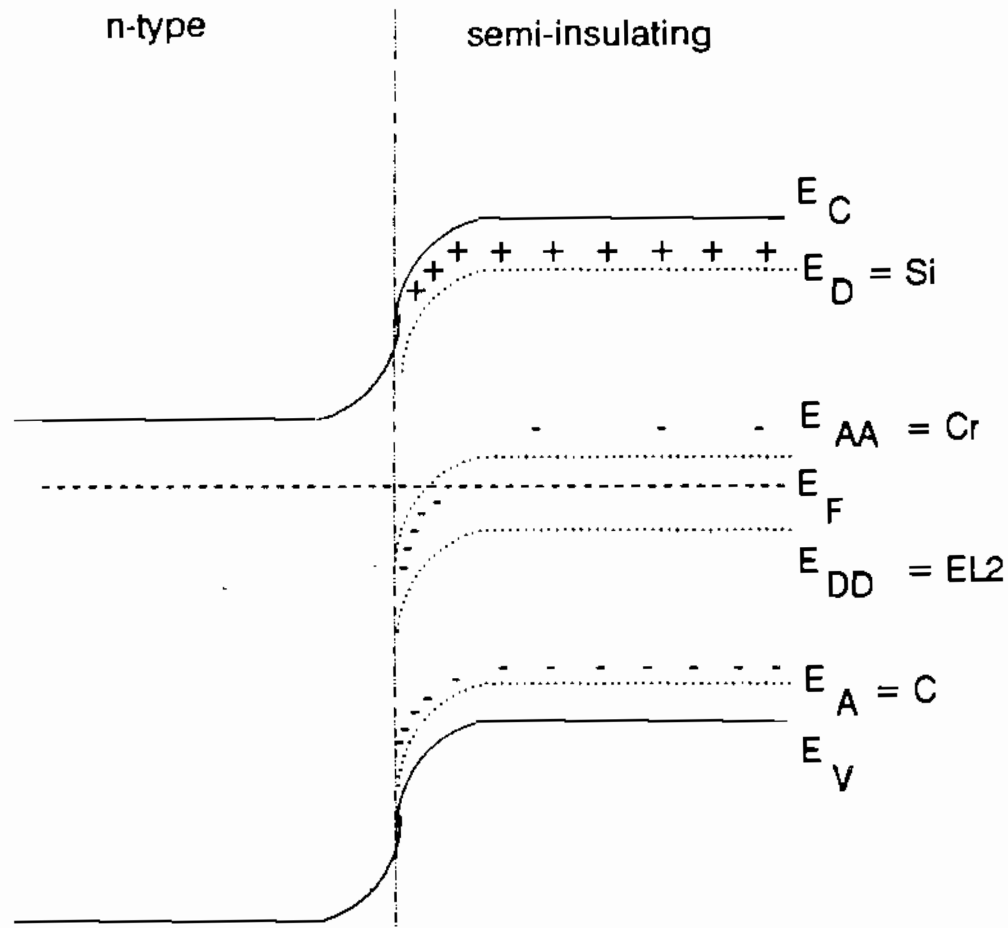

Charge distribution at the interface of the semi-insulating substrate and the active layer.

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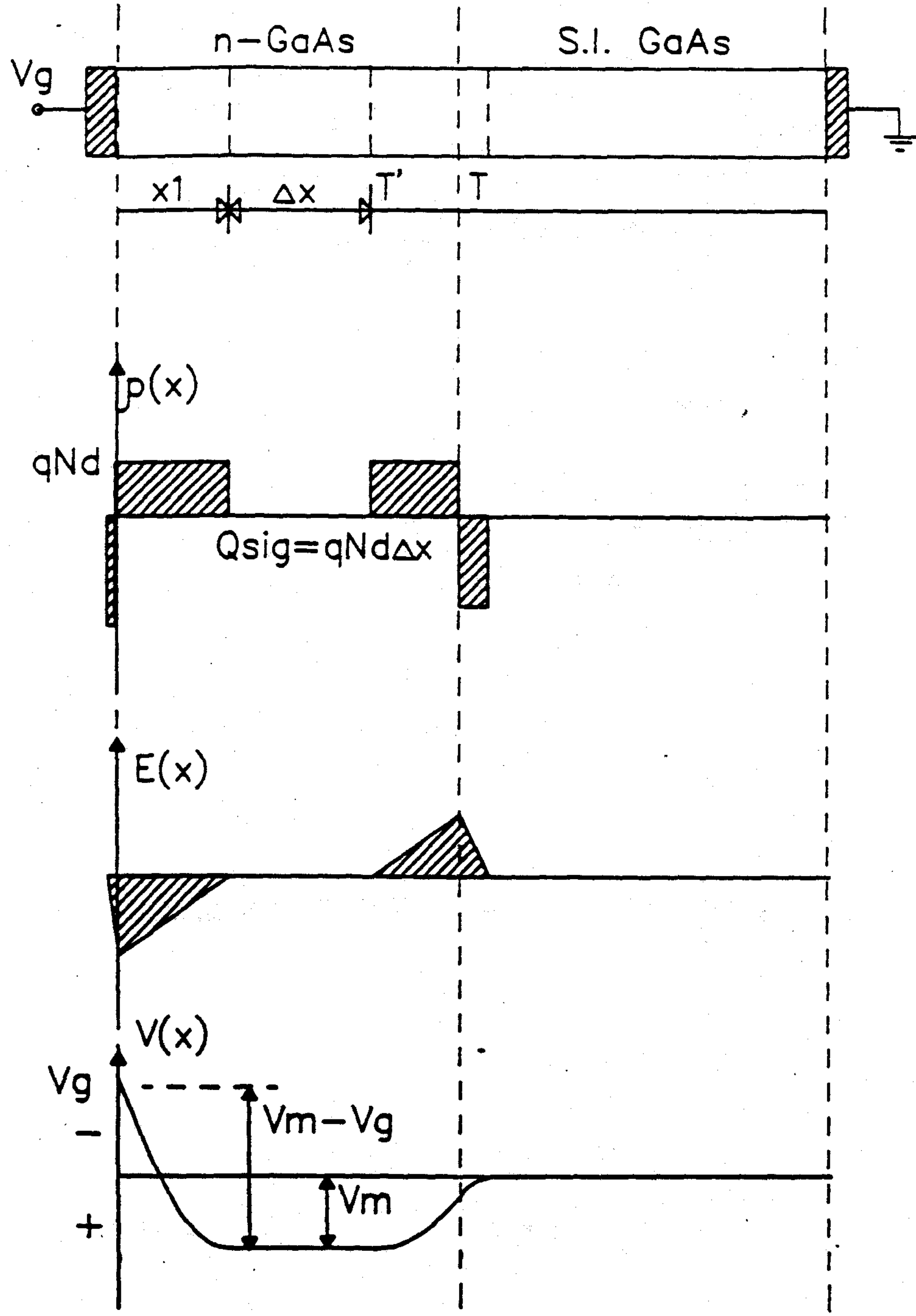

1-dimensional solution to Poisson's equation through GaAs CGCCD cross-section, assuming substrate appears p-type.

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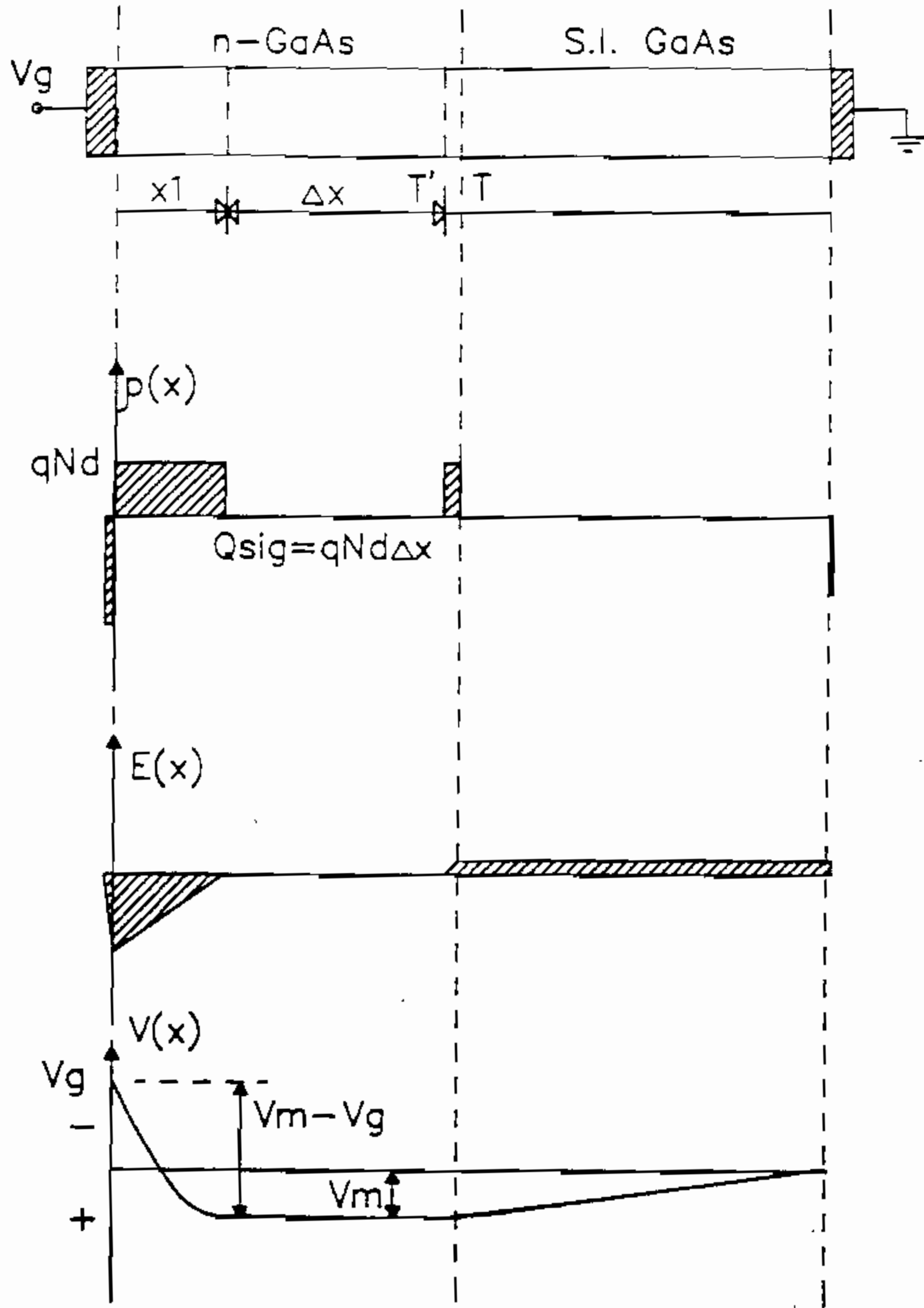

High frequency solution to Poisson's equation through GaAs CGCCD cross-section. Analysis assumes deep level traps in substrate do not respond to changes in gate voltage.

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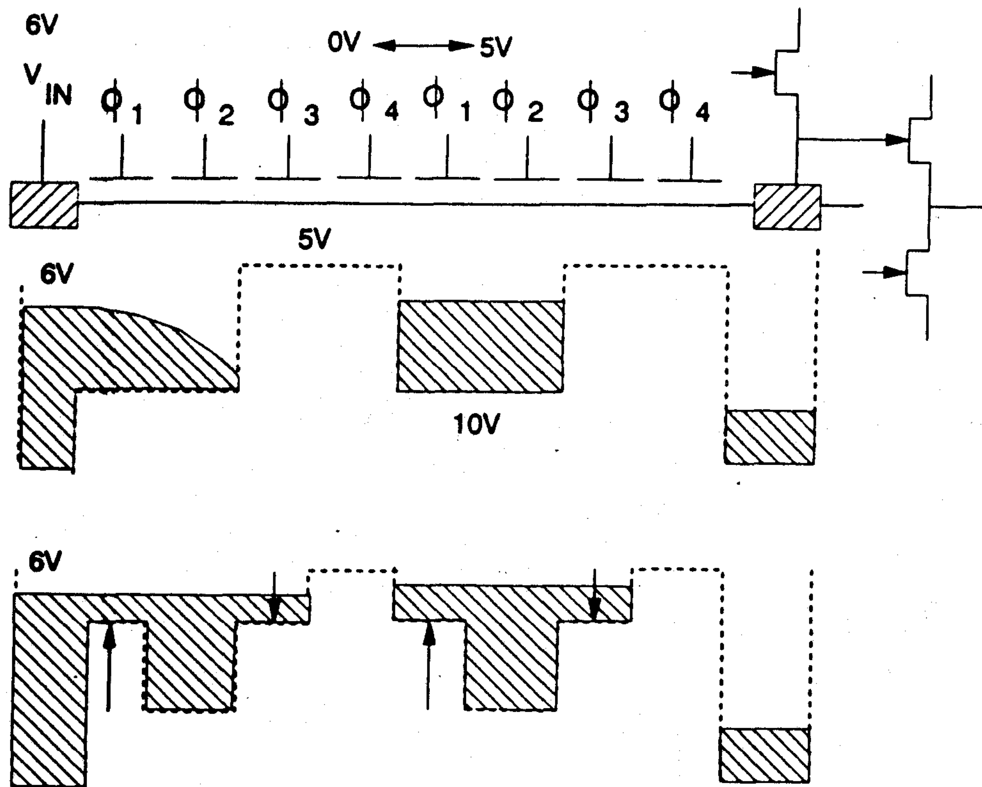

Example of charge injection input technique in GaAs CGCCD's. V_p is 5 volts.

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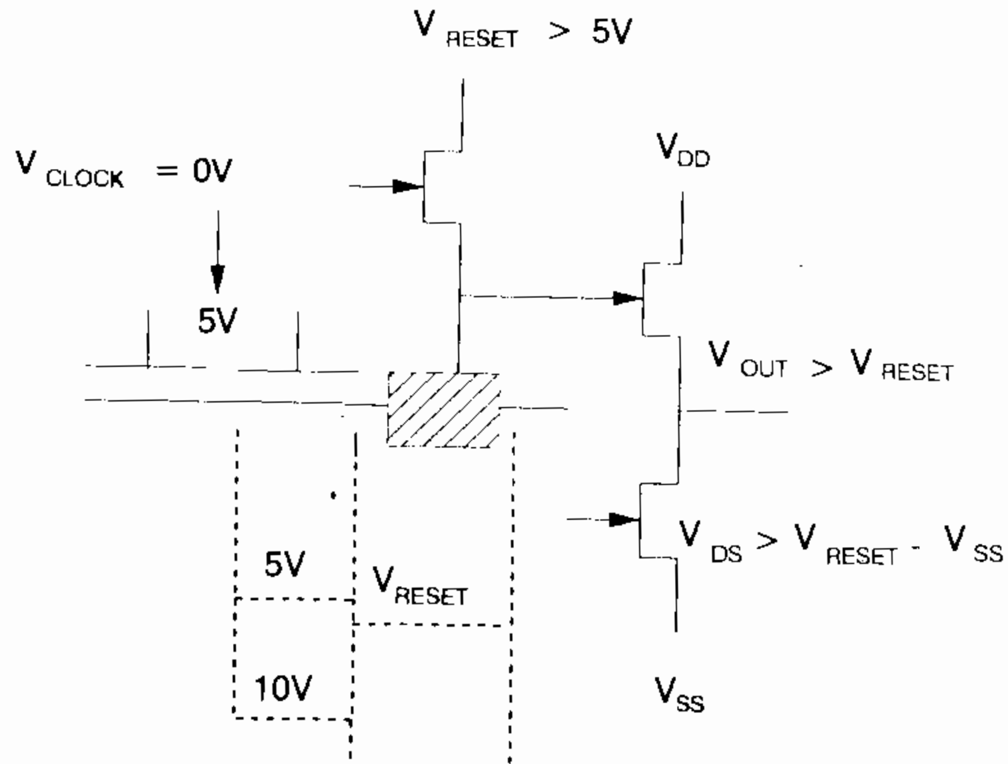
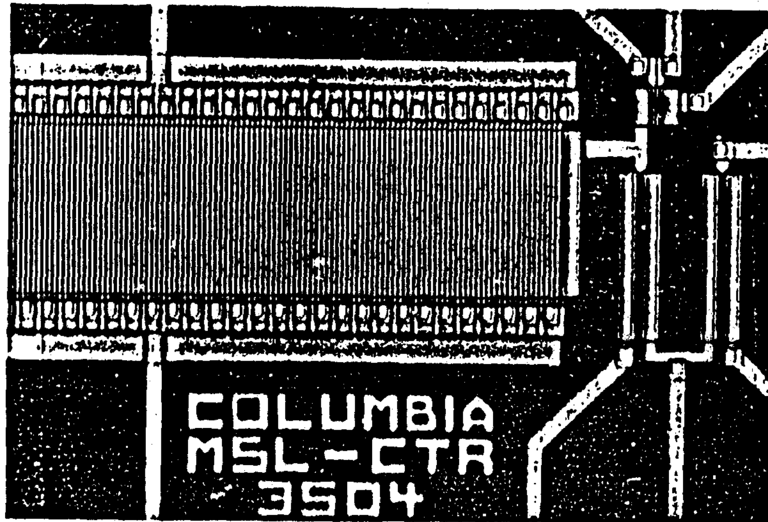
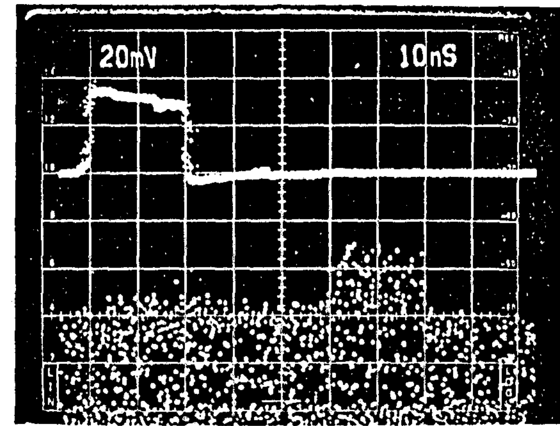


Output amplifier biasing constraints.

1 GHz GaAs CCD

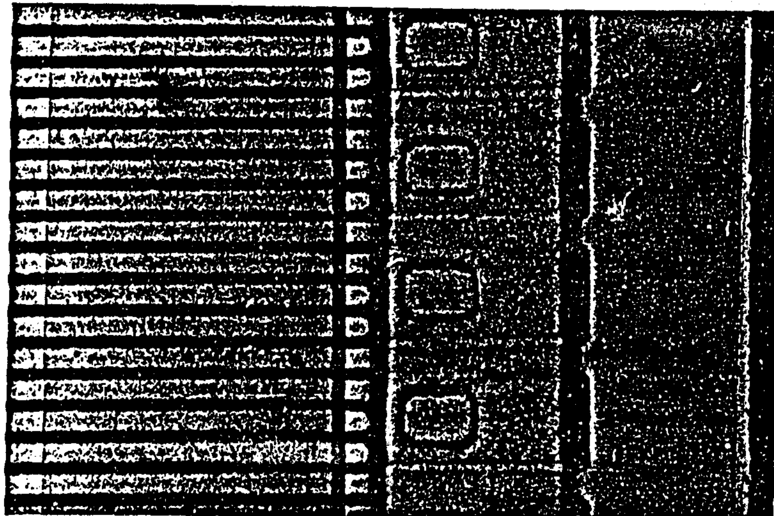


4—phase x 50 stages

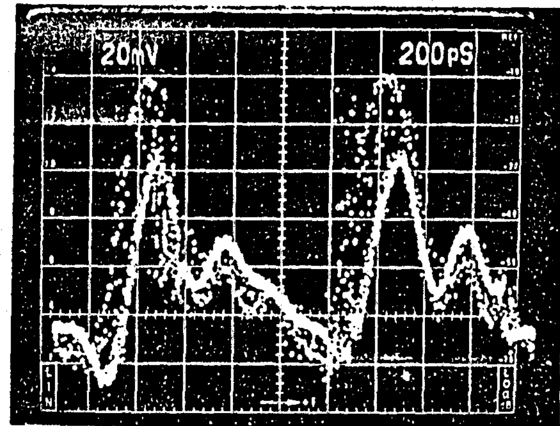


50 nsec delay

2 um gate, 1 um gap



Output Amplifier Signal



R.Colbeth/E.R.Fossum

Columbia University, October 1988

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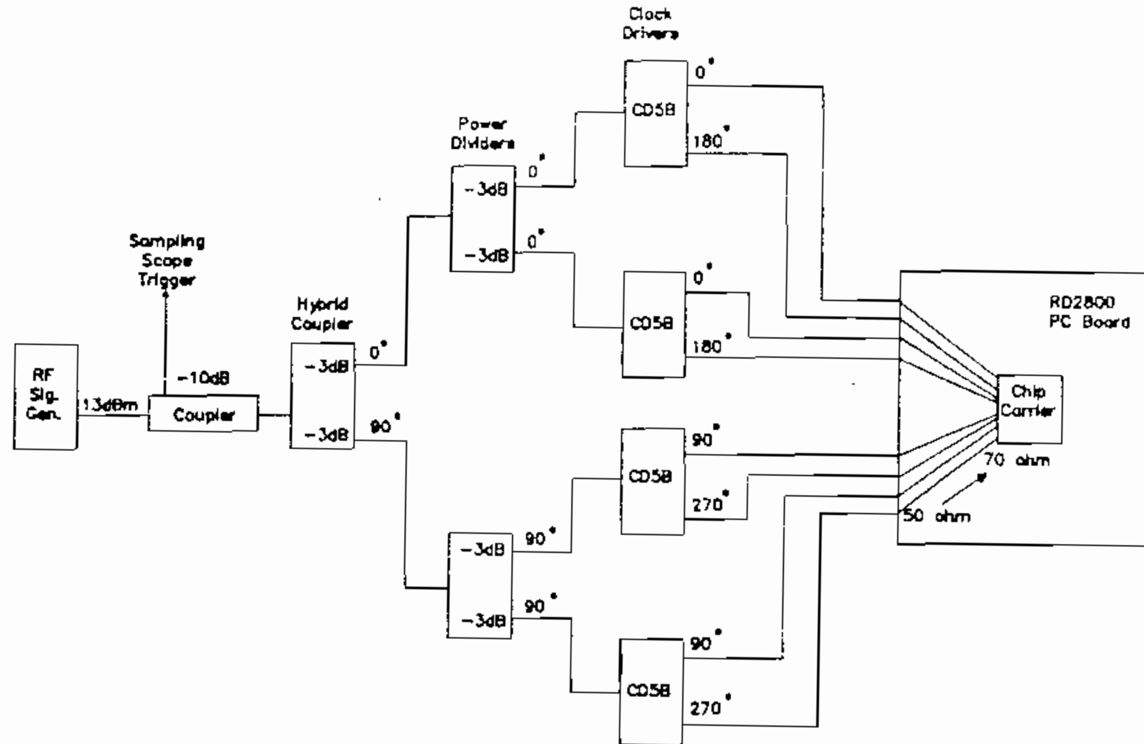
From R. Colbeth, 1989



High speed CCD test station (from Colbeth, Rossi, Song and Fossum 1989).

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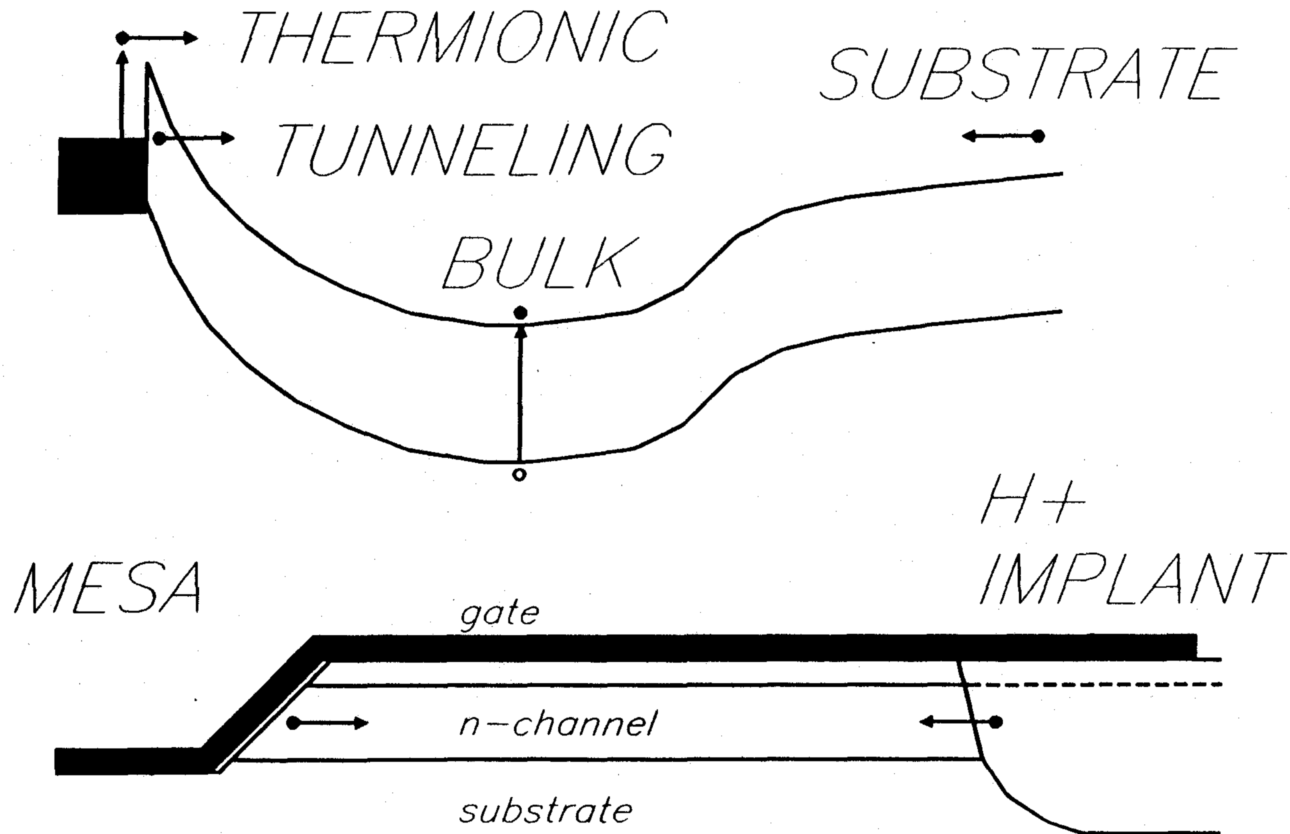
Dark Current

Dark Current dominated by gate leakage current.



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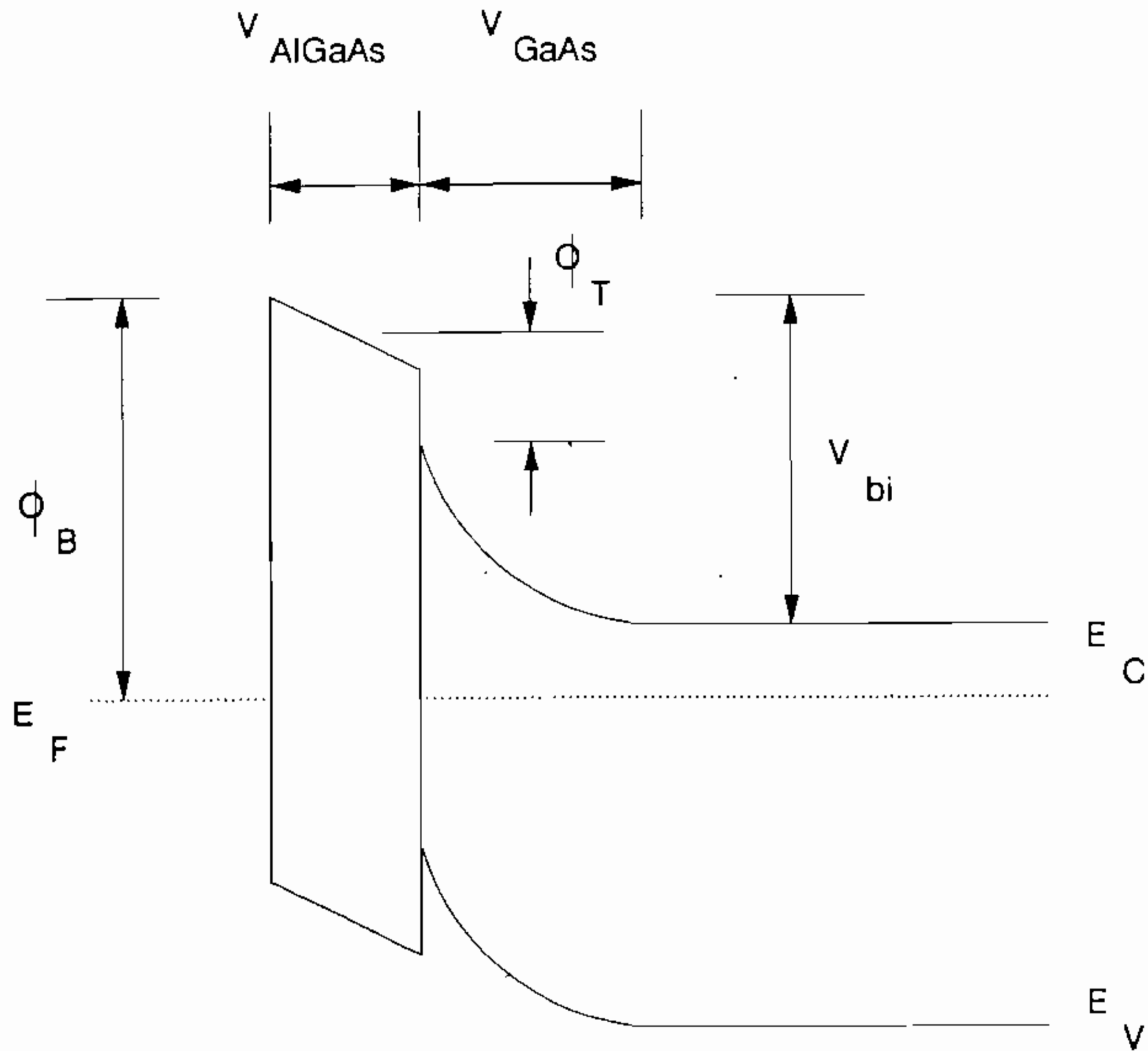
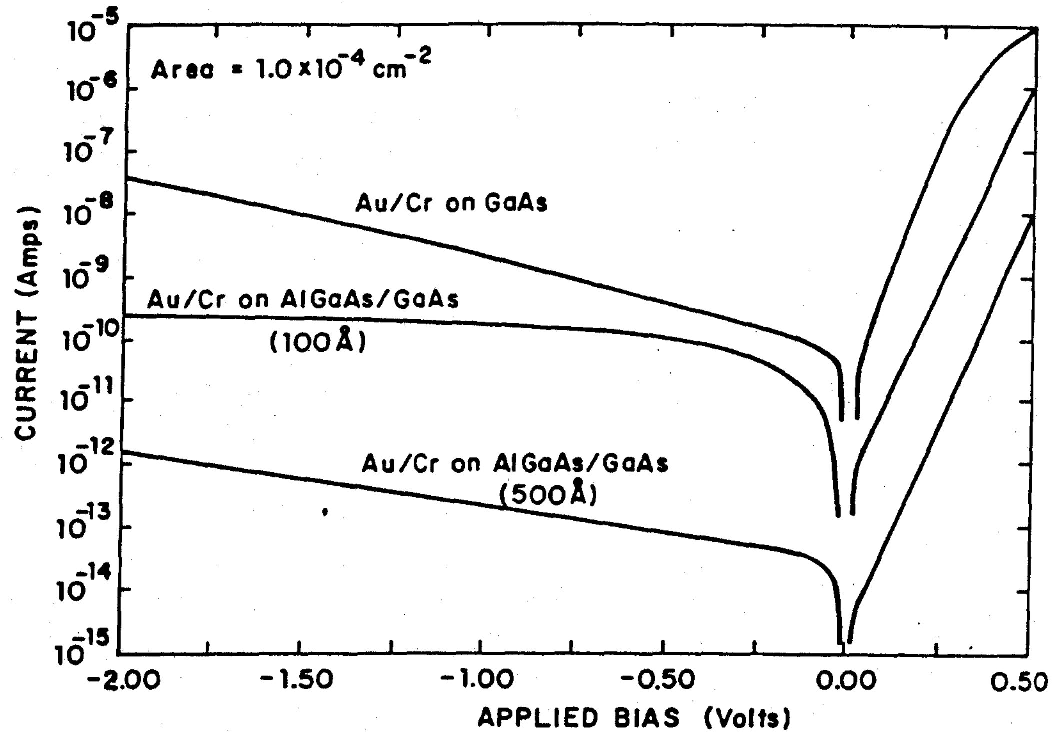
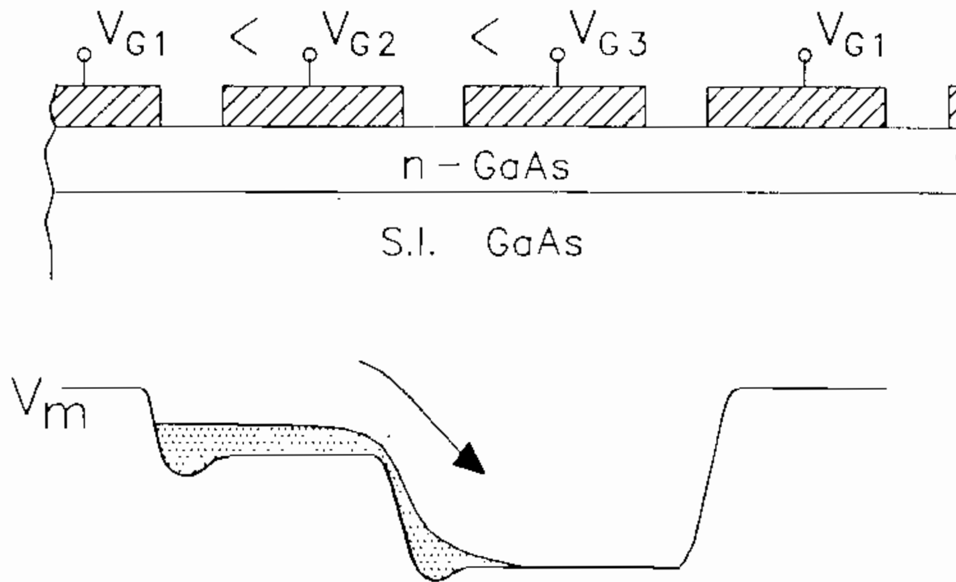


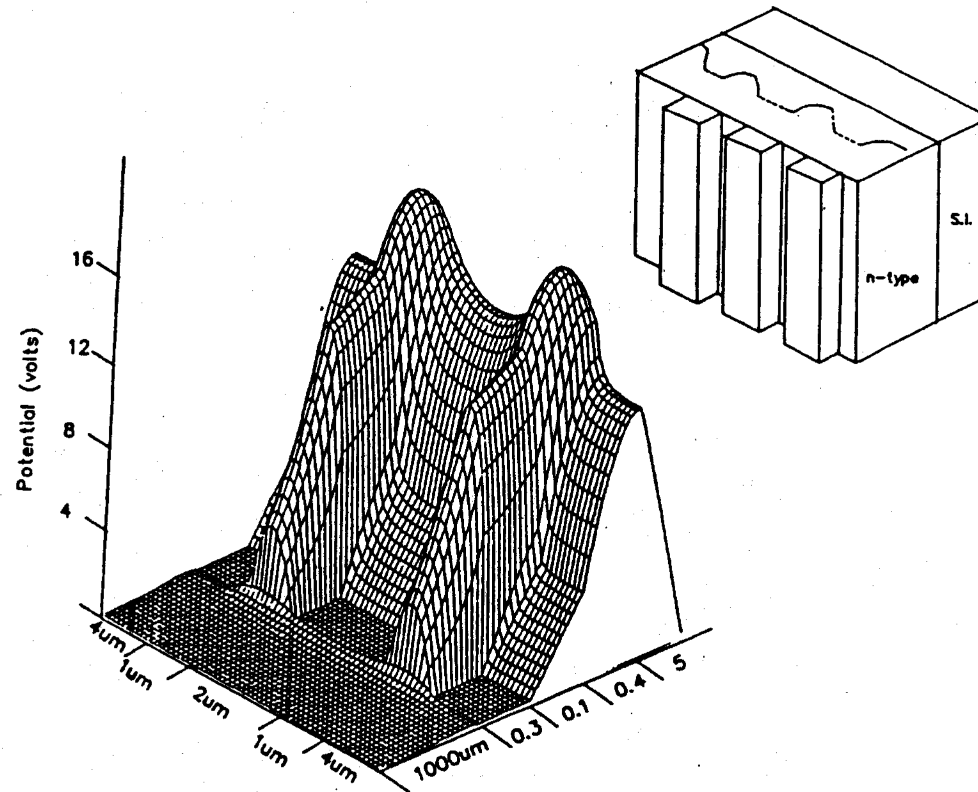
Equilibrium band diagram for large bandwidth GaAs CCD.



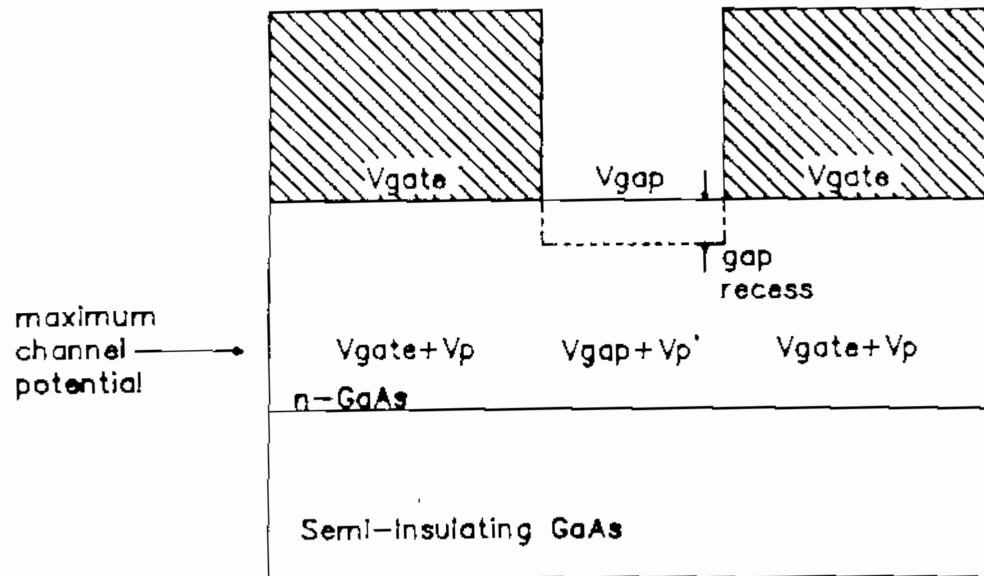
I-V curve for a diode fabricated on material from wafer W353. The AlGaAs cap layer is 100 A thick and the GaAs channel is 9000 A with doping of $1x10^{16}$ /cm^3.



Schematic illustration of the device structure and channel potential of a GaAs capacitive-gate charge-coupled device.



Full 2-dimensional solution to Poisson's equation in the interelectrode gaps between 3 gates (Song 1989).



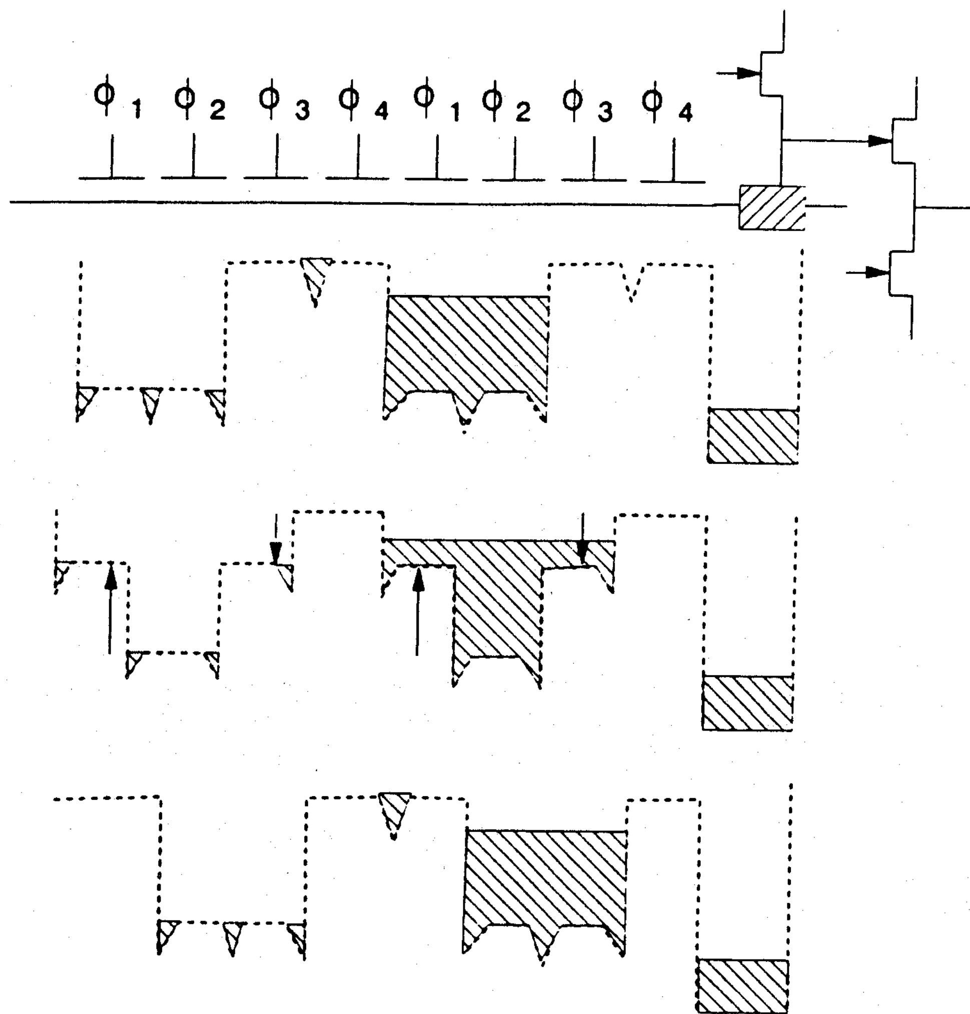
Vgap > Vgate

Vgap = f(gap size)

Vp' = f(layer thickness in gap)

V_{trough} = (Vgap+Vp')−(Vgate+Vp)

Superposition of two 1-D solutions to Poisson's equation in the interelectrode gap.



Channel potential and charge transport in GaAs CGCCD's with interelectrode potential troughs and small clock swing.

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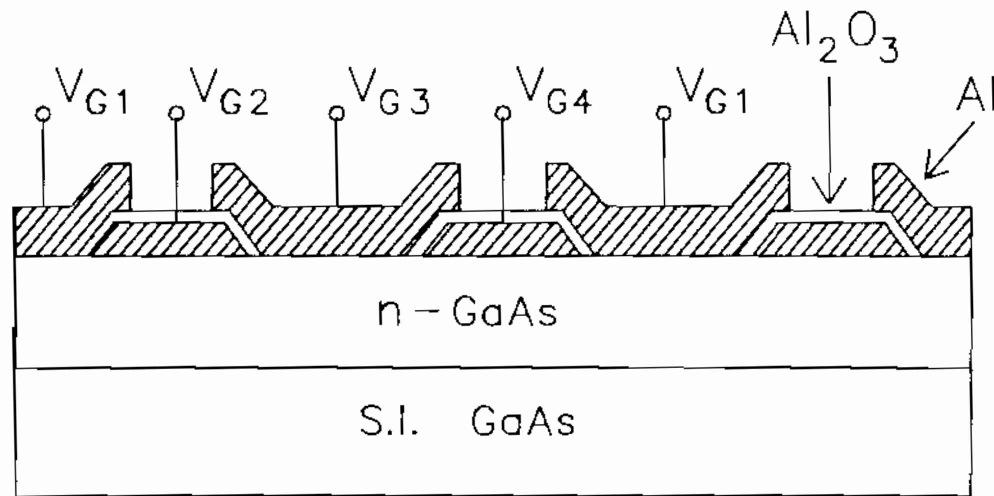

Cross section of an overlapping-gate GaAs charge-coupled device. (Ref. 22.)

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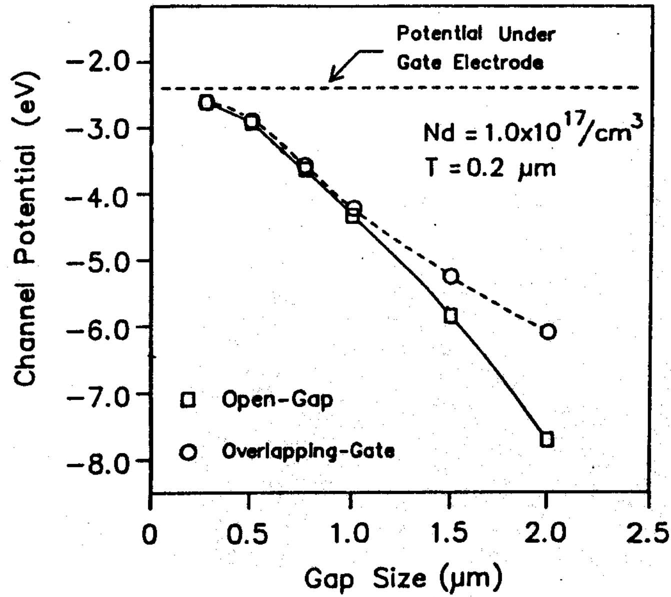
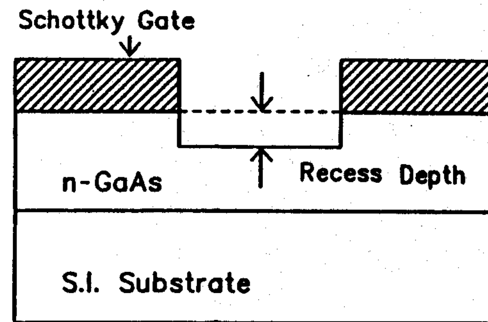
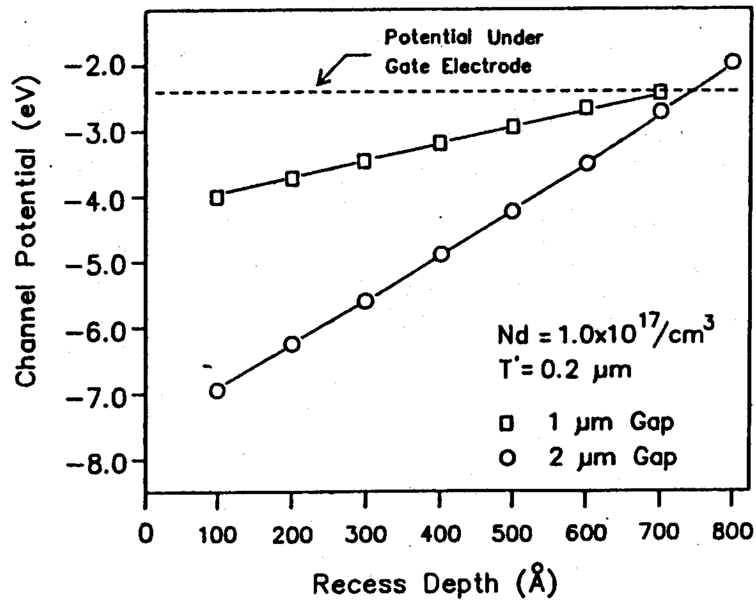
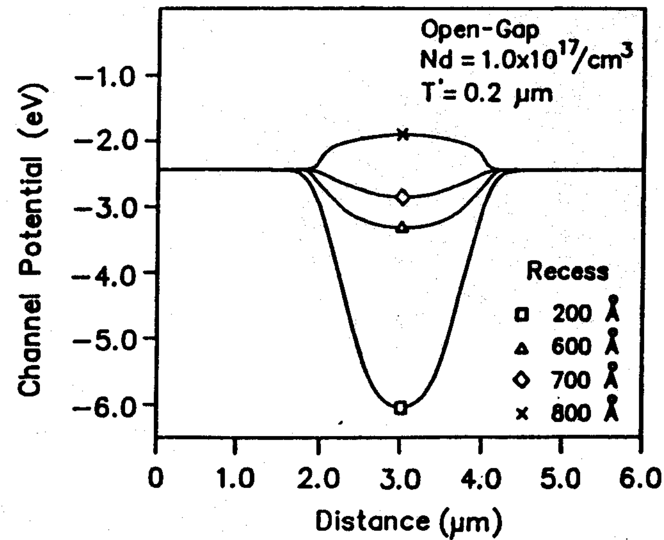




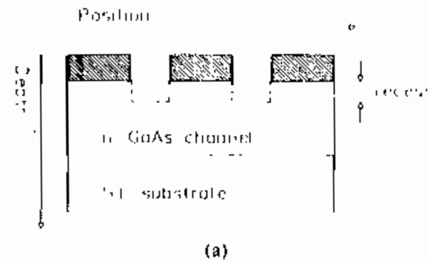
a)



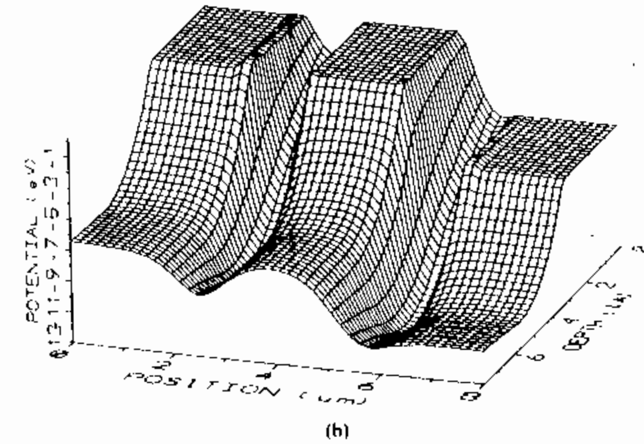


A Recessed-Gap Capacitive-Gate GaAs CCD

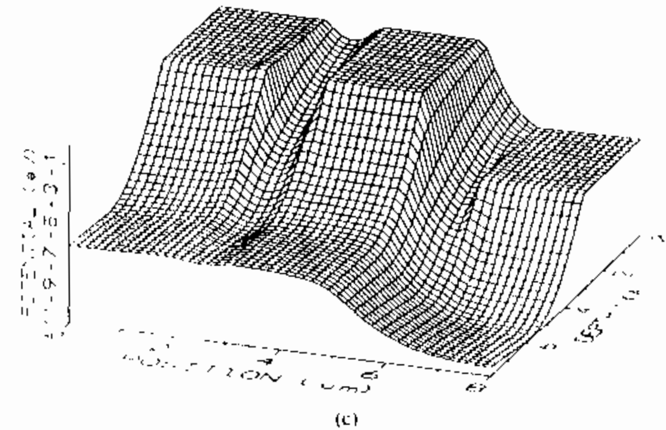
R. E. COLBETH, STUDENT MEMBER, IEEE, J.-I. SONG, D. V. ROSSI, STUDENT MEMBER, IEEE, AND
ERIC R. FOSSUM, MEMBER, IEEE



(a)



(b)



(c)

Fig. 1. Potential wells under three gates obtained by two-dimensional solution to Poisson's equation for a fully depleted channel. Channel region is toward viewer. (a) Schematic cross section of simulation structure (b) with no recess and (c) with gap recess of 1300 Å. Channel is n type, 0.285 μm thick, and doped at $1.2 \times 10^{17}/cm^3$. Electrodes (rear flat regions) are 0.3 μm thick, 2 μm long, and spaced 1 μm apart. The first two gates are biased at 0 V, and the third gate (right) is biased at +5 V.

Fig. 2. Photograph of 50-stage four-phase delay line. CCD gates are 100 μm wide by 2 μm long with 1-μm interelectrode gap spacing. FET gate lengths are 1 μm.

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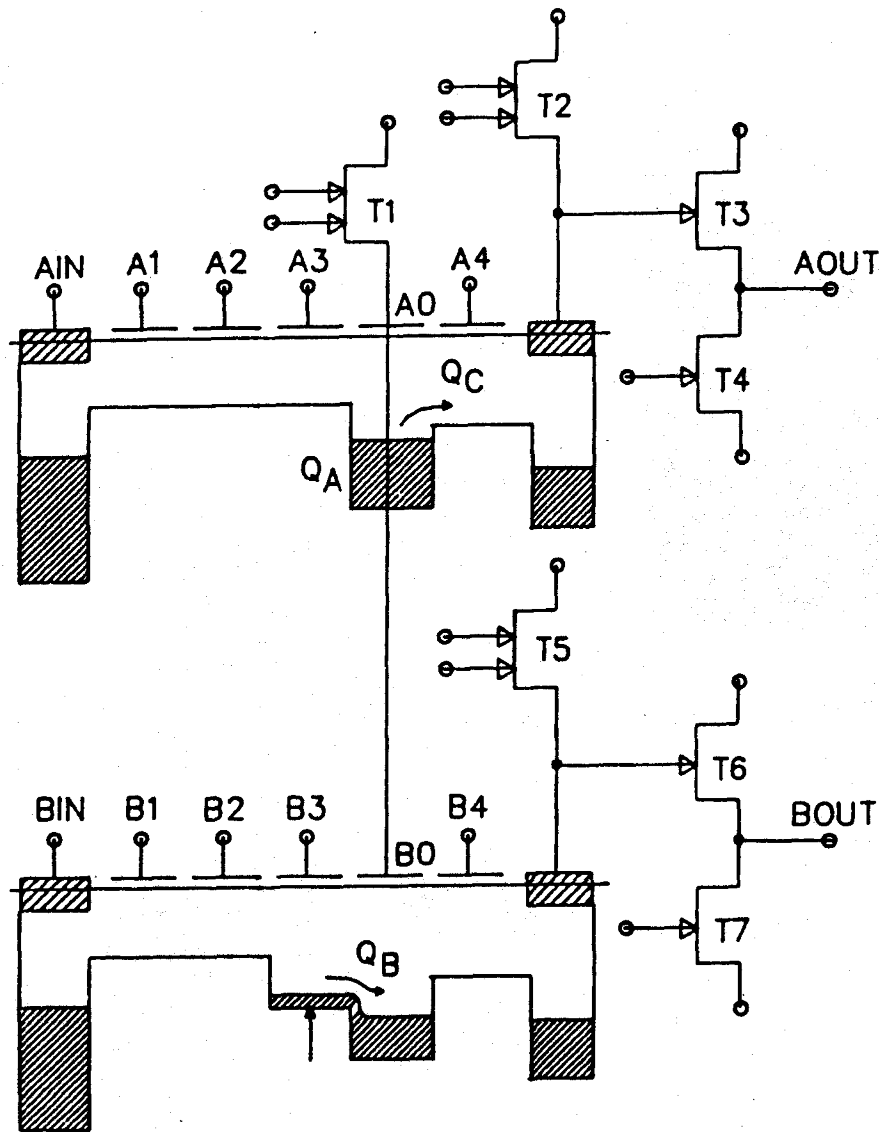
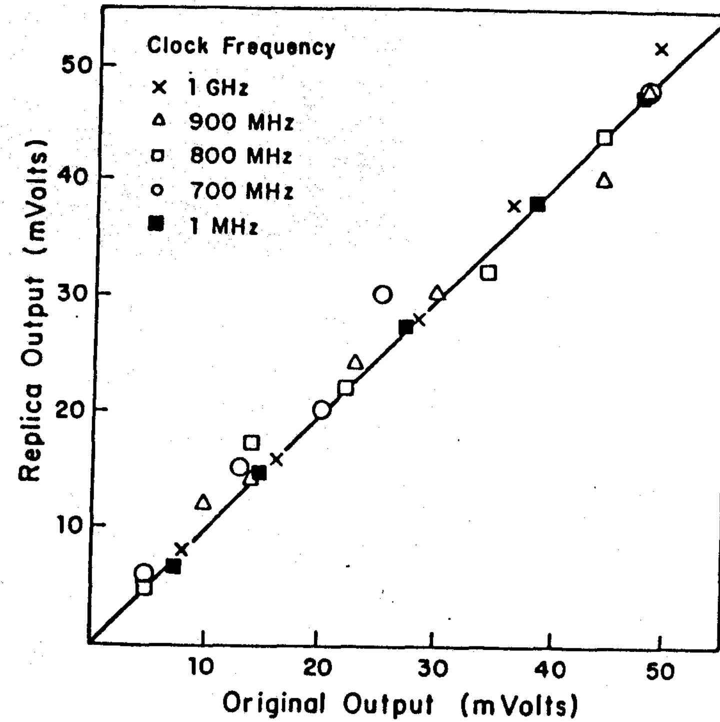


Schematic diagram of charge packet replicator/subtractor.



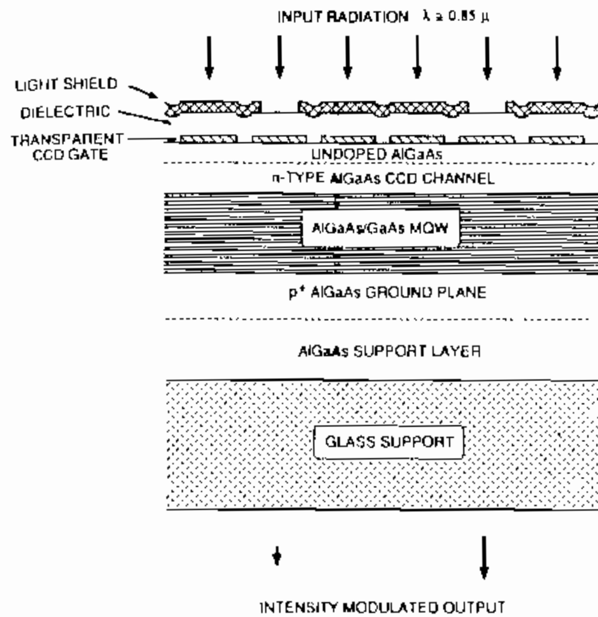


FIG. 1. Cross-sectional schematic of a CCD/MQW spatial light modulator

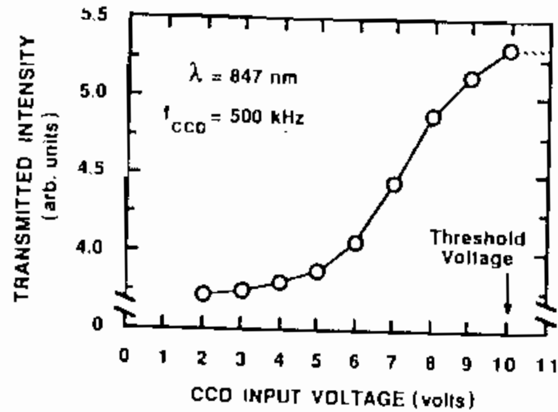


FIG. 3. Optical modulation data at 847 nm for a GaAs/AlGaAs-based, CCD/MQW spatial light modulator.

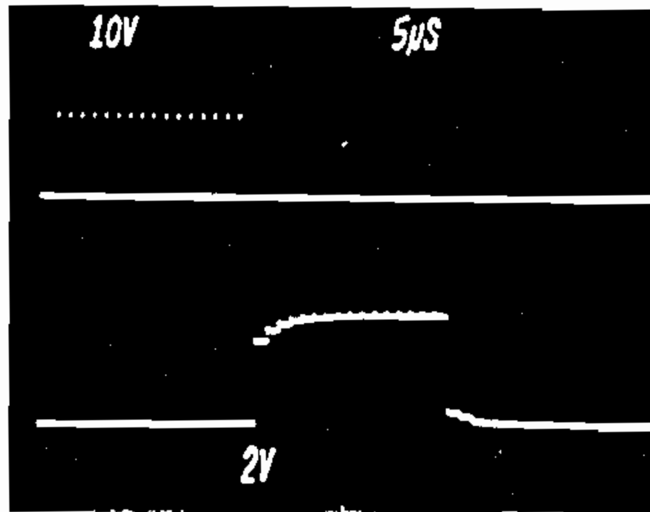


FIG. 2. Electrical performance of a 16-stage, AlGaAs charge-coupled device at 1.0 MHz clock rate The upper trace is the input to the device and the lower trace is the delayed output.

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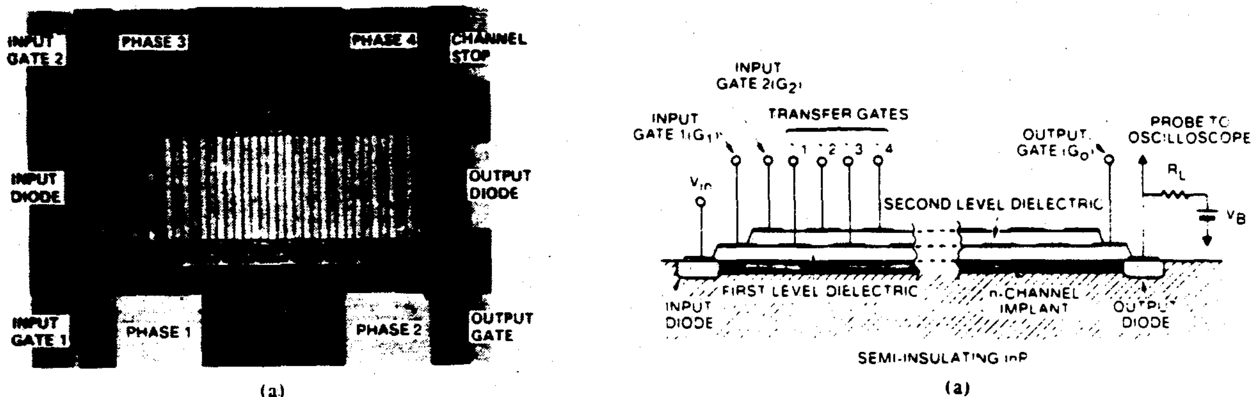
InP CCD



(a) (a)

Fig. 1. (a) A photomicrograph and (b) schematic cross section of the 8-bit buried-channel CCD on InP.

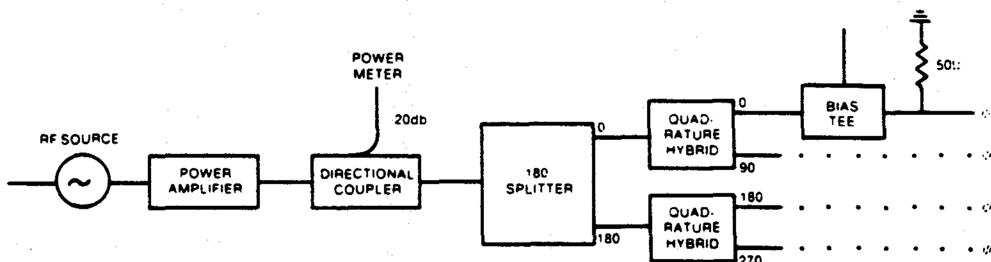
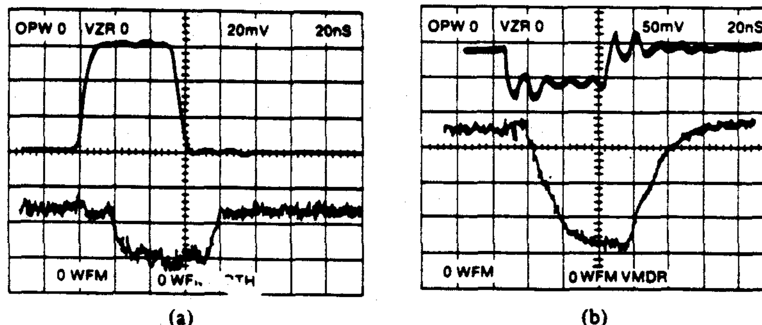


Fig. 2. Schematic layout of the high-frequency clocking system.



(a) (b)

Fig. 3. Input pulse (upper) and resulting output signal (lower) for clock drive frequencies of (a) 450 MHz and (b) 800 MHz. In case (a) the input was applied to the input gate whereas in (b) it was applied to the diode. Horizontal scale is 20 ns/major division.

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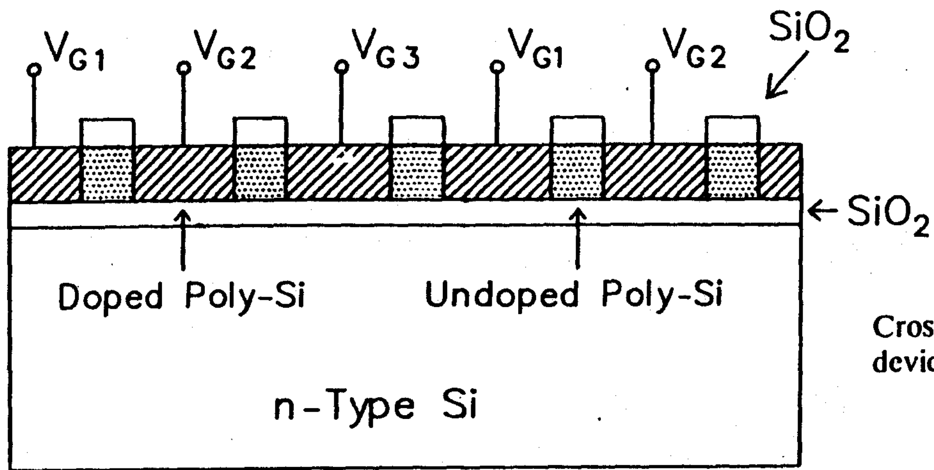
Resistive-Gate GaAs CCDs



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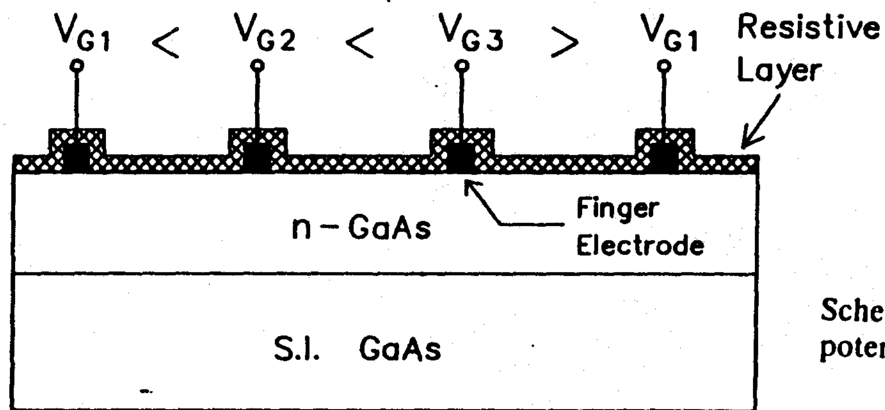
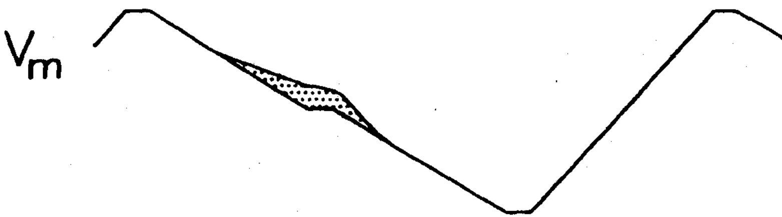
Cross section of a p-channel silicon resistive-gate charge-coupled device using a polysilicon as a resistive gate material. (Ref. 23.)





Schematic illustration of the device structure and channel potential of a GaAs resistive-gate charge-coupled device.

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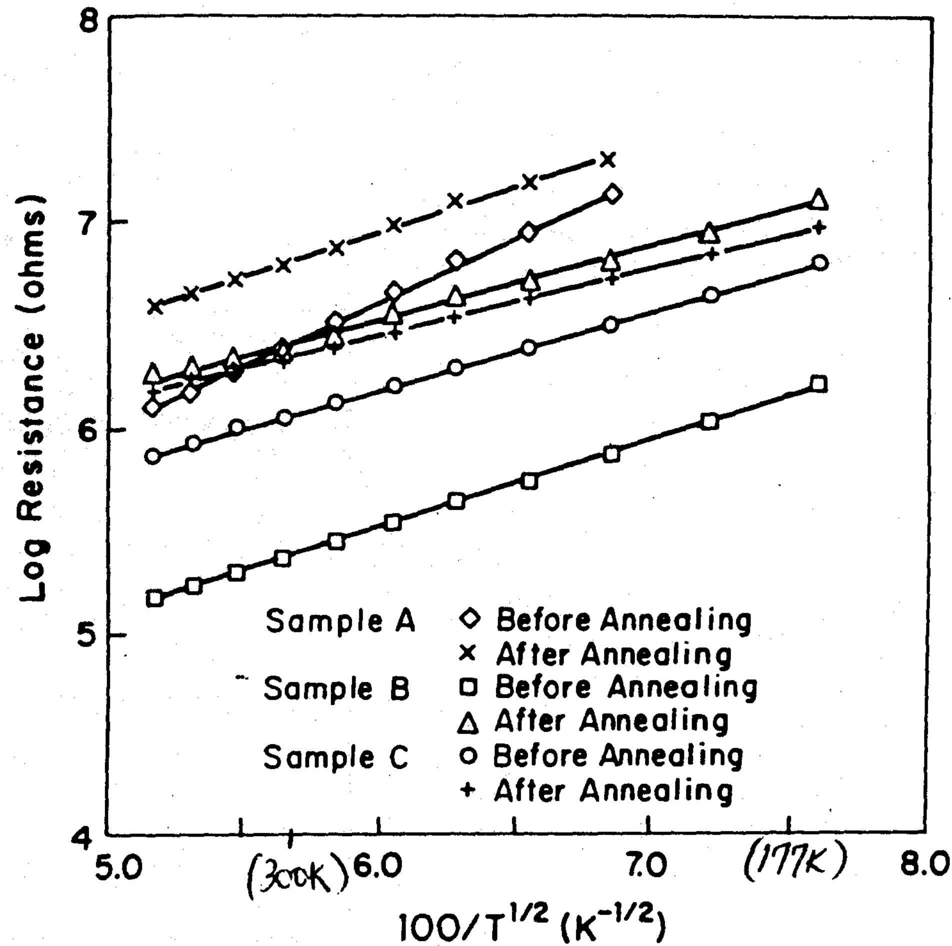

Temperature dependence of the sheet resistance of cermet films before and after annealing.

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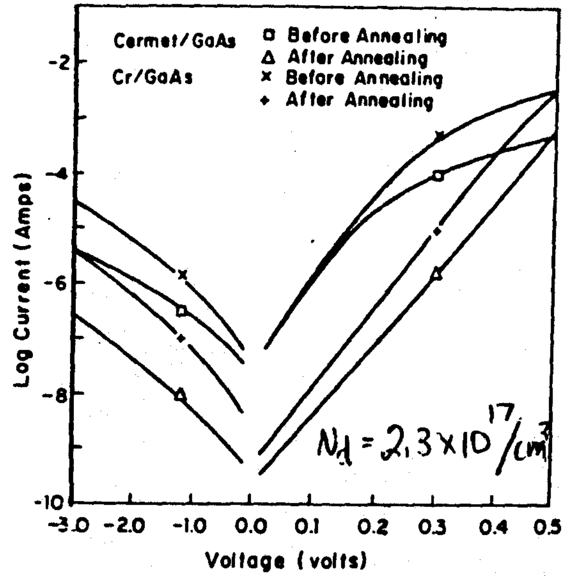
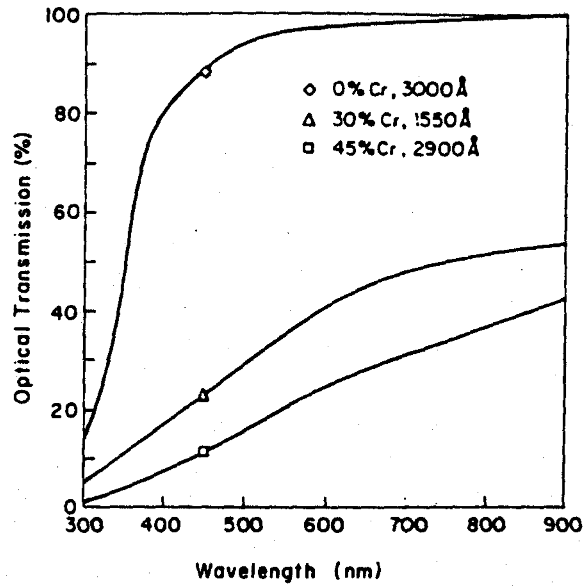
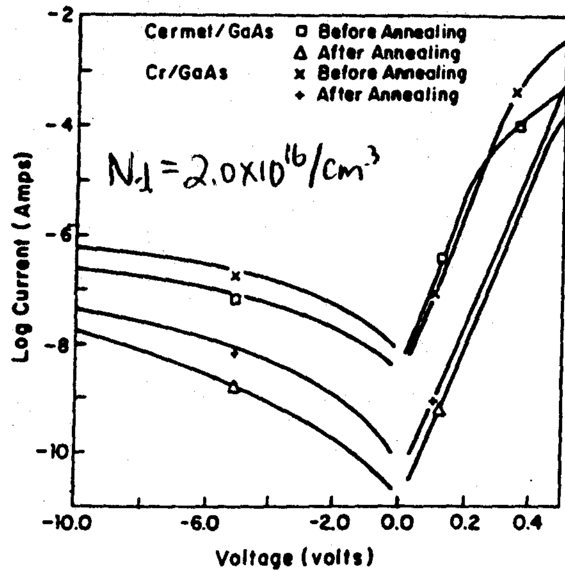
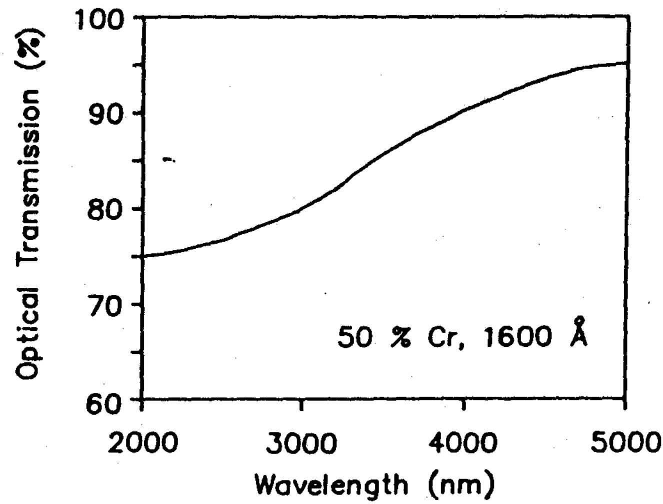
Cr-SiO Cermet









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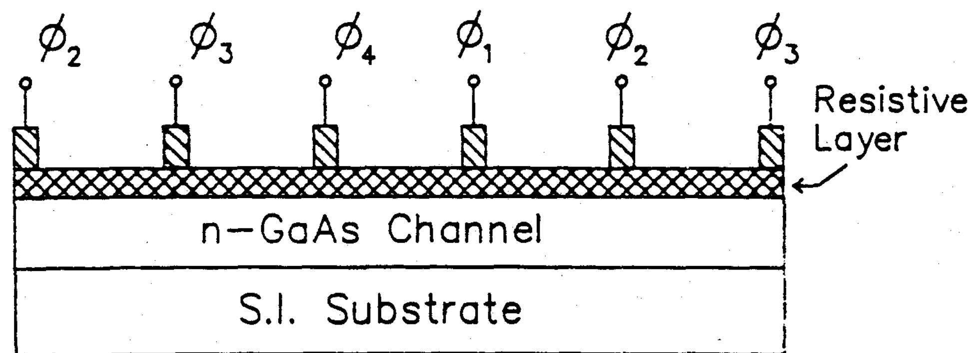
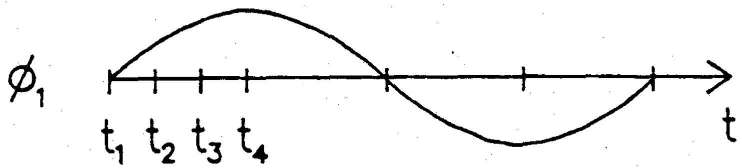


a)



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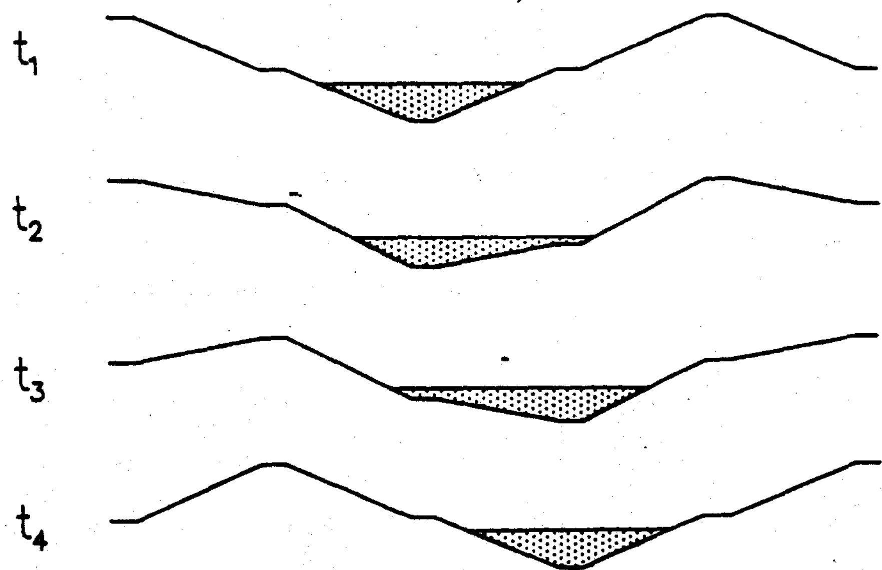
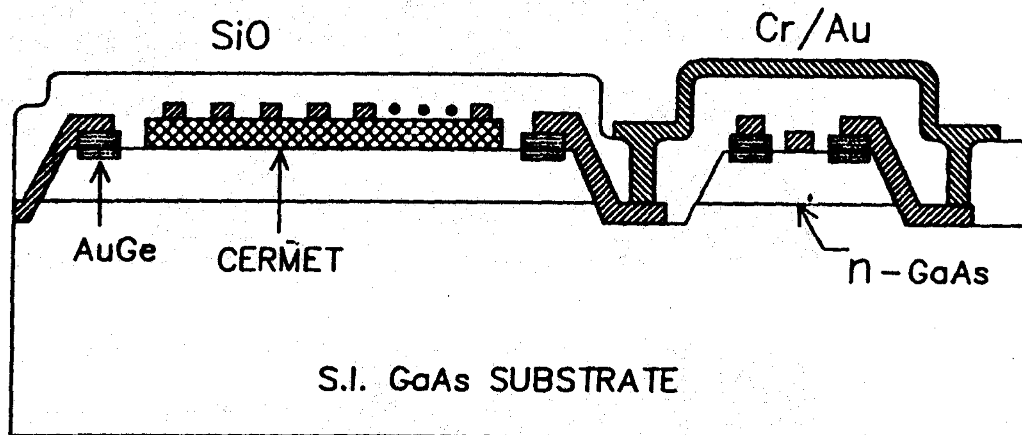
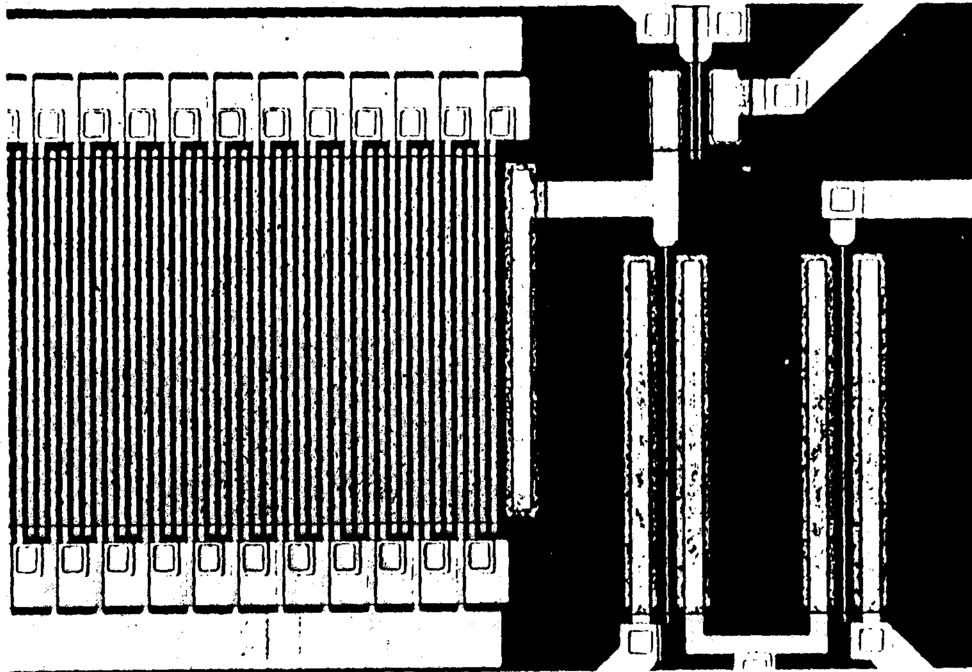


c)

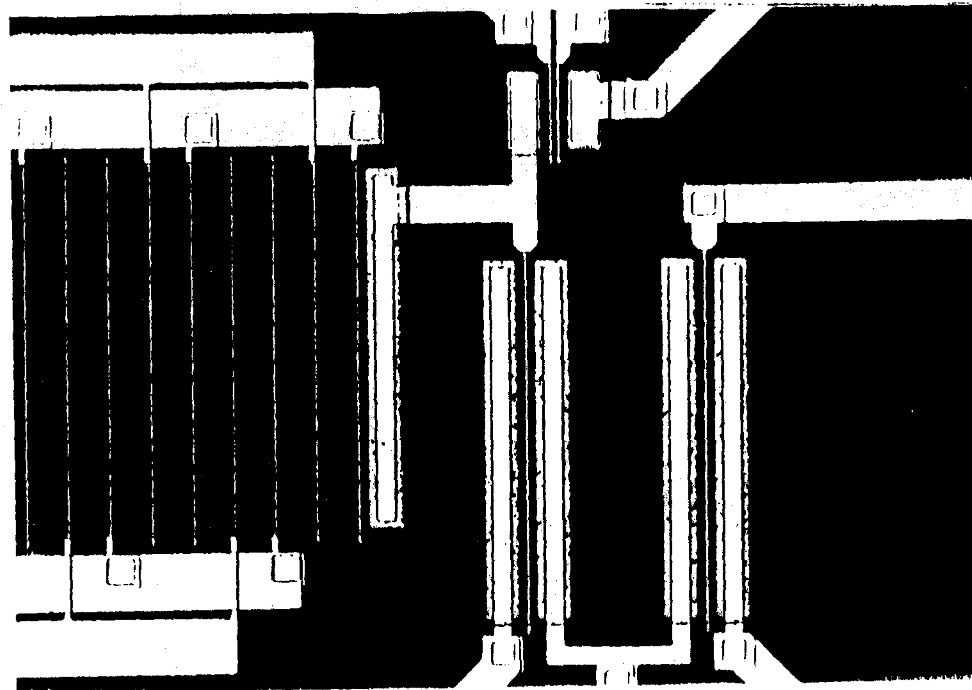
Four-phase operation of a GaAs resistive-gate charge-coupled device. a) Cross section of the device structure. b) Clock signal (ϕ_1). c) Evolution of the channel potential.



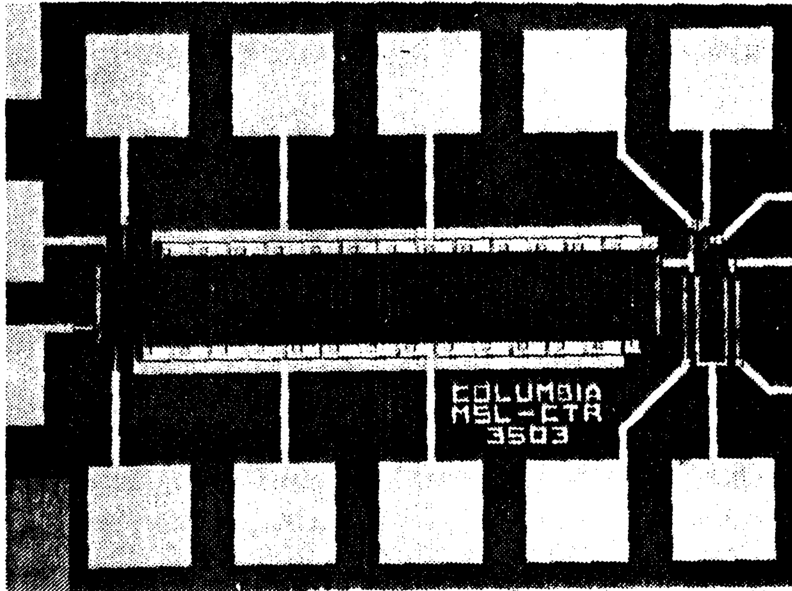
Schematic device cross section of a GaAs resistive-gate charge-coupled device.



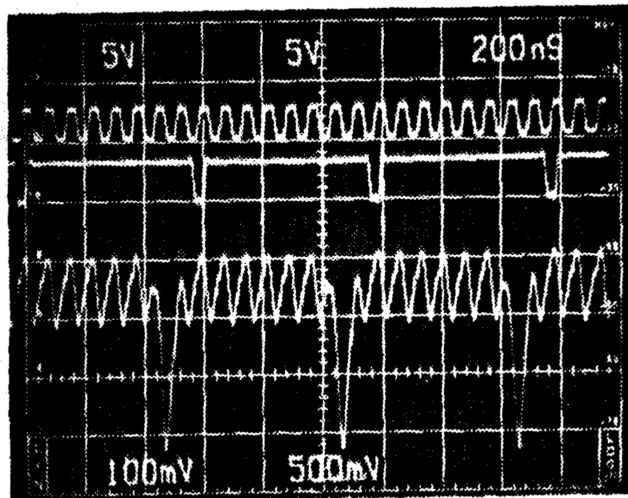
RGCCD with 2 um fingers spaced by 1 um



RGCCD with 1 um fingers spaced by 10 um



(a)



(b)

(a) Photograph of resistive-gate CCD delay line with 15 stages of four-phase electrodes. The channel is 100 μm wide and the electrodes are 1 μm wide spaced by 10 μm. The doping density of the channel is $2.0 \times 10^{17}/cm^3$, and thickness is 0.16 μm. The sheet resistance of the cermet was 850 k$\Omega/\square$ and 1200 Å thick. (b) Waveforms of delay line operated at 13-MHz clock frequency. Upper, middle, and bottom waveforms are one of the clock signals, input signal, and output signal of read-out amplifier, respectively.

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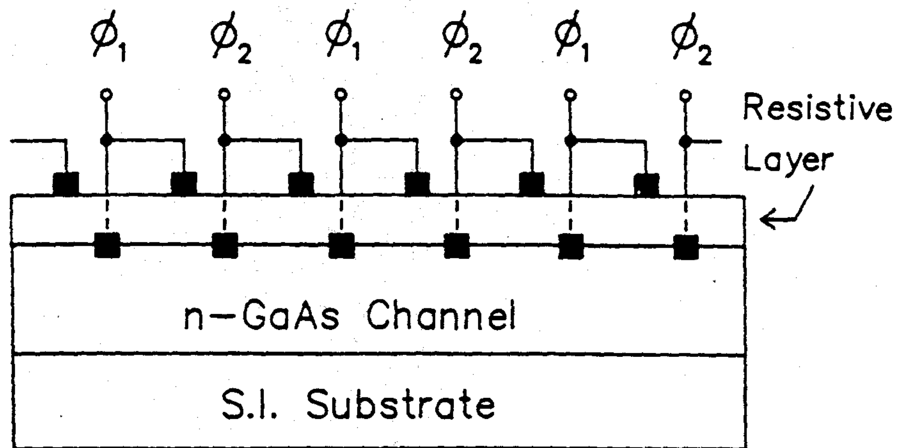
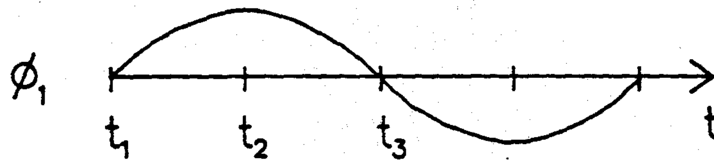
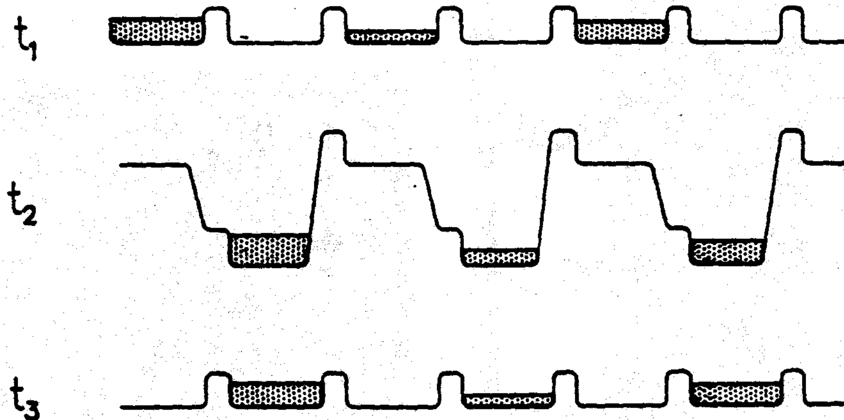


a)



b)



c)

Two-phase operation of a GaAs resistive-gate charge-coupled device. a) Cross section of the device structure. b) Clock signal (ϕ_1). c) Evolution of the channel potential.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 37, NO. 8, AUGUST 1990

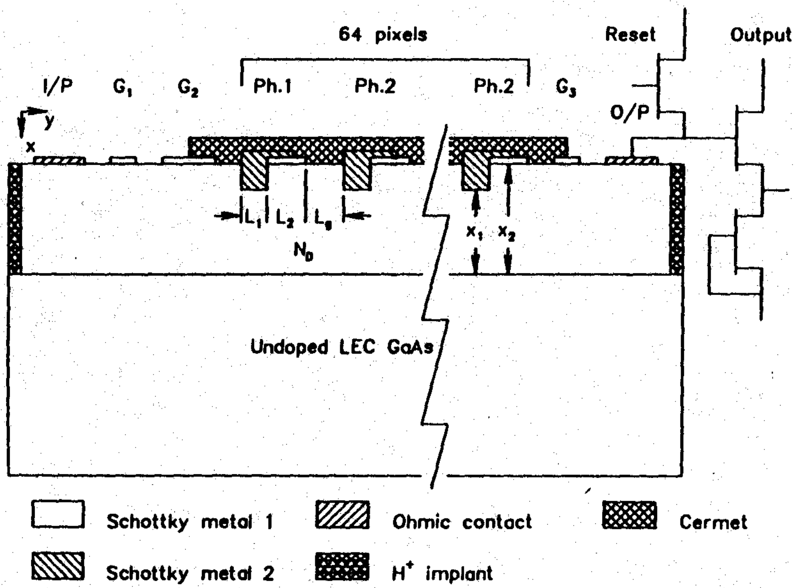
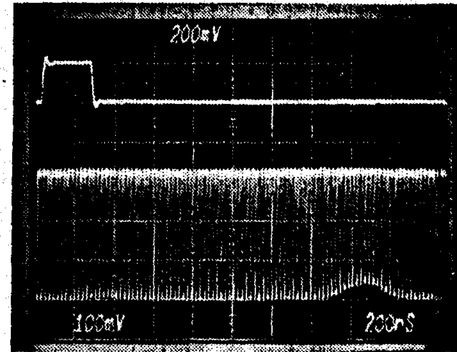
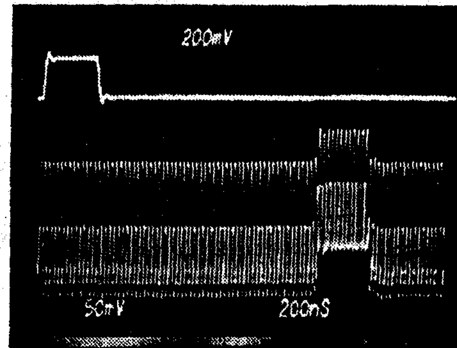


Fig. 1. A schematic cross-sectional view of the 2-phase GaAs CMCCD.



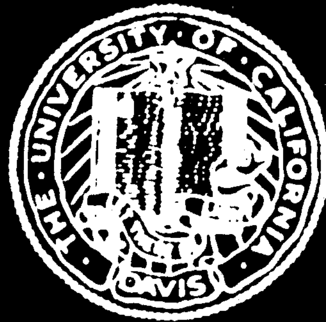
(a)



(b)

The 46-MHz performance of the 2-phase GaAs CMCCD: (a) using a 2-V amplitude clock and (b) using a 4-V amplitude clock.

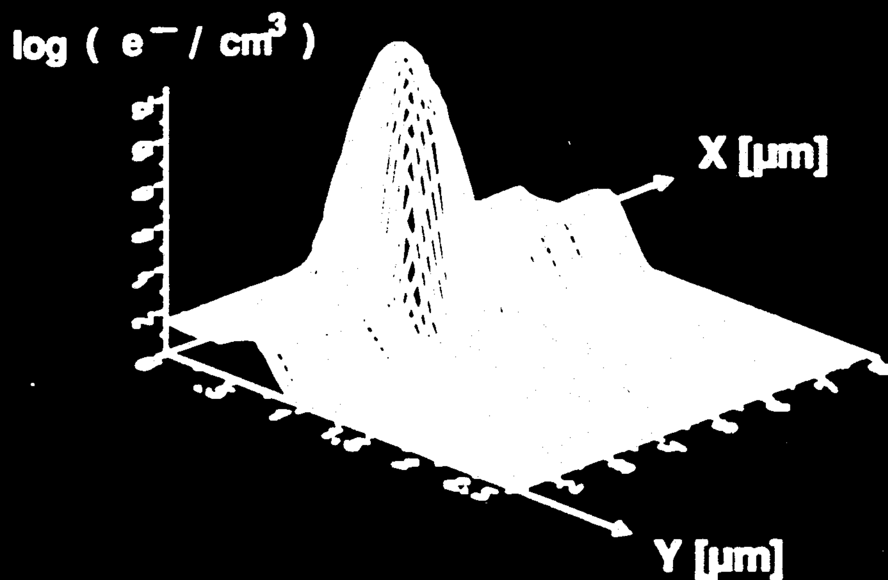
Modeling

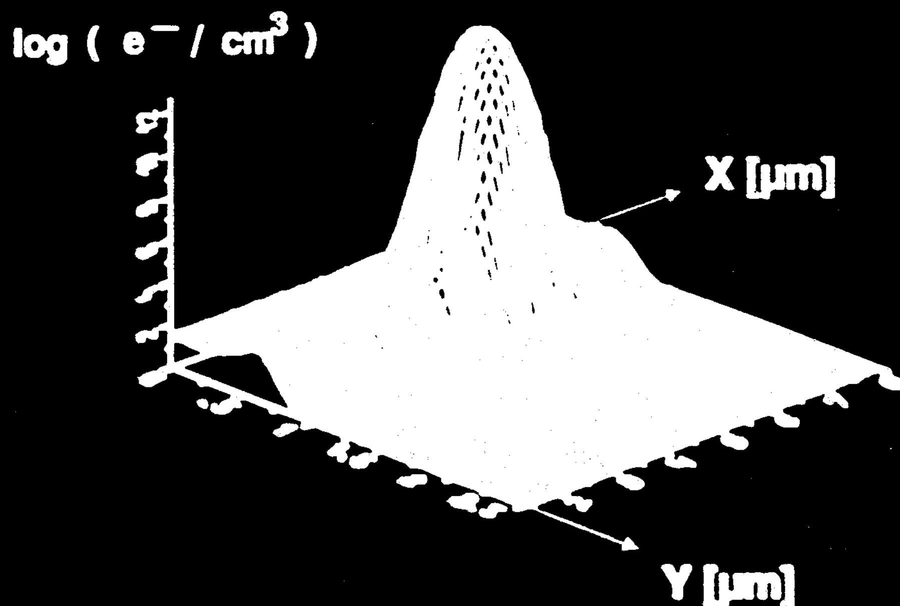


UC Davis

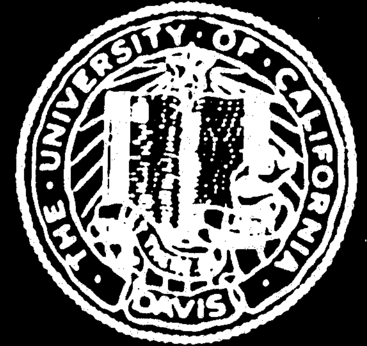
- 2-D finite-difference device simulation program: Basic Analyzer for Mos and BIpolar devices (BAMBI)
- General purpose solver of the three basic semiconductor differential equations
- Solves arbitrary configurations with externally supplied parameters
- Developed at Technical University, Vienna, by Prof. S. Selberherr and associates
- Kind help of Gerd Nanz from Digital Equipment Corporation, Vienna (formerly of Technical University of Vienna) acknowledged

Measurement of Charge Transfer Efficiency



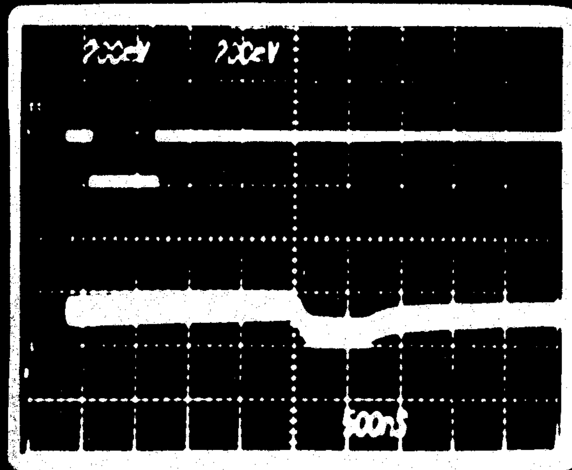


Measured electrical input and delayed output signal for a RGCCD

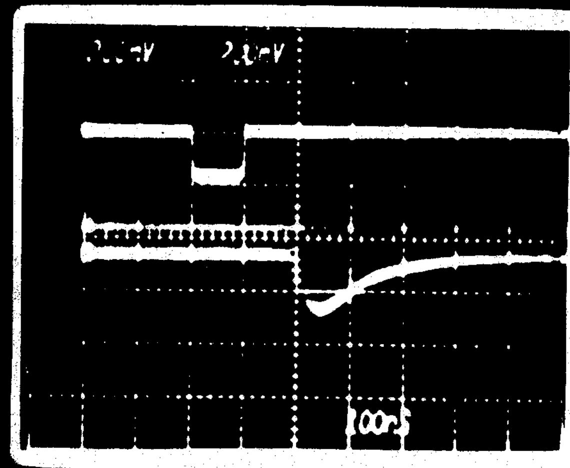


UC Davis

- 16 cells 3-Phase RGCCD
- 1.75μm gate length with 3.0μm gate pitch
- 200nm MBE grown active layer
- Electrically induced charge packet

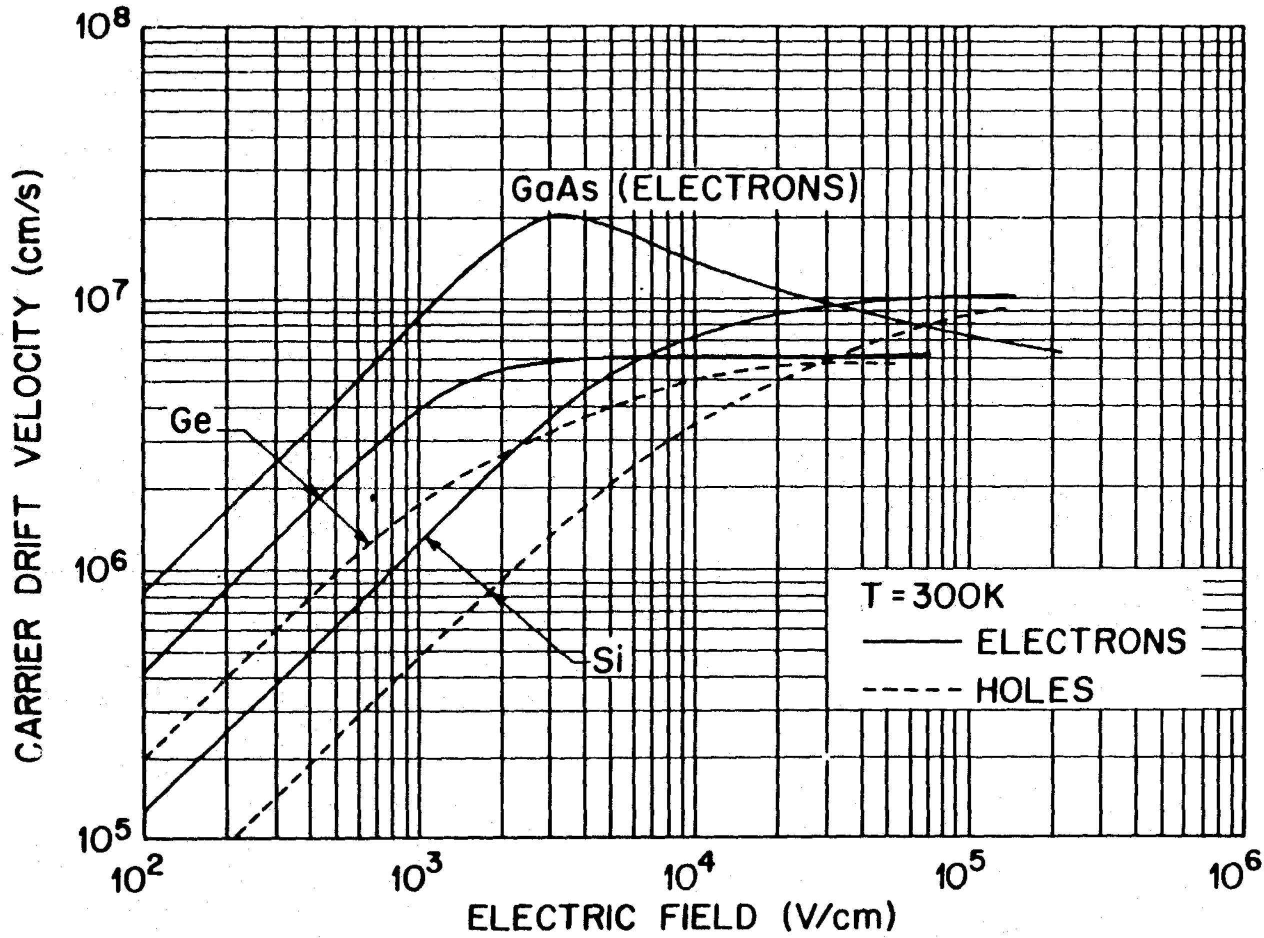


20 MHz Clock



290 MHz Clock

JPL
Jet Propulsion Laboratory
California Institute of Technology



Inhibition of charge packet broadening in GaAs charge-coupled devices

J. I. Song and E. R. Fossum
Department of Electrical Engineering and Center for Telecommunications Research, Columbia University, New York, New York 10027

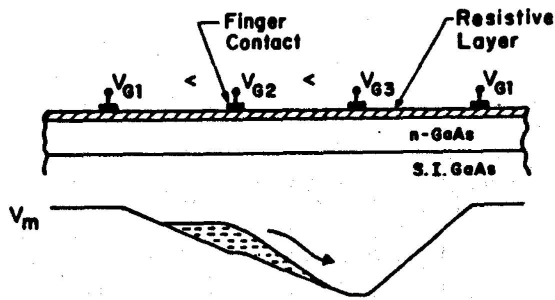


FIG. 1. Schematic illustration of the device structure and channel potential of a resistive-gate charge-coupled device.

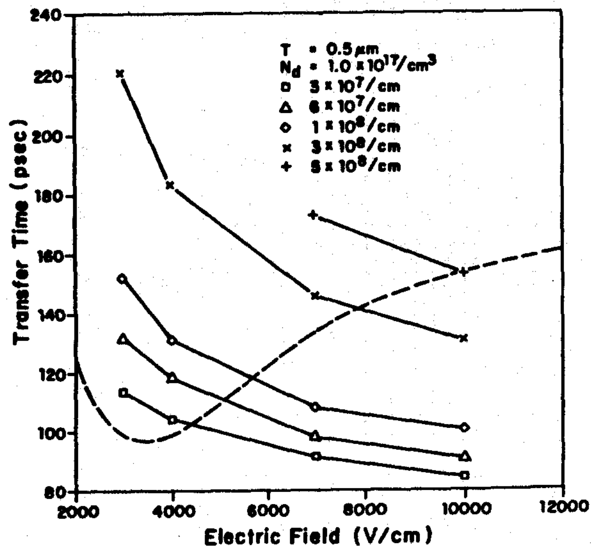


FIG. 4. Transfer time as a function of applied electric field for different charge packet sizes. The dashed line shows the transit time between two electrodes spaced by 10 μm, as explained in the text.

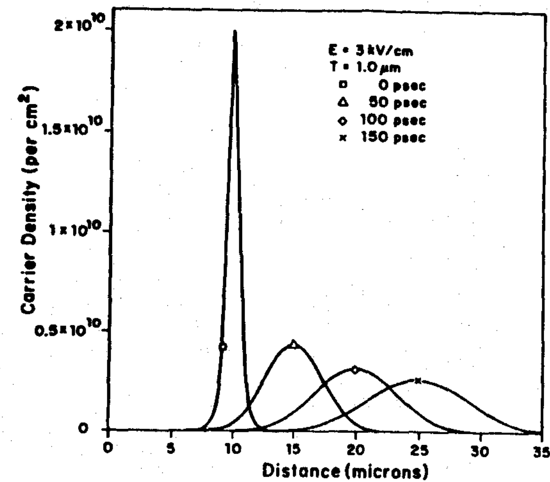


FIG. 2. Evolution of a charge packet with applied electric field of 3 kV/cm and a size of 2.5×10^6 electrons/cm. The charge packet broadens due to diffusion and self-repulsion effects. (Charge packet size is normalized by the channel width.)

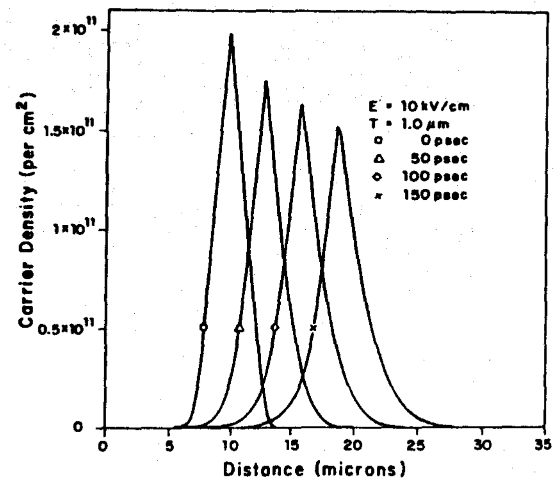


FIG. 3. Evolution of a charge packet with an applied electric field of 10 kV/cm and a size of 6.0×10^7 electrons/cm. The broadening of the charge packet is inhibited by transferred-electron effects.

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COLUMBIA UNIVERSITY
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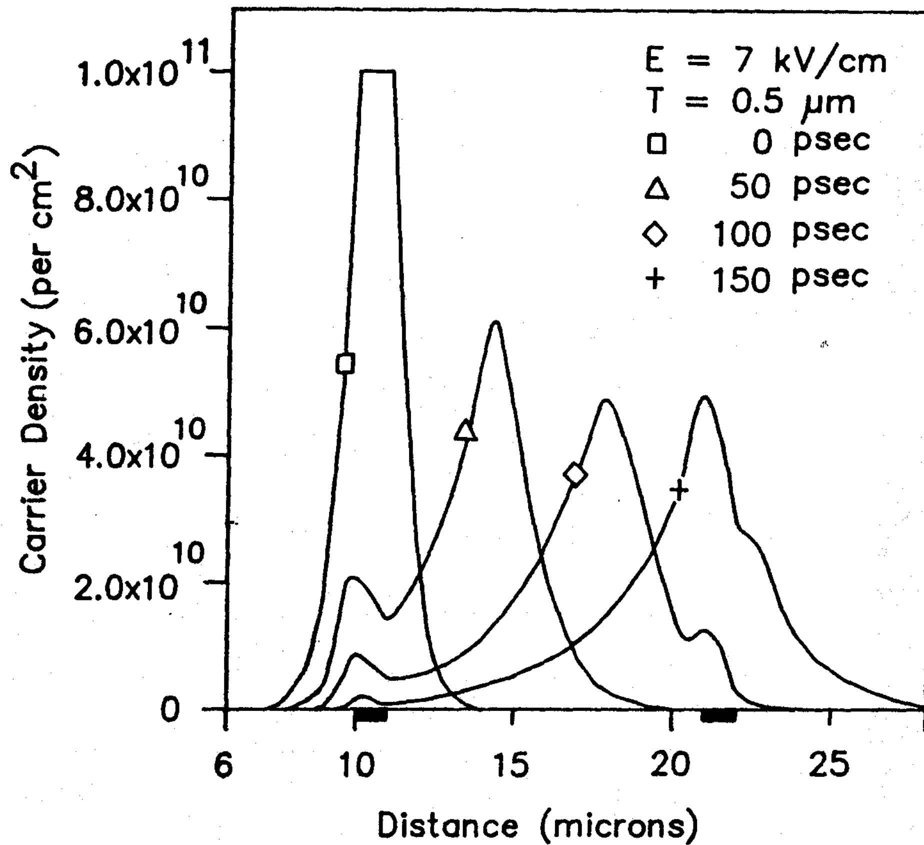
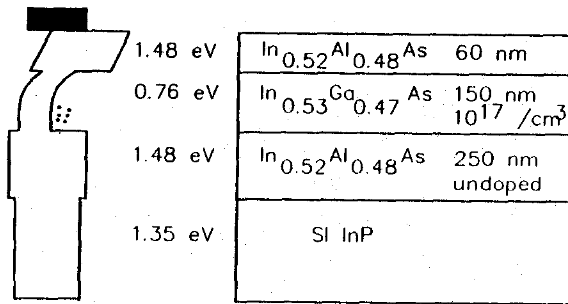


Evolution of a charge packet with an applied electric field of 7 kV/cm. Width of potential flats is 1 μm, as shown on the x-coordinate. Pile up of carriers is observed on the potential flat regions.

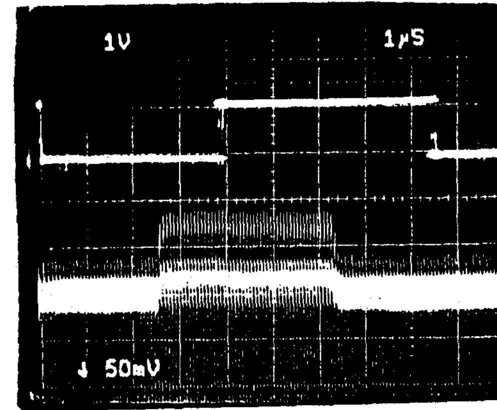
InGaAs/InP Heterostructure CCD

4-Phase, 33-Stage, 28 um Pixel, RGCCD

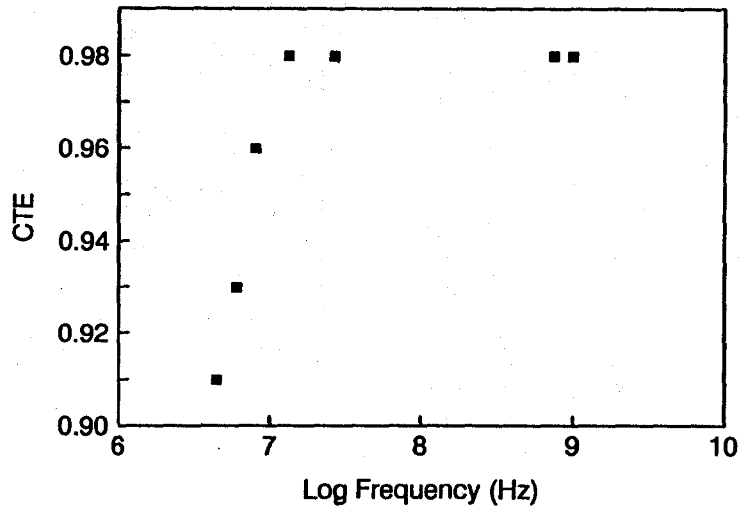
Rossi et al., Columbia University

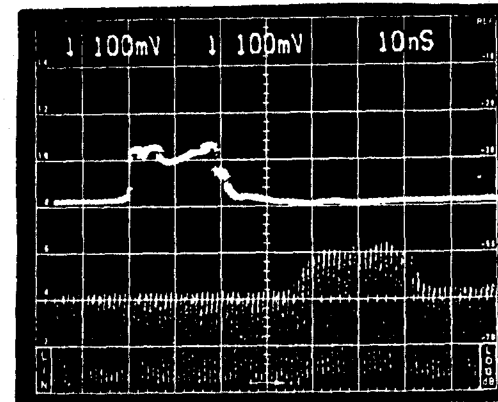


Layer	Thickness / doping
$In_{0.52}Al_{0.48}As$	60 nm
$In_{0.53}Ga_{0.47}As$	150 nm 10^{17} /cm^3
$In_{0.52}Al_{0.48}As$	250 nm undoped
SI InP	



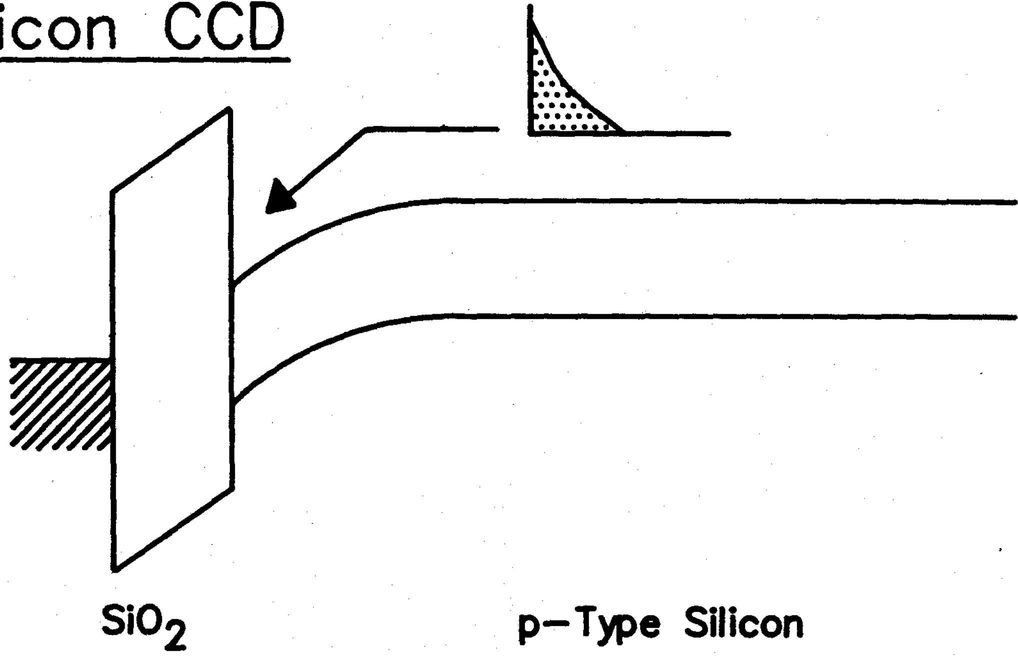
Cooled, 13 MHz

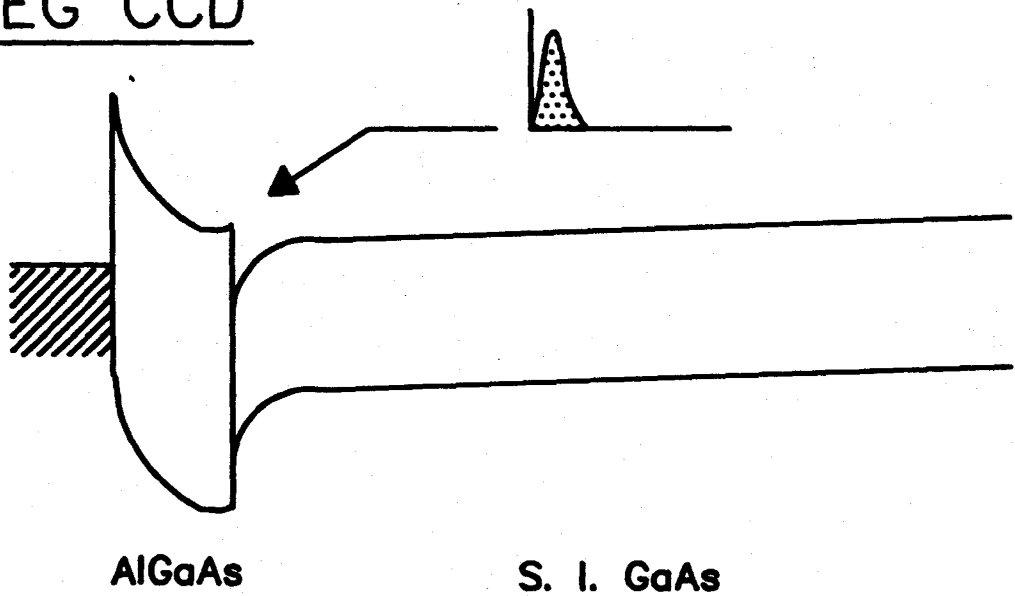




Room Temp. 1 GHz

2 DEG-CCDs


Silicon CCD
SiO$_2$
p-Type Silicon


2DEG CCD
AlGaAs
S. I. GaAs

ADVANTAGES OF AlGaAs / GaAs 2DEG-CCDs

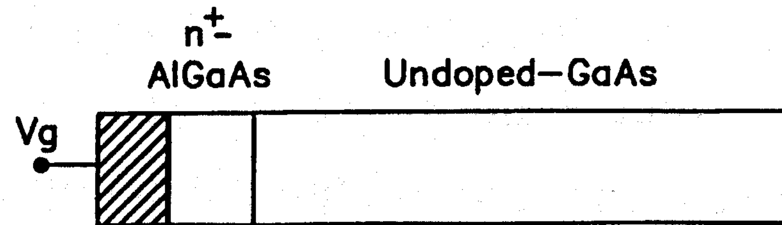
- High charge handling capability

  $n_s > 10^{12}$ carriers / cm^2
- Lattice-matched interface
- Very high speed operation possible

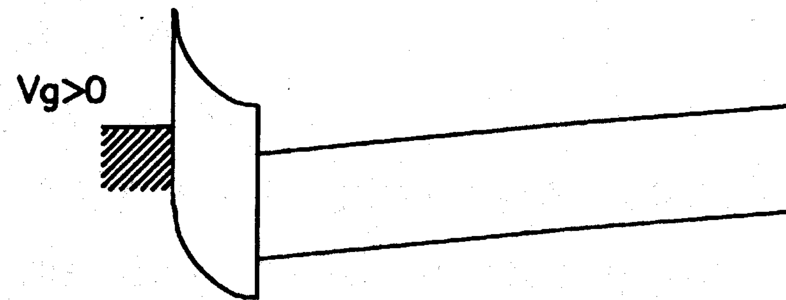
  mobility > 5000 cm^2/V-sec at RT
- Low clock swing
- Radiation-hard

  no oxide
- Fabrication compatibility with III-V IR detectors
- Natural anti-blooming Schottky gate
- Very low temperature operation

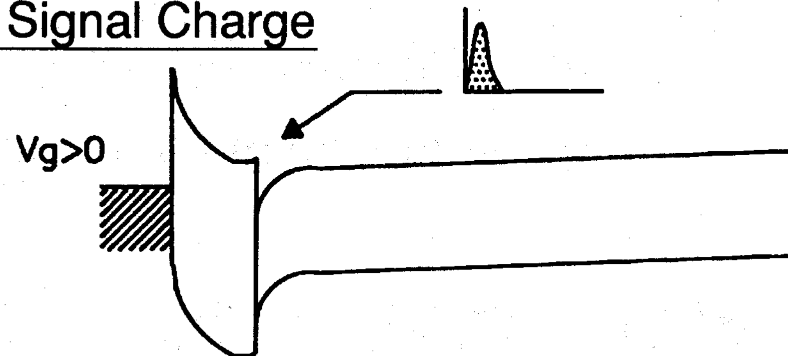
BAND DIAGRAM OF 2DEG CCD



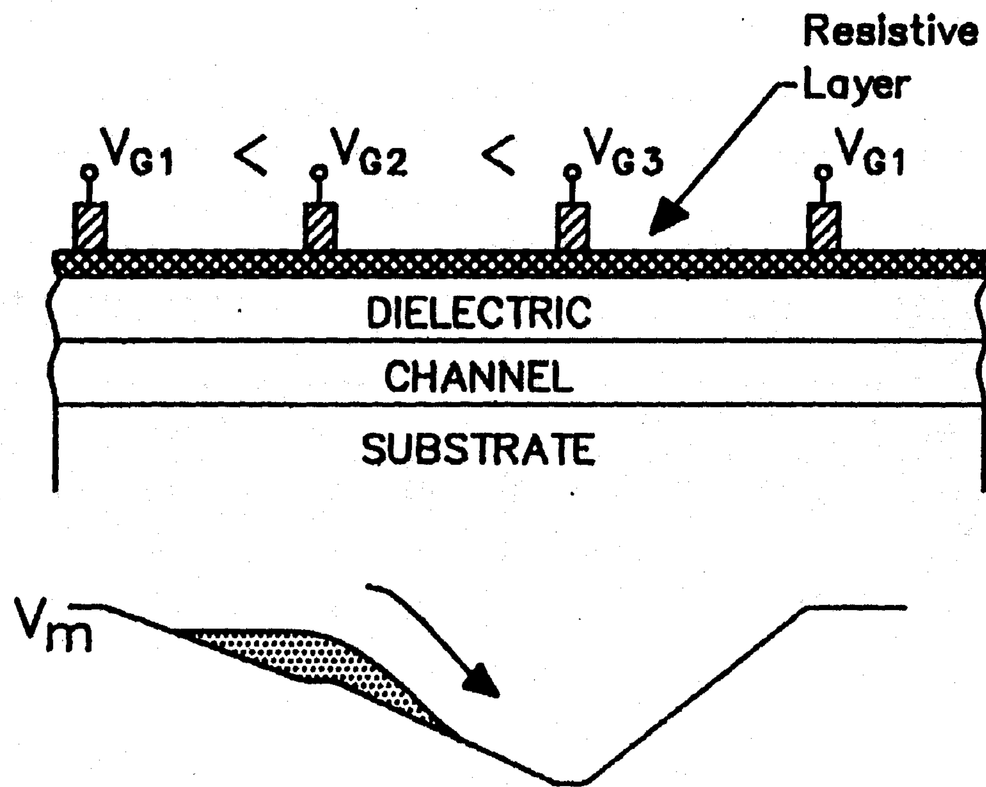
Without Signal Charge



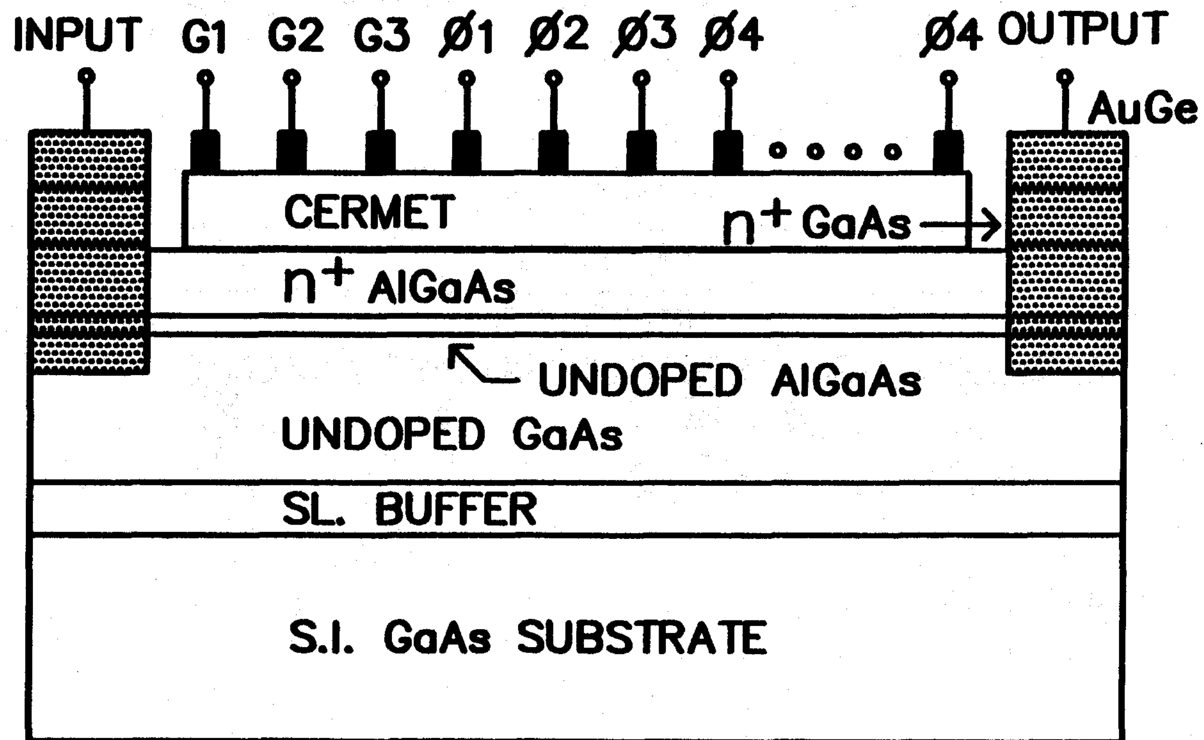
With Signal Charge

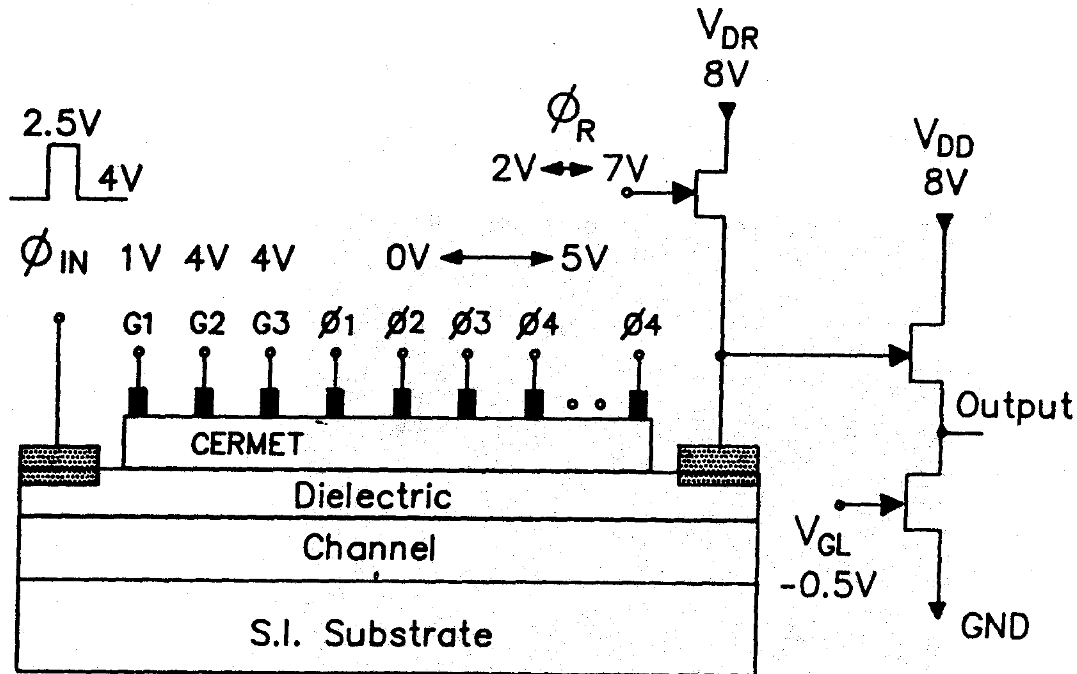


RESISTIVE-GATE 2DEG-CCD



DEVICE STRUCTURE OF 2DEG RGCCD





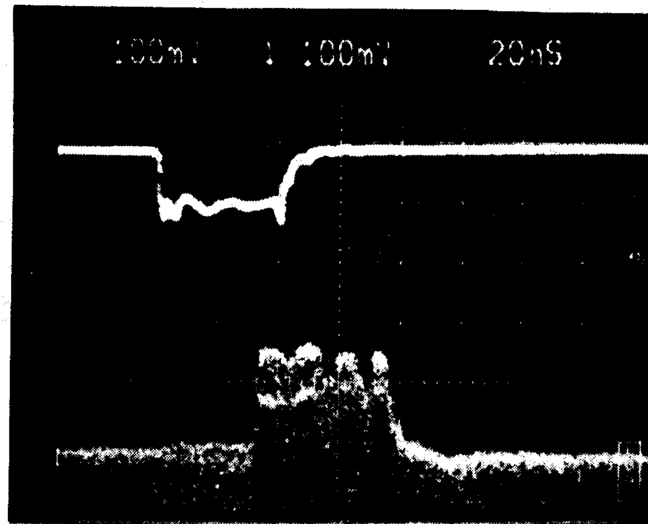
Typical bias conditions for the test of a 2DEG RGCCD delay line. The pinch-off voltage of the CCD channel and 2DEGFET is assumed to be -1.0 V.

OPERATION OF 2DEG RGCCDs

Room Temperature

4 Phase Clocking, 32 Stages (128 Transfers)

1 um Electrode Width, 4 um Spacing, 100 um Channel Width

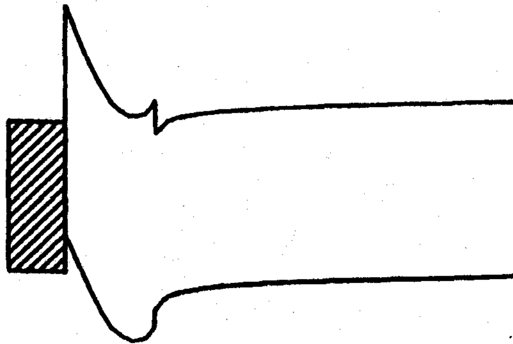


Uniform–Doped 2DEG RGCCD

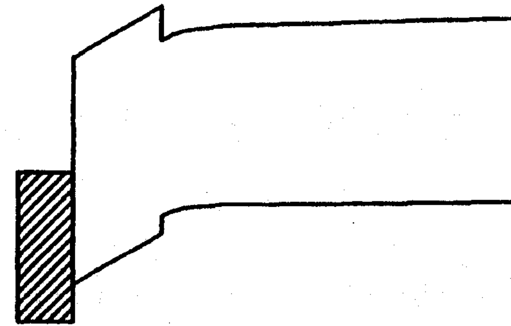
CTE = 0.999 At 1 GHz

2DEG-CCD STRUCTURES

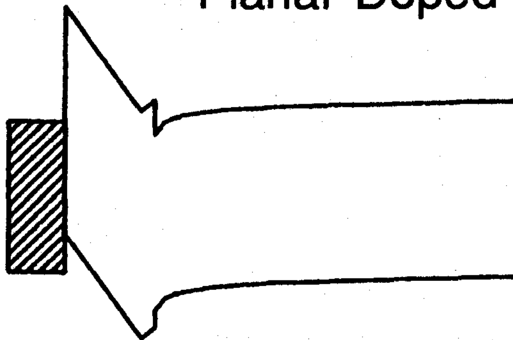
Uniform-Doped



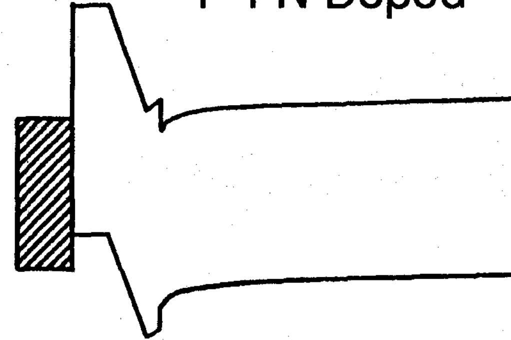
Undoped



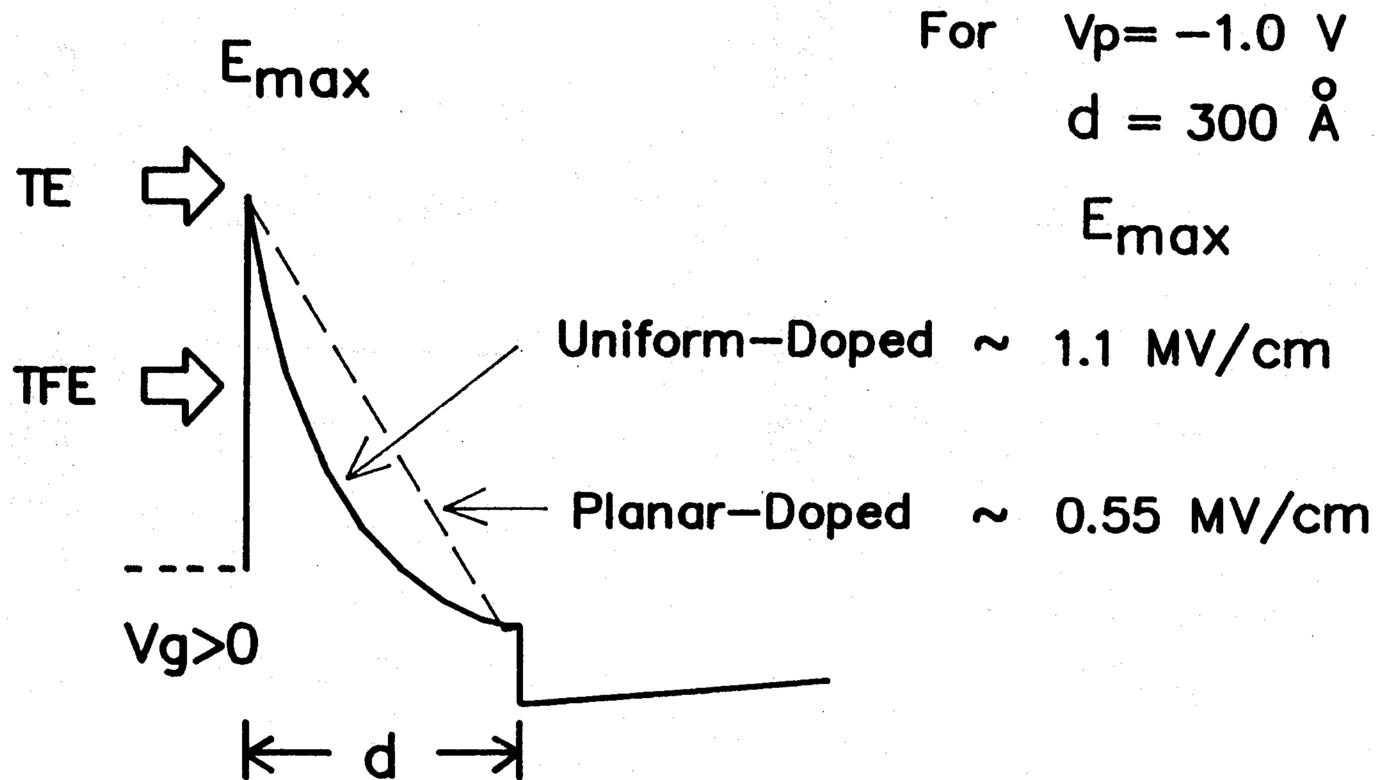
Planar-Doped



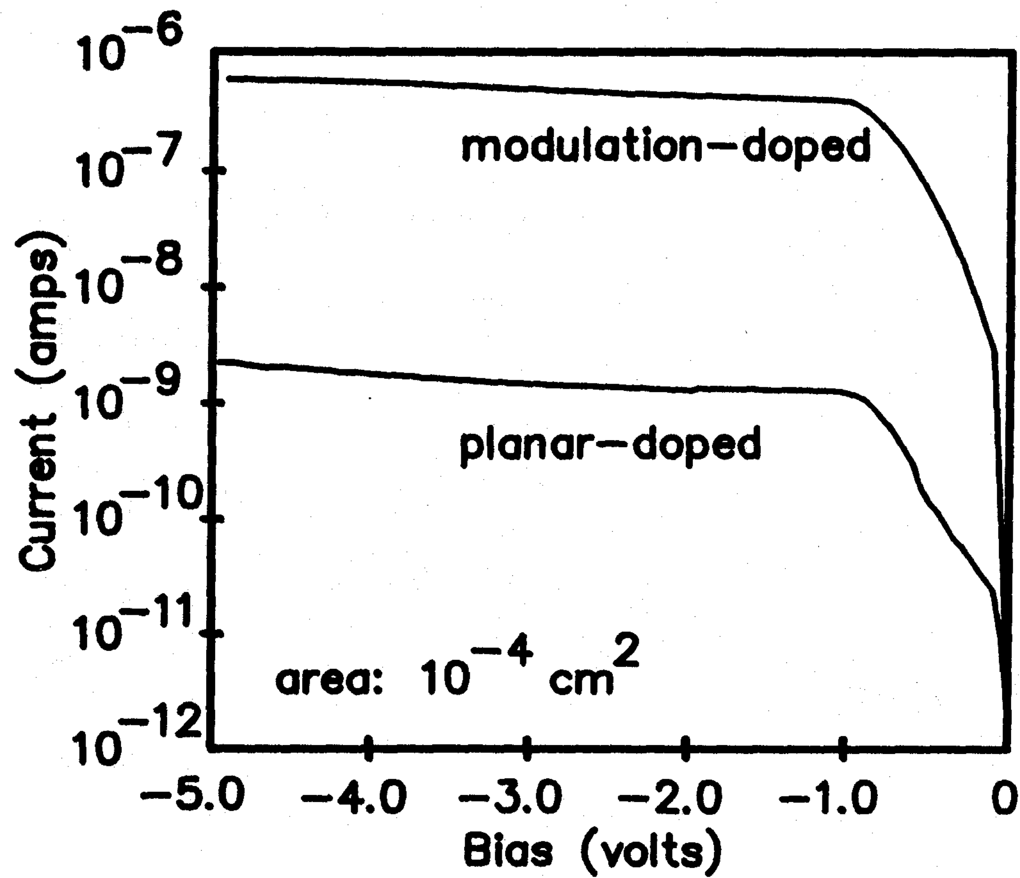
P-I-N Doped



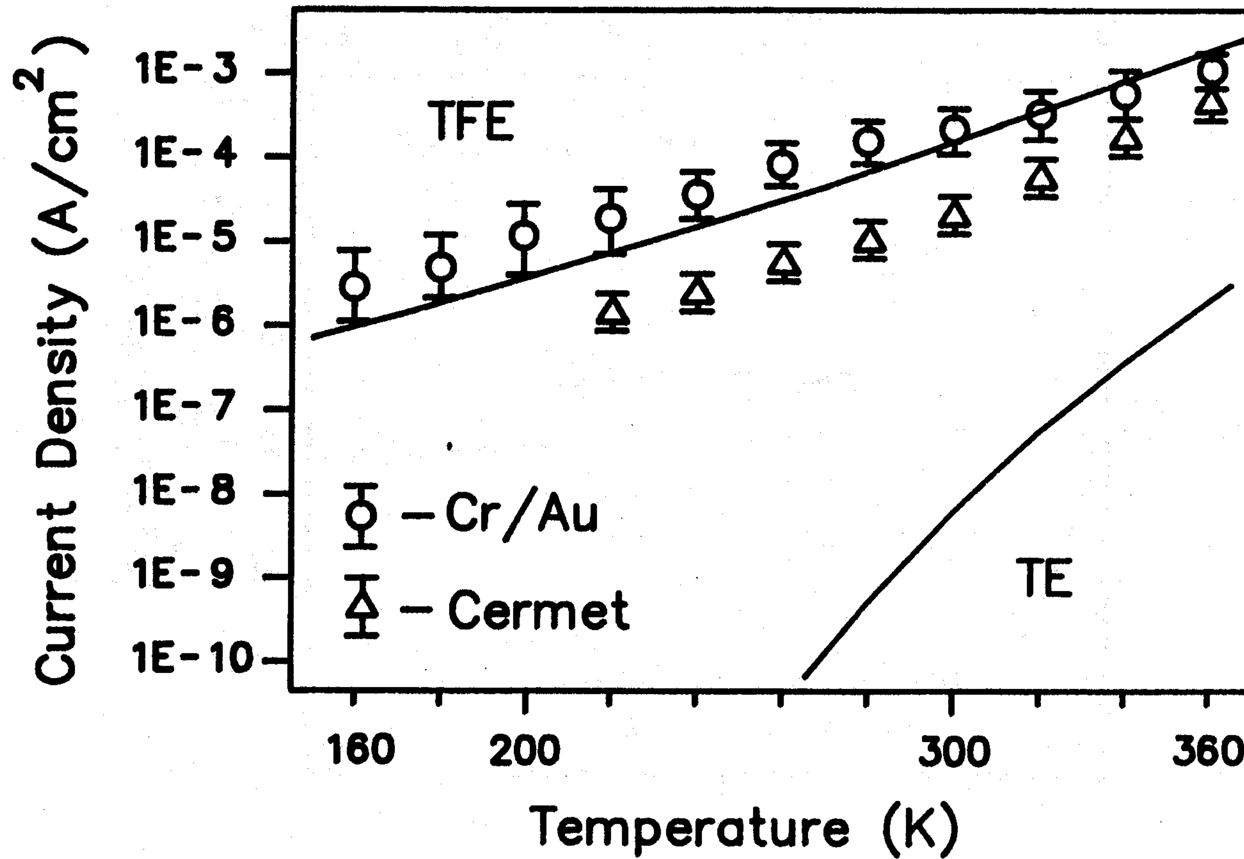
UNIFORM- vs. PLANAR-DOPED 2DEG CCD



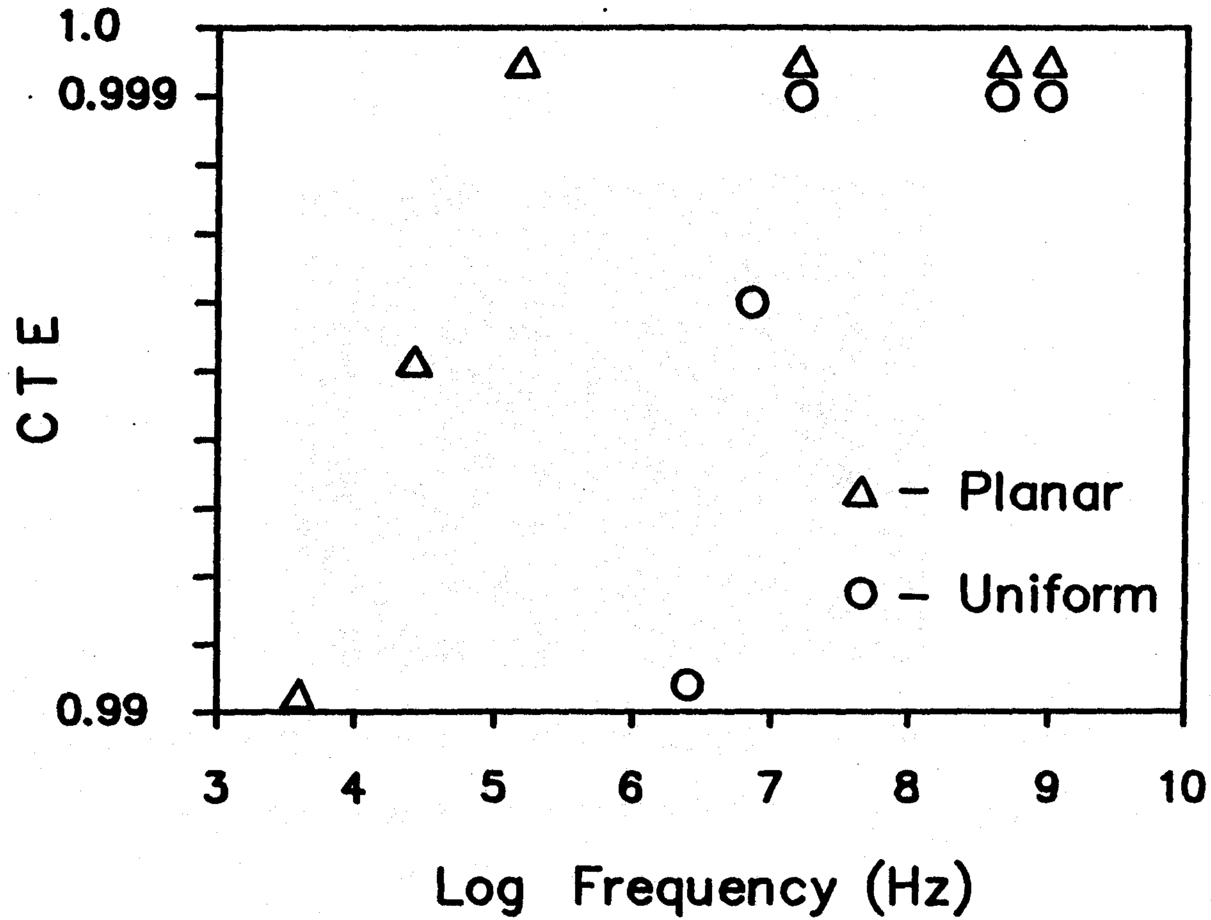
GATE LEAKAGE CURRENT



GATE LEAKAGE vs. TEMPERATURE



CTE OF 2DEG CCDs

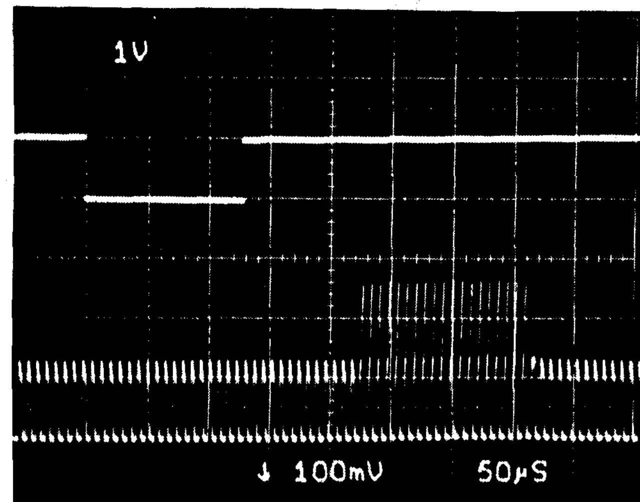


OPERATION OF 2DEG RGCCDs

Room Temperature

4 Phase Clocking, 32 Stages (128 Transfers)

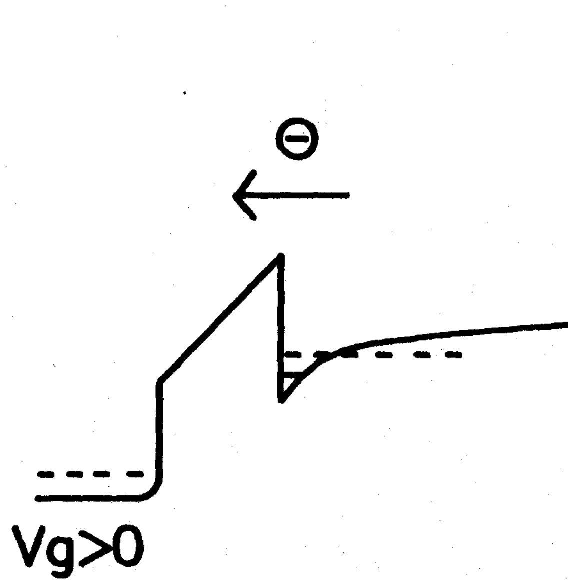
1 um Electrode Width, 4 um Spacing, 100 um Channel Width

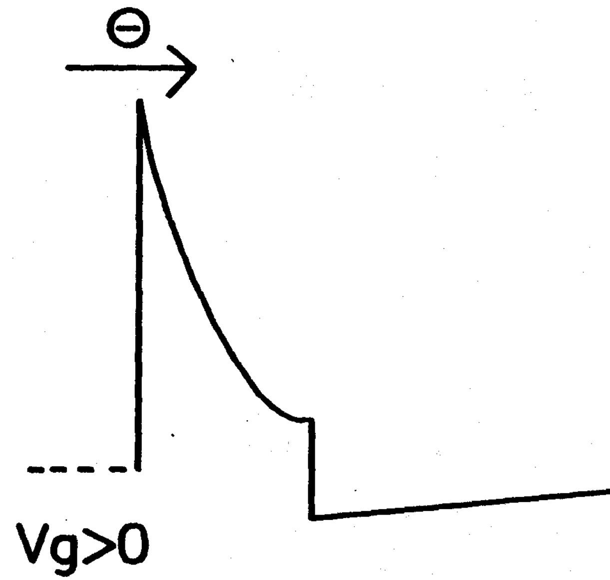


Planar-Doped 2DEG RGCCD

CTE > 0.999 At 133 KHz

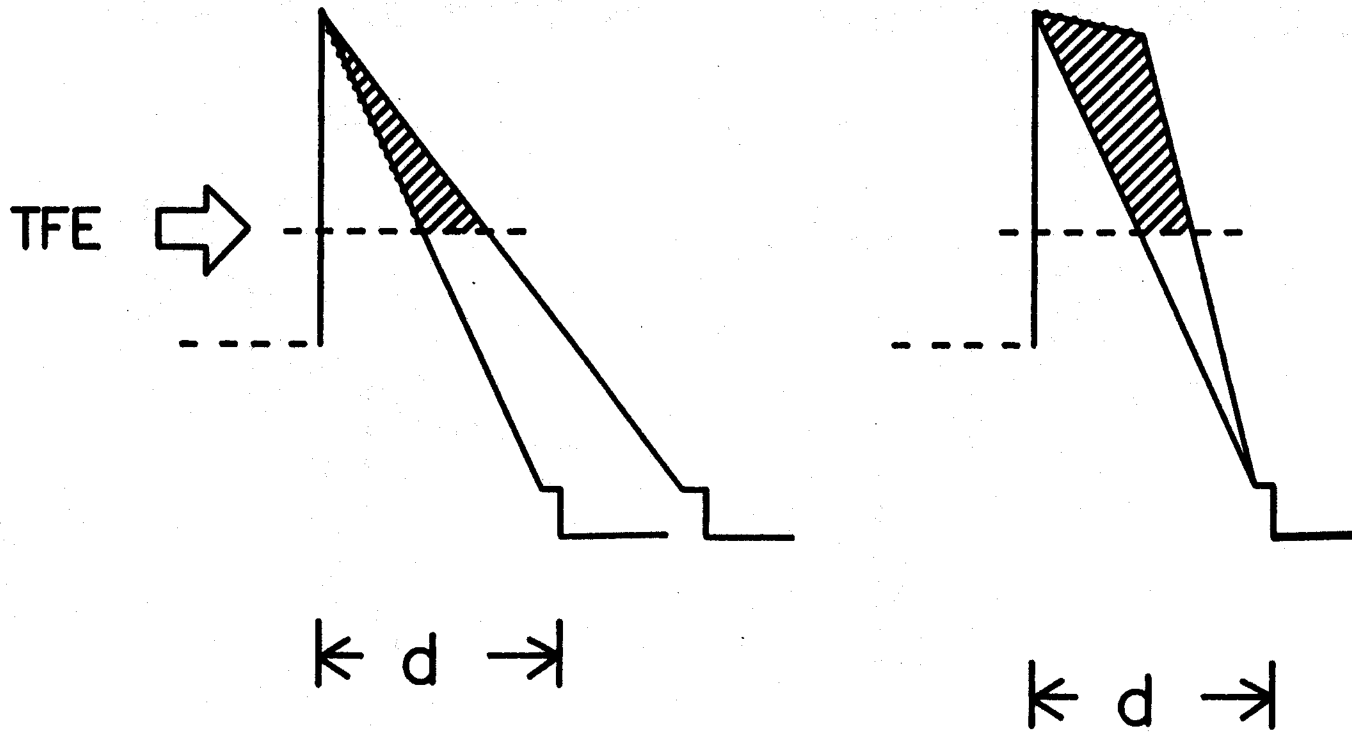
HIG CCD vs. MOD CCD



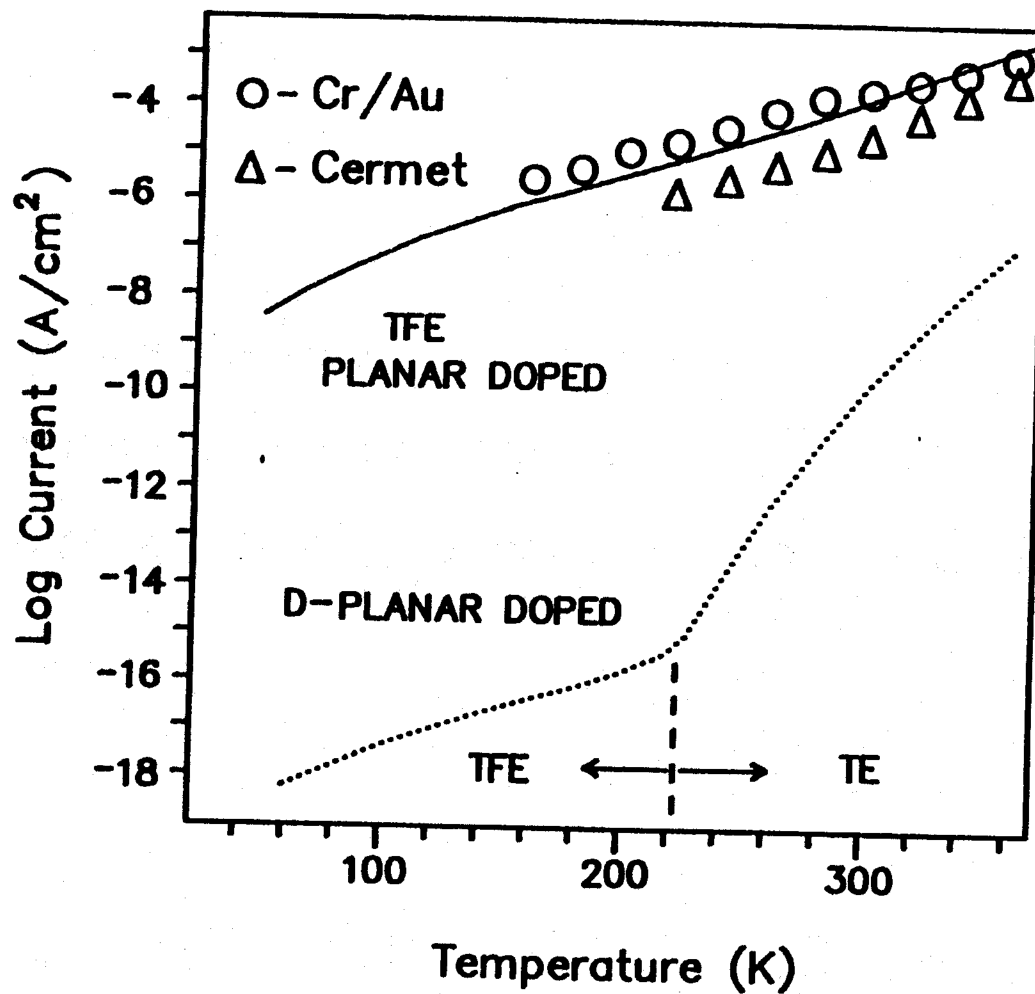


ΔE_c	ϕ_{Bn}
~0.3 eV, AlGaAs/GaAs	~ 0.9 eV, AlGaAs/GaAs
~0.48 eV, InAlAs/InGaAs	~ 0.7 eV, InAlAs/InGaAs

DUAL-PLANAR-DOPED CCD ?



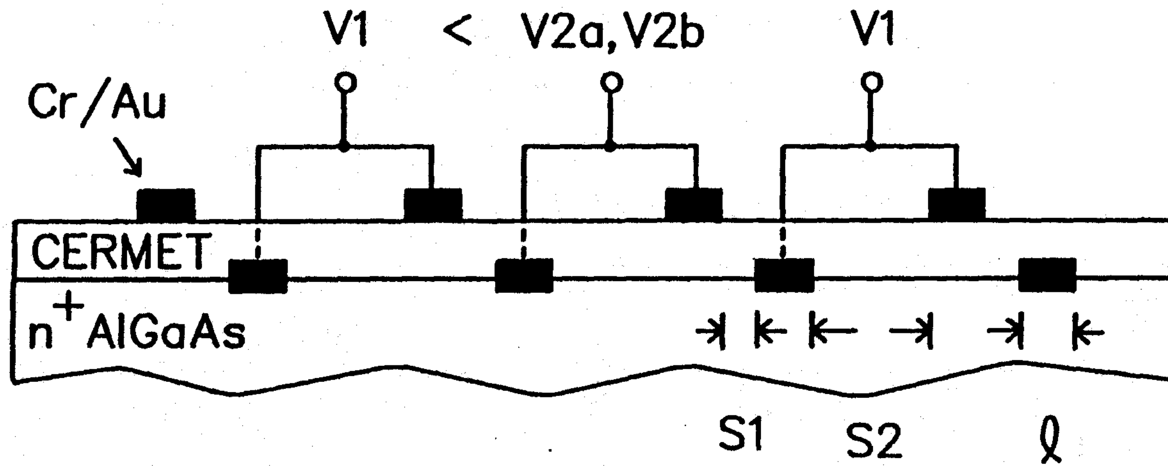
DARK CURRENT IN 2DEG-CCDs

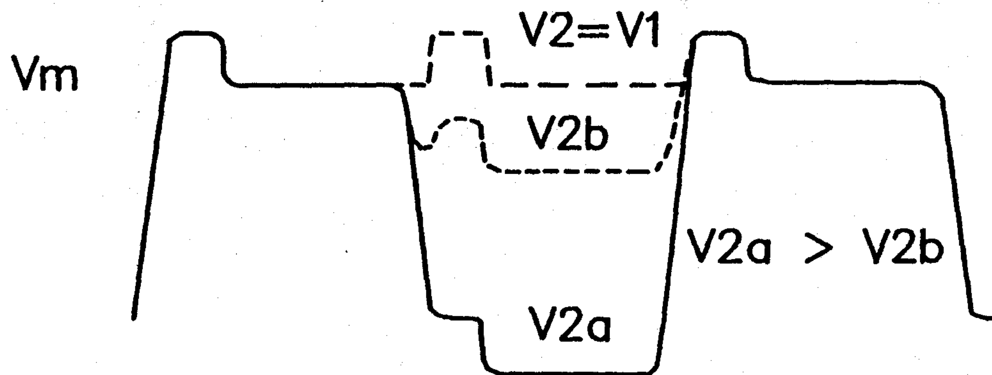


TWO-PHASE 2DEG-CCD MOTIVATION

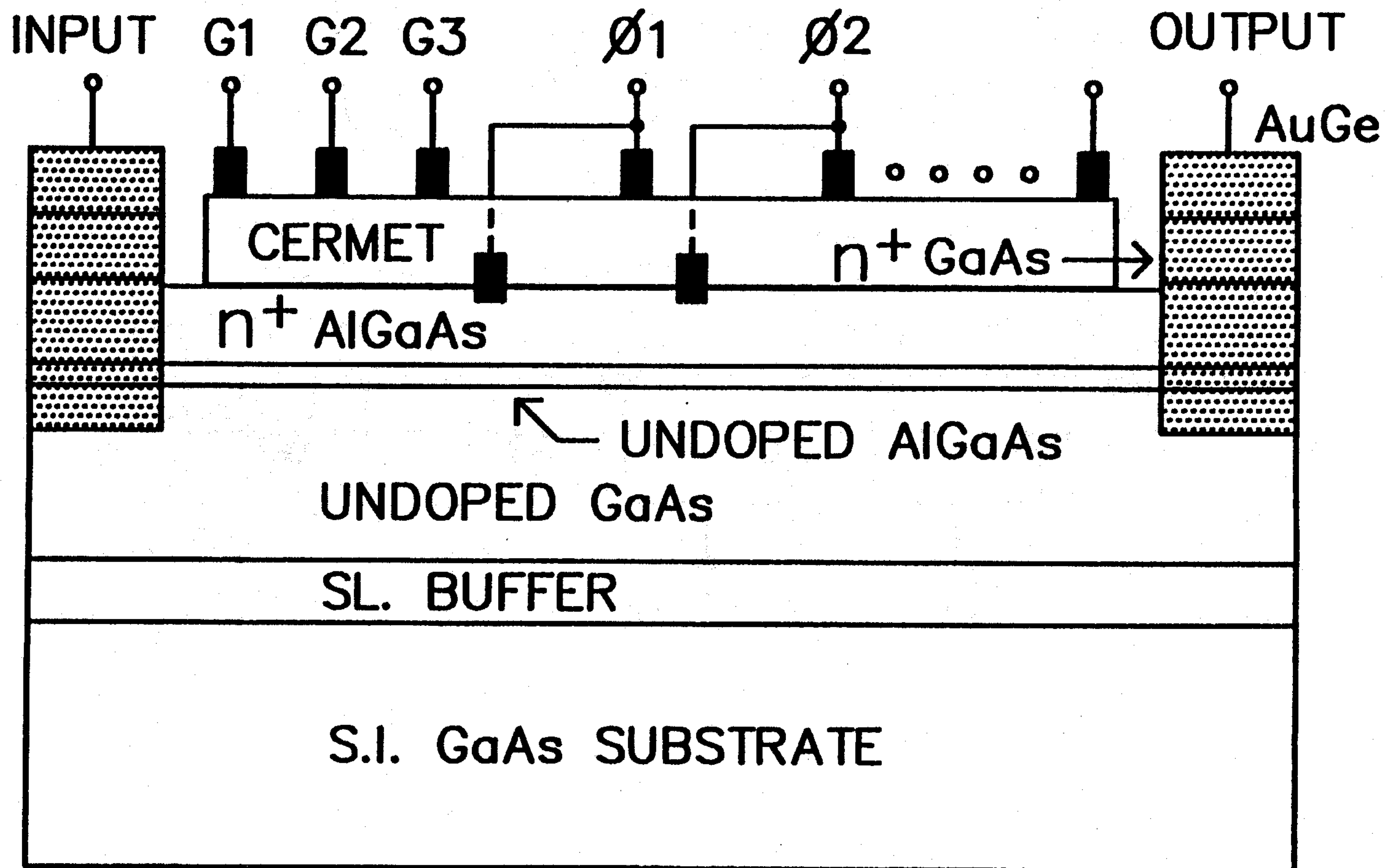
- No dc power dissipation in resistive gate during frame integration
- Reduced number of clock drivers
- High effective fill-factor

TWO-PHASE 2DEG-CCD



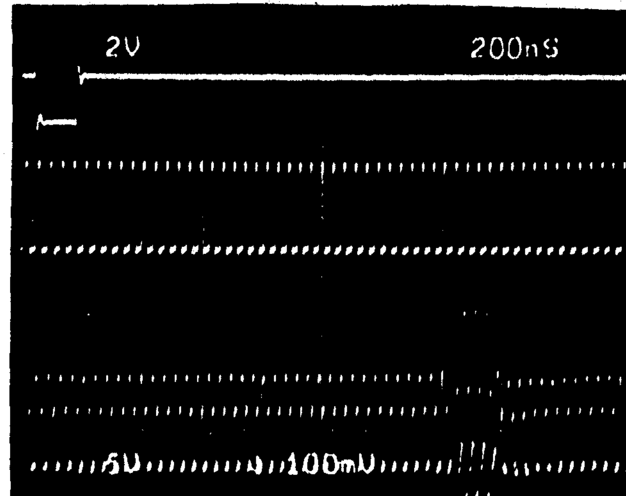


PHYSICAL LAYER STRUCTURE



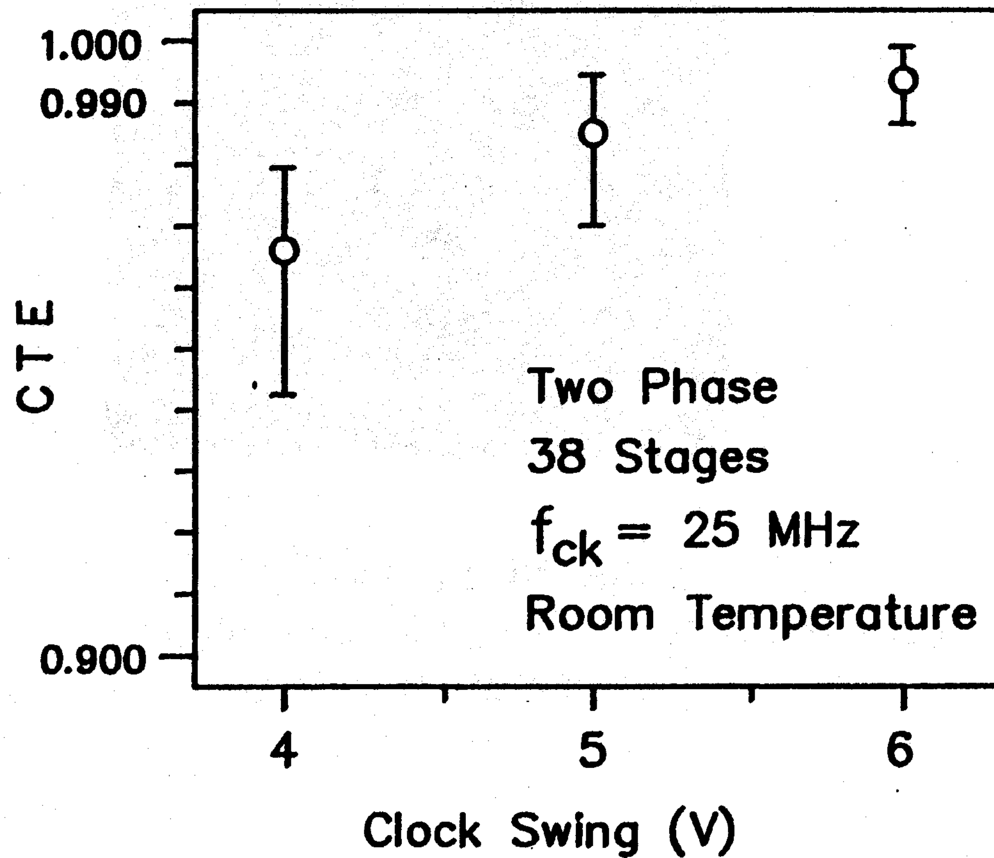
OPERATION OF 2DEG-CCDs

Room Temperature
2 Phase Clocking, 38 Stages (76 Transfers)
24 μm x 24 μm Pixel

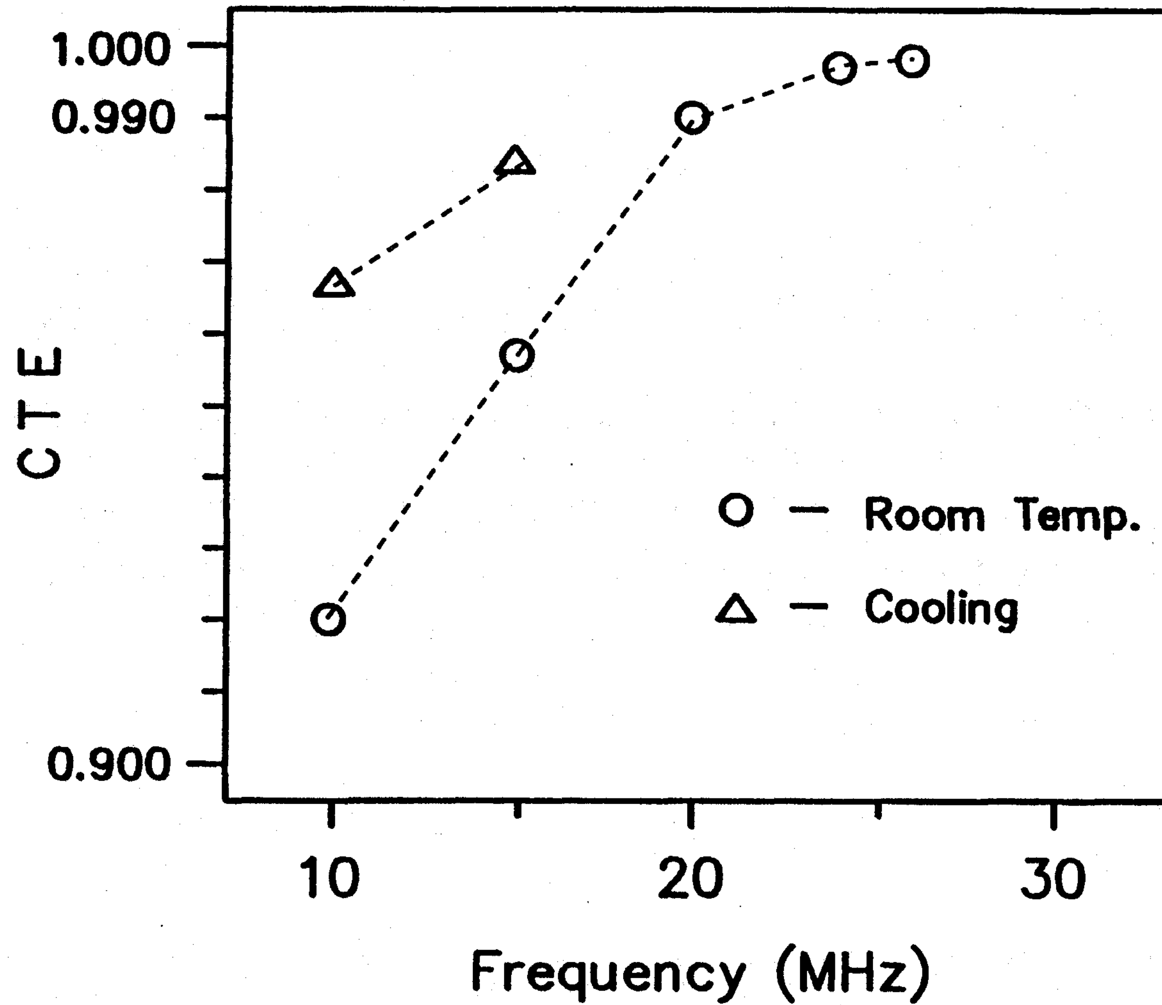


CTE = 0.9993 at 25 MHz

EFFECT OF CLOCK SWING



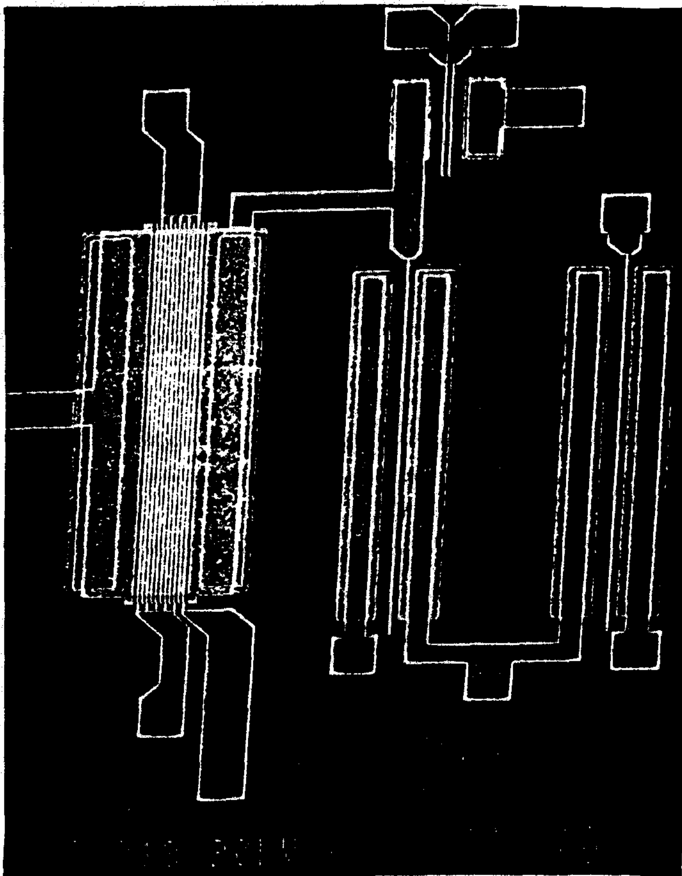
EFFECT OF OPERATING FREQUENCY

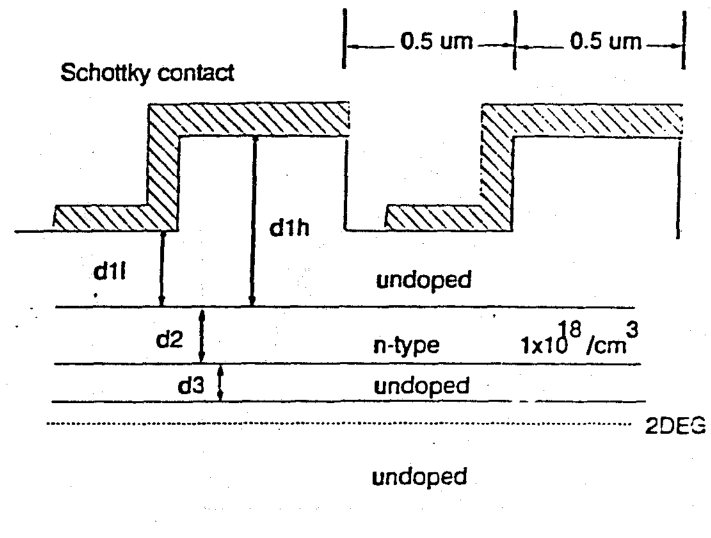


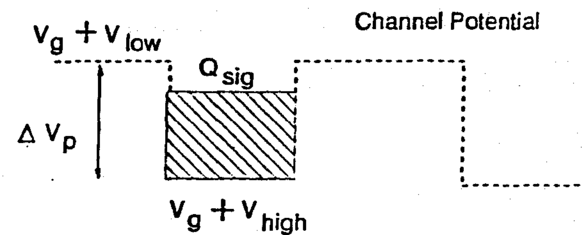
CRITIQUE OF TWO-PHASE 2DEG-CCD

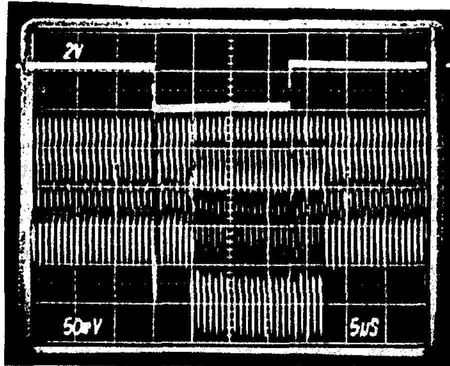
- Power dissipation savings during frame integration offset by higher clock swings during transfer
- Recess of 100 Å may be difficult to control over larger areas
- Recess-induced barrier voids natural anti-blooming in 2DEG-CCD
- Structure more difficult to achieve with planar doping

Colbeth, et al.
private communication (4/91)









fcl = 1.25MHz

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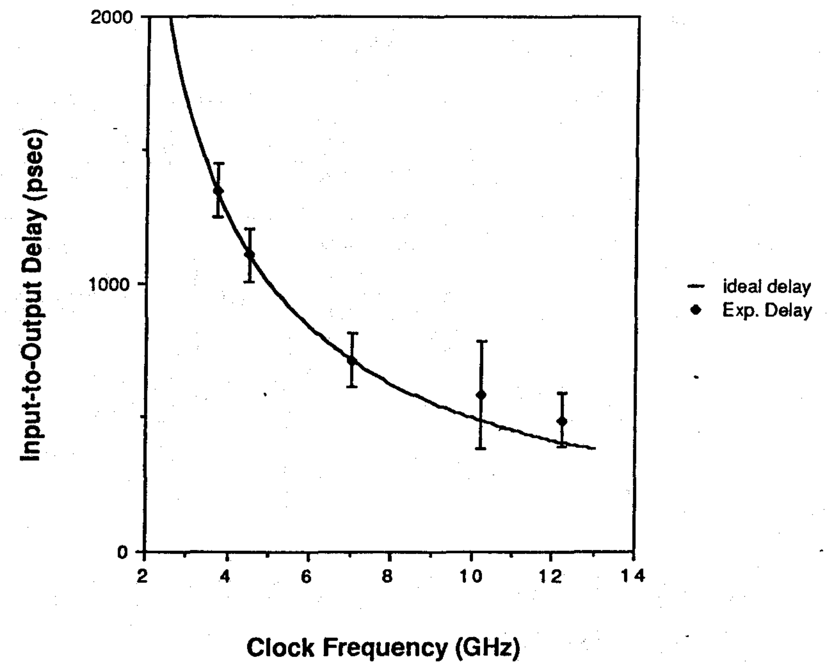
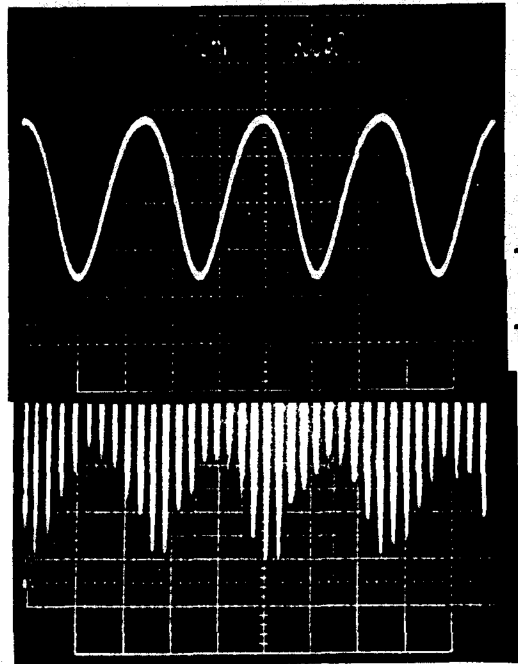
AlGaAs/GaAs 2DEG-CCD





fin = 750MHz
fcl = 7.0GHz

500ps/DIV

5 stage delay
2 gates/stage

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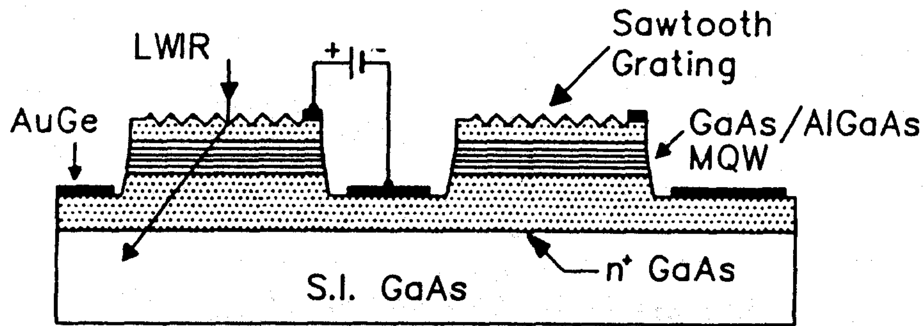
From J.-I. Song, 1990

Summary of advances in AlGaAs/GaAs 2DEG CCDs.

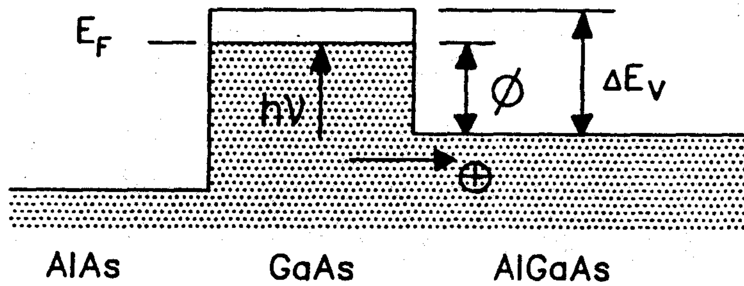
Year	Group	Channel Layer Material	Gate Structure	Gap Size	Gate Length x Width (um)	Clock Freq-uency	CTE	Comments
1982	Rockwell	AlGaAs /GaAs	Capacitive	2	40 x 400	< 83 KHz	0.98	300 K
1983	Rockwell	AlGaAs /GaAs	Capacitive	1	5 x ?	< 83 KHz	< 0.9	300 K
1990	Columbia	AlGaAs /GaAs	Resistive	N/A	5 x 100	13 MHz – 1 GHz	0.999	4-Phase, 300 K
1990	Columbia	AlGaAs /GaAs (δ–Doped)	Resistive	N/A	5 x 100	130 KHz – 1 GHz	>0.999	4-Phase, 300 K
1990	Columbia	AlGaAs /GaAs	Resistive	N/A	24 x 24	26 MHz	0.9993	2-Phase, 300 K
1991	Varian	AlGaAs /GaAs	Capacitive	<0.2	0.5 x 100	12 GHz	>0.99	2-Phase

STATUS OF 2DEG-CCDs

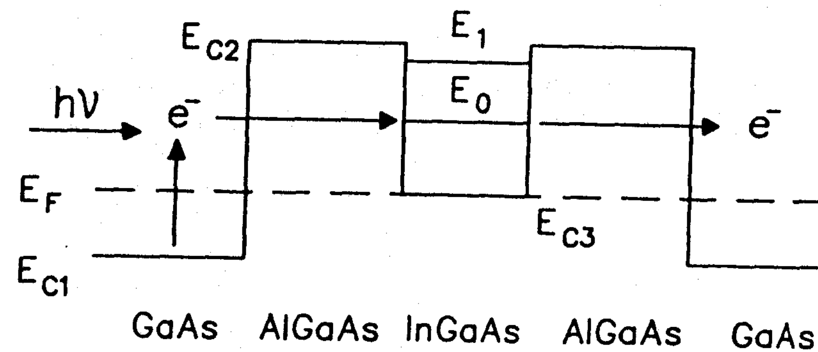
- Resistive-gate 2DEG-CCD demonstrated with CTE of 0.9997 from 100 KHz to 1 GHz at room temperature
- High frequency limit not yet explored, low frequency limit set by dark current
- Dark current mechanism understood and improved structure proposed
- Two-phase device structure demonstrated with CTE of 0.9993



a)

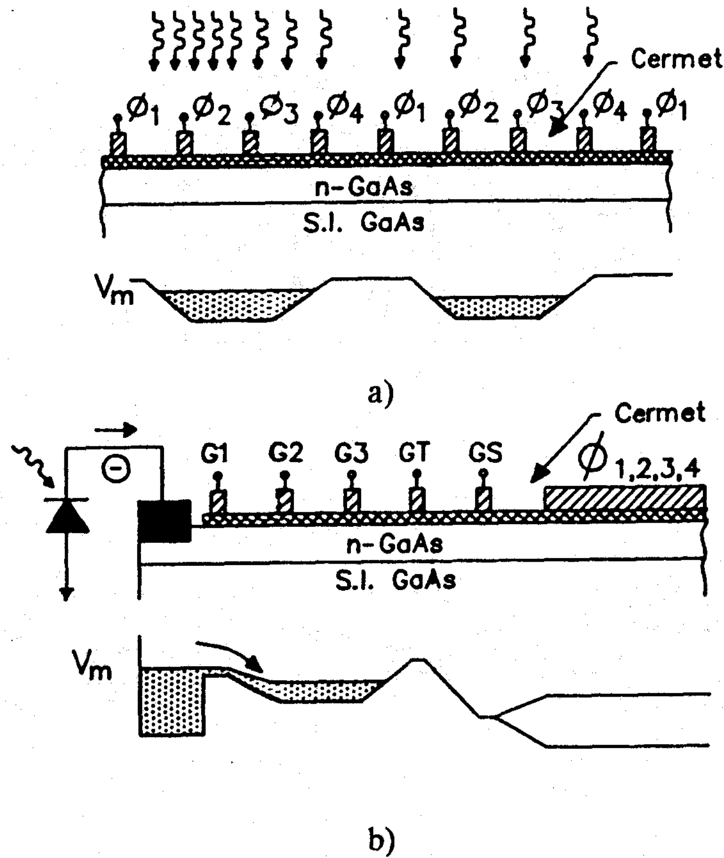


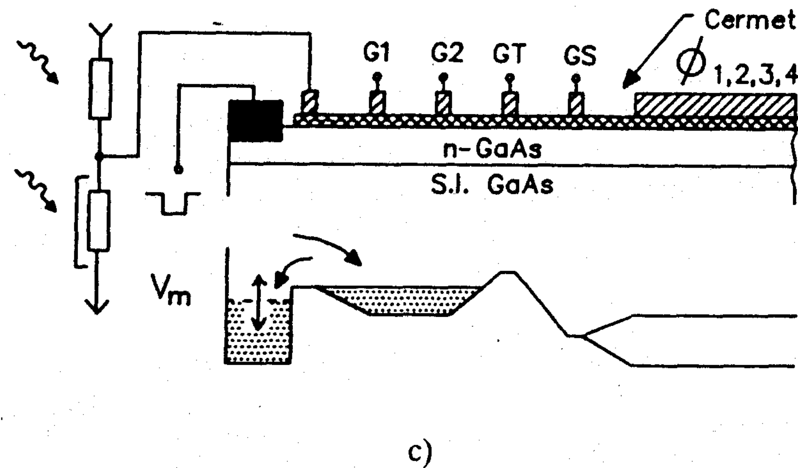
b)



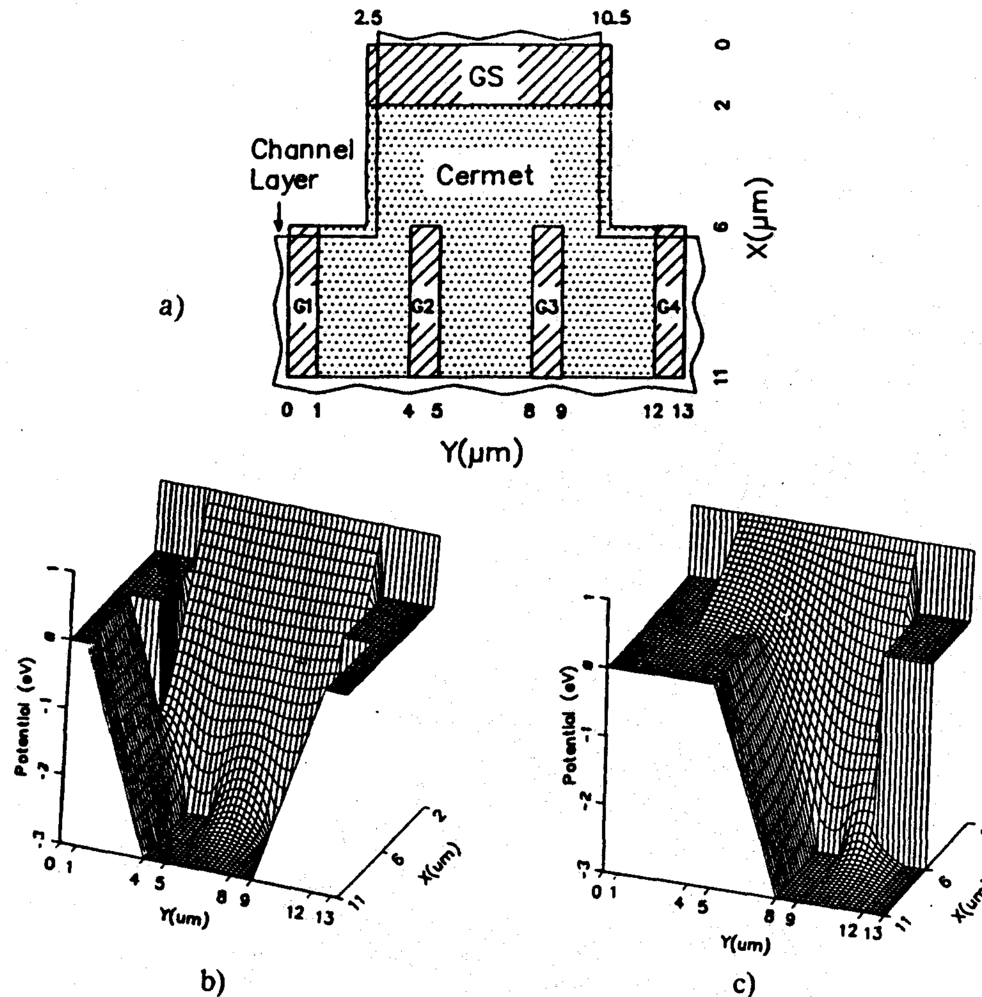
c)

a) Schematic cross section of a GaAs/AlGaAs multiquantum well photodetector. (Ref. 10.) b) Energy band diagram of a heterojunction internal photoemission detector. (Ref. 12.) c) Energy band diagram of a resonant tunneling photodetector. (Ref. 13.)





Schematic cross sections and channel potentials of GaAs RGCCD multiplexers. a) Direct detection method. b) Direct injection scheme (indirect detection). c) Gate modulation scheme (indirect detection).



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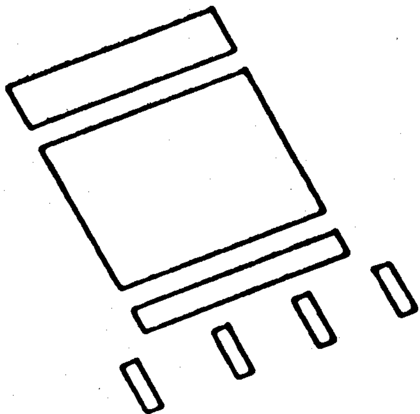
a) Schematic of a portion of the side-injection gate utilizing a resistive-gate structure for the computer simulation. b) Potential profile of the resistive layer with GS=-1V, G1=G4=0V, G2=G3=3V. c) Potential profile of the resistive layer with GS=-1V, G1=G2=0V, G3=G4=3V.


POTENTIAL(V)
Y(um)
0.0
8.0
16.0
24.0
32.0
X(um)
0.0
4.0
8.0
12.0
16.0

GaAs CCD Research Effort at the University of Cincinnati

Contributors: Dr. P.B. Kosel (P.I.), M.R. Wilson (Ph.D.), L.A. King (M.S.), H.D. Lee (M.S.), W.J. Roeckner (M.S.), E.M. Miller (M.S.), D.S. Katzer (Ph.D.), L.E. Bechtler (M.S.), N. Bozorgebrahimi (Ph.D.), R.E. Poore (Ph.D.)

Research Emphasis: Novel fabrication methods
Novel CCD architectures
Applications to imaging & signal processing

Accomplishments: 1. Fabrication

Rapid thermal annealing of ion-implanted GaAs CCDs - 1985

Anodization process for overlapping gate (OVG) CCDs - 1986

Tantalum masking for 2-phase meander channel CCDs - 1988

2. CCD architectures

4-phase OVG CCD delay line with 60 nm gate spacing - 1987

3-phase linear OVG CCD imager on GaAs - 1988

2-phase doubly implanted meander channel CCD - 1988

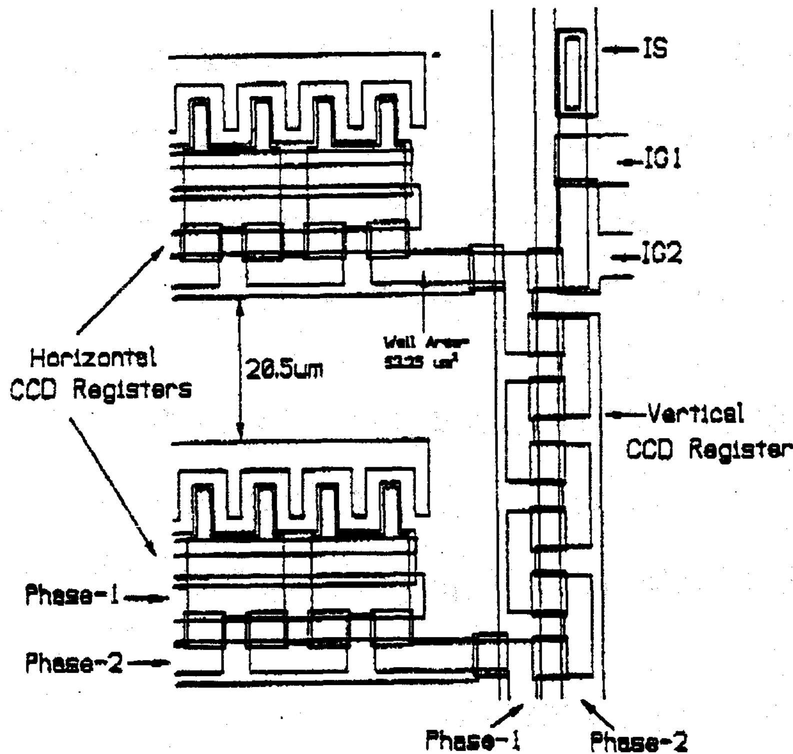
3. Applications

2-phase meander channel GaAs CCD imager with metal-semiconductor-metal (MSM) detectors - 1991

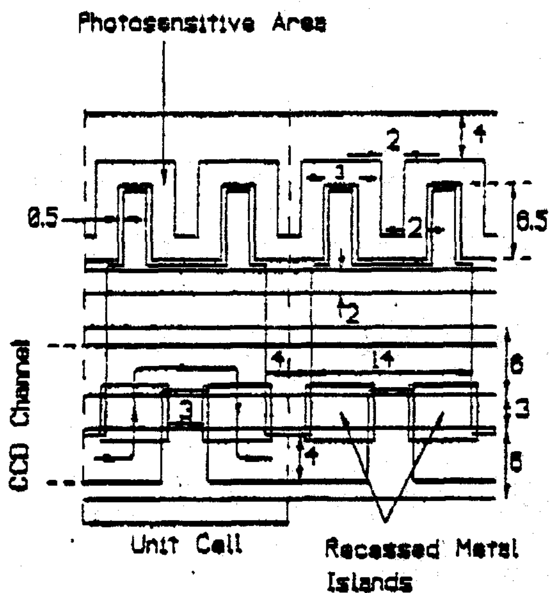
Current Effort

Two-phase meander channel CCD imager on GaAs with MSM photodetectors

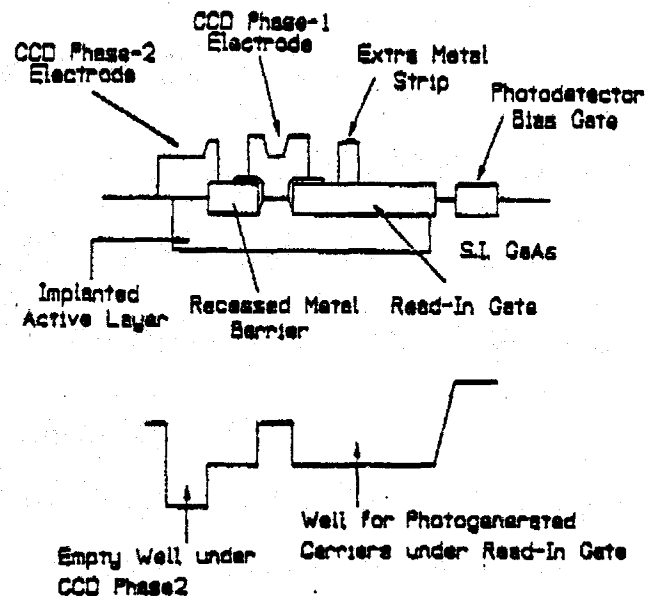
1. Layout features of row & column CCD registers:



2. Unit cell of CCD imager (dimensions in microns)



3. X-section and potential well profile for operation



COMMENTS ON MONOLITHIC INTEGRATION OF 2DEG-CCD AND QWIP (AS OF TODAY)

- Dark current of QWIP at 65 K approximate

  10^5 times that of 2DEG-CCD
- QWIP device can tolerate approximately 1 volt swing during integration so direct injection OK
- Vertical integration possible for high fill-factor
- Broad-band imaging (10 μm) requires readout at 10 KHz frame rate given 2DEG-CCD capacity due to QWIP dark current (10 x photo current)

JPL

Jet Propulsion Laboratory
California Institute of Technology

Summary

- Highest CTE is 0.9999 at 1GHz using capacitive-gate CCDs (Columbia).
- Highest Speed is 12GHz using 2DEG-CCD with 2-phase capacitive-gate (Varian).
- Most complex chip was transversal filter using resistive-gate (Rockwell).
- Lowest power, high performance CCD seems to be resistive-gate 2DEG-CCD.
- IR CCD multiplexer best-choice seems to be resistive-gate 2DEG-CCD.
- Low speed performance limited by dark current from gate to channel.

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