PHOTODIODE SENSOR ARRAYS

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ABSTRACT. A discussion of photodiode sensor arrays which includes the basic photodiode sensor, photodiode address and scan circuits, on-chip MOS electrometer amplifiers, off-chip analog signal processing, and image performance of photodiode arrays. The signal-to-noise (S/N) ratio is formulated at the photodiode sensor for Nyquist, shot, and equivalent first-stage current noises. CMOS and varactor-boot strapped PMOS scan registers are presented and their associated address and reset MOS switches. Examples of photodiode sensor arrays are line arrays, or matrix area arrays, and special-purpose arrays such as circular configuration.

1. SPECTRAL RESPONSE

The spectral response of a photodiode approaches an ideal photon detector in the 400 nm to 800 nm wavelength band[1] as illustrated in figure 1. A photodiode with a deep diffusion, 12 μm $P^+/P^-/N$ junction, has improved response in the infrared because the long-wavelength photogenerated carriers are collected with improved efficiency; however, there is some sacrifice in the short-wavelength or blue response. Conversely, a shallow diffusion, 2 μm P^+/N junction has improved response in the blue since the short-wavelength carriers near the silicon surface are collected more efficiently than with the deeper diffused diode structure. The deep diffusion has several disadvantages: (1) a restriction on the achievable pitch of the array due to lateral diffusion and (2) increased noise due to the additional sidewall capacitance of the diffusion. The short-wavelength fall-off in

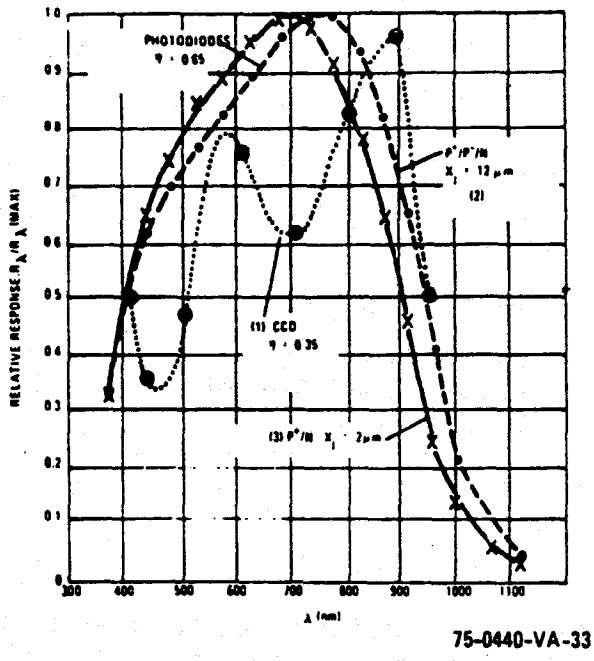

Figure 1. Photodiode Relative Spectral Response vs Wavelength[1]

spectral response ($\lambda < 400$ nm) is a result of surface recombination of photogenerated carriers while the long-wavelength fall-off ($\lambda > 800$ nm) up to the band-gap limitation is due to bulk recombination of photogenerated carriers. Typically, a shallow-diffused photodiode with a 2 μm SiO_2 protective overcoat layer has a quantum efficiency $\eta \simeq 0.70$ in the 400 nm to 800 nm wavelength band. The advantage of diffused photodiodes over other sensors is the lack of spectral streaking from element-to-element (i.e., spectral response variations versus wavelength) which is important for multispectral scanning.

1.1 Responsivity

The responsivity concept has been discussed in the chapter "Design of Solid-State Imaging Arrays" and a particular example was taken for an effective irradiance in the 400 nm to 800 nm wavelength band referenced to a 6000°K blackbody temperature. For the photodiode of figure 1, the responsivity becomes

$$R_D = A \frac{\int_{400}^{800} R_\lambda H_\lambda d\lambda}{\int_{400}^{800} H_\lambda d\lambda} = \frac{0.212fC}{\mu J/m^2}\left[\frac{A}{1\ mil^2}\right]\left[\frac{\eta}{0.70}\right] = \frac{1325e^-}{(\mu J/m^2)}\left[\frac{A}{1\ mil^2}\right]\left[\frac{\eta}{0.70}\right] \quad (1)$$

for an effective quantum efficiency η and area A. The signal charge collected on a photodiode operating in the charge-storage integration mode[2] in an exposure time τ is

$$Q_S = R_D H(eff.)\tau = R_D E(eff.) \quad (2)$$

where H(eff.) is the denominator in equation (1). The maximum signal charge $Q_s(sat.)$ is related to the reset voltage V_R across the photodiode and the photodiode storage capacitance C,

$$Q_S(sat.) = V_R C \equiv R_D E_{sat.}(eff.) \quad (3)$$

which defines a saturation exposure density. Thus, to handle large exposure densities we need a sizeable capacitance C; however, we shall see this limits the minimum detectable signal by the kTC noise.

The signal in general will consist of a leakage current component I_L which accumulates over the exposure time to provide a "signal" charge

$$Q_S' = R_D E(eff.) + I_L\tau = (I_{ph} + I_L)\tau \quad (4)$$

where $I_{ph} = R_D E(eff.)$ is the photocurrent collected. In general, the leakage current is typically less than 0.1 pA for a 1 mil^2 area (i.e., < 15 nA/cm^2 leakage current). The leakage or dark current is a strong function of temperature and it may be written as,[3]

$$I_L = qn_i\left(\frac{A_B W_j}{\tau_{g-r}} + A_S s\right) \quad (5)$$

where n_i is the intrinsic carrier density $n_i \sim \exp(-E_G/2kT)$ with a value n_i (300°K) = 1.45×10^{10} cm^{-3}. A_B and A_S are the areas associated with the bulk and surface components of leakage, W_j the width of the space charge region, s the surface recombination

velocity and τ_{g-r} the bulk generation recombination lifetime with typical values of $s < 10$ cm/sec and $\tau_{g-r} > 100$ μsec. Special gettering techniques with phosphorous[3] for bulk gettering and hydrogen for surface-state annealing have yielded $s < 1$ cm/sec and $\tau_{g-r} > 1$ msec. In practice, the leakage current is sufficiently low such that small variations in temperature [e.g. $\Delta T \simeq 0.1°C$] do not affect the low light level performance of the photodiode arrays; however, anomalous leakage current spots in the array with extreme temperature sensitivity affect array performance through "streaking" [e.g. "white" lines in the hard copy image] which is highly objectionable to the observer. These anomalous "streakers" [note: streakers usually prefer to remain anomalous] have been attributed to metal-ion precipitates of the silicon surface which give rise to generation recombination centers with unusually high emission rates as a function of temperature. Rapid "quenching" of silicon photodiode arrays from high temperatures "freezes" these centers in the bulk and prevents precipitation at the surface.

2. NOISE EQUIVALENT SIGNAL (N.E.S.)

The noise equivalent signal (N.E.S.) is defined as the input exposure density E(eff.) which will make the signal-to-noise (S/N) = 1 at a specified position in the signal flow path. A conventional reference point is the storage node of the photodiode, although other points may be selected with the same end result for N.E.S. Before we formulate the N.E.S. the various noise sources must be examined in the photodiode array.

2.1 Johnson-Nyquist Noise[4] (kTC)

An electronic switch or a conductor has a finite resistance to the flow of charge carriers. This electrical resistance defines the fluctuation of charge across a capacitor C. To illustrate this effect we consider a series RC circuit as shown in figure 2 with an ideal switch on a resistance with associated noise voltage generator v(t). The differential equation which describes the charge across the capacitor may be written as,

$$\frac{dQ}{dt} + \frac{Q}{RC} = \frac{v(t)}{R} \tag{6}$$

which can be integrated to yield,

$$Q(t) = \frac{1}{R} e^{-t/RC} \int_0^t v(\tau) e^{\tau/RC} \, d\tau \tag{7}$$

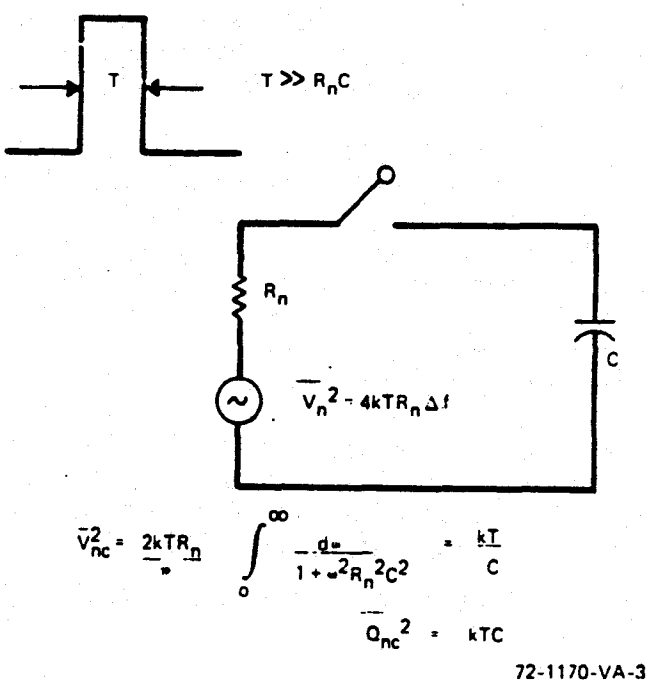

Figure 2. Johnson-Nyquist Thermal Noise

The fluctuation in Q(t) may be obtained as follows:

$$\overline{q_n^2} = \overline{\Delta Q(t)^2} = \left[Q(t) - \overline{Q(t)}\right]^2 \tag{8}$$

$$= \frac{1}{R^2} e^{-2t/RC} \int_0^t \int_0^\tau \langle v(\tau_1)v(\tau_2)\rangle e^{(\tau_1+\tau_2)/RC}\, d\tau_1 d\tau_2$$

For the "white" noise Johnson-Nyquist power spectra the thermal fluctuations of charge carriers in the resistor give

$$\langle v(\tau_1)v(\tau_2)\rangle = 2kTR\,\delta\langle(\tau_1 - \tau_2)\rangle \tag{9}$$

Substitution of equation (9) into (8) yields

$$\begin{aligned}\overline{q_n^2} &= kTC\,(1-e^{-2t/RC}) \\ &= kTC \text{ for } t \gg 1/2\ RC \\ &= 2kTt/R \text{ for } t \ll 1/2\ RC\end{aligned} \tag{10}$$

Examination of equation (10) reveals the noise charge fluctuations approach zero as $t \ll RC$. [The above results are analogous to the theory of Brownion Motion for which the particle displacement $\overline{x_n^2} \sim \overline{q_n^2}$ and the diffusion coefficient $D = kT/R$.] In general, the address or reset time intervals (i.e., the time the switch is closed) are sufficiently long such that $t \gg 1/2RC$. For two independent switch closures and measurements the total charge uncertainty is obtained by addition of the fluctuations,

$$\overline{q_n^2}\ \begin{matrix}(2\ \text{independent} \\ \text{measurements})\end{matrix} = 2kTC \tag{11}$$

We should note the probability density for the Johnson-Nyquist noise has a Gaussian distribution. An intuitive derivation of equation (10) may be obtained if we note the fluctuation energy by the equipartition theorem is $kT/2$ which we can equate to $\overline{q_n^2}/C$ the electrostatic energy of a capacitor.

2.2 "Shot" Noise ($e\bar{I}\tau$)

The fluctuation in the intensity of a charge carrier stream as it flows from one point to another is the so-called "shot" effect. The fluctuation in this stream is random, similar to the thermal fluctuations of the Nyquist noise; however, the probability density has a Poisson distribution. The spectral noise current density may be written as,

$$\overline{i_n^2} = 2e\bar{I}\,\Delta f \tag{12}$$

where $\bar{I}$ is the average current flow. We will apply the "shot" effect to the collection of photo and thermally generated charge carriers in a reverse-biased photodiode. If the photodiode is reverse-biased for an exposure time τ, then the Fourier transform of equation (12) multiplied by a square wave transform yields,

$$\overline{q_n^2} = \int_0^\infty \left(\frac{i_n^2}{\Delta f}\right)\tau^2\left(\frac{\sin \pi f\tau}{\pi f\tau}\right)^2 df = e\bar{I}\tau \tag{13}$$

with the exposure time interval acting as a filter for the "white" noise spectrum of the "shot" process. The average current $\bar{I} = I_{ph} + I_L$ as used in equation (4) may be substituted into equation (13)

$$\overline{q_n^2} = \underset{\text{photon}}{eR_D E(\text{eff.})} + \underset{\text{leakage}}{eI_L\tau} \tag{14}$$

2.3 Equivalent Noise Current in the Preamplifier

We may write a general expression for the equivalent noise current in the preamplifier due to surface or "1/f" noise in the MOS electrometer, if one is used in conjunction with the photodiode, or any equivalent noise source which may be placed at the input of the preamplifier. This noise current spectral density may be transformed to the photodiode storage node by the expression,

$$\overline{q_n^2} = \left(\frac{C}{g_m}\right)^2 \int_0^\infty \frac{\overline{i_n^2}}{\Delta f} |T(f)|^2 \, df \tag{15}$$

where C is the storage node capacitance, g_m the transconductance of the MOS electrometer, and T(f) the transfer function of the analog signal processor. Equation (15) may be written in a slightly different form as,

$$\overline{q_n^2} = \left(\frac{\overline{i_{no}^2}}{\Delta f}\right) B_{eff} \left(\frac{C}{g_m}\right)^2 \tag{16}$$

where $\overline{i_{no}^2}/\Delta f$ is determined at a characteristic corner frequency of the noise spectrum. The effective bandwidth is,

$$B_{eff} = \frac{1}{2\pi} \int_0^\infty \frac{\overline{i_n^2}/\Delta f}{\overline{i_{no}^2}\Delta f} |T(\omega)|^2 \, d\omega \tag{17}$$

If we consider a special case with a "white" noise spectral density and the transfer function of equation (31) in the chapter "Design of Solid-State Imaging Arrays," then the effective bandwidth becomes,

$$B_{eff} = \frac{2}{\pi} \int_0^\infty \frac{\sin^2 \frac{\omega \tau_o}{2}}{1 + \omega^2/\omega_o^2} \, d\omega = \frac{\omega_o}{2} \left(1 - e^{-\omega_o \tau_o}\right) \tag{18}$$

where ω_o is the bandwidth of the preamplifier and τ_o is the time difference between clamping to the reset reference and the sample determination. If we use equation (12) as the noise current spectral density, then the noise charge becomes,

$$\overline{q_n^2} = e\bar{I}_A \omega_o \left(1 - e^{-\omega_o \tau}\right) \left(\frac{C}{g_m}\right)^2 \tag{19}$$

where $\bar{I}_A$ is the average current flow into the amplifier. If we consider thermal noise in the form of surface or "1/f" noise in the electrometer amplifier, then the noise charge may be written in the form $\overline{q_n^2} = kTC_{ST}$, where C_{ST} is an effective storage trap capacitance. Notice equation (13) and the example expressed by equation (19) illustrate the basic feature of the electrometer, namely, a low C/g_m ratio is desired to minimize off-chip noise contribution to the N.E.S.

2.4 Formulation of Noise Equivalent Signal (N.E.S.)

If we consider the various noise contributions of sections (2.1, 2.2, 2.3) and the signal charge described by equation (2), then the noise equivalent signal (N.E.S.) becomes,

$$N.E.S. = \frac{1}{R_D}\left[\beta kTC + e\bar{I}_L\tau + \left(\frac{\overline{i_{no}^2}}{\Delta f}\right) B_{eff}\left(\frac{C}{g_m}\right)^2\right]^{\frac{1}{2}} \qquad (20)$$

Johnson Nyquist — Shot — Preamplifier Noise Current

where $\beta = 1$ or 2 dependent upon a single or double address switch closure and $\overline{i_{no}^2}/\Delta f$ is determined at the input of the off-chip preamplifier. Alternately, equation (20) may be written with $\overline{v_{no}^2} = \overline{i_{no}^2}/g_m^2$ to reference the noise current to the input of the on-chip electrometer. In the case where surface or "1/f" noise is present in the electrometer we have,

$$\frac{\overline{i_{no}^2}/g_m^2}{\Delta f} = 4kTR(\omega) \sim \frac{N_{ST}}{\omega C_A} \qquad (21)$$

where N_{ST} is the surface trap density and C_A is the area of the electrometer gate region.[5,6] The total storage capacitance $C = C_p + C_A$, where C_p is the parasitic capacitance of interconnect or line capacitance and photodiode capacitance. If we combine equations (20) and (21), then the N.E.S. may be minimized with respect to the gate area of the electrometer amplifier.

Figure 3 illustrates the measured N.E.S. ($\mu J/m^2$) of a photodiode sensor chip[7] as a function of input exposure density E ($\mu J/m^2$). This particular chip has an N.E.S. limited by the Johnson-Nyquist noise of the storage capacitance C = 0.75 pF and the reflected current noise in the electrometer due to the high C/g_m ratio [g_m = 130 μmhos at V_R = 8V]. The photodiode sensor has an area of 18 μm x 22 μm as discussed in the chapter "Design of Solid-State Imaging Arrays" Section 4, and with an effective quantum efficiency of η= 0.70 the responsivity is 0.13fC/$\mu J/m^2$.

If we consider only the Johnson-Nyquist noise, then the calculated N.E.S. becomes

$$\text{N.E.S.}\left(\begin{matrix}\text{J-N noise}\\ \text{limited}\end{matrix}\right) \simeq \frac{\sqrt{2kTC}}{R} = 0.60 \quad \frac{\mu J}{m^2} \tag{22}$$

which is close to the measured values at low exposure densities. The radiation "shot" noise contribution does not disturb the N.E.S. until the exposure density is on the order of the above noise,

$$E\ (\text{radiation shot}) \simeq R\ \frac{(\text{N.E.S.})^2}{q} = \frac{2kTC}{qR} \simeq 300\ \frac{\mu J}{m^2} \tag{23}$$

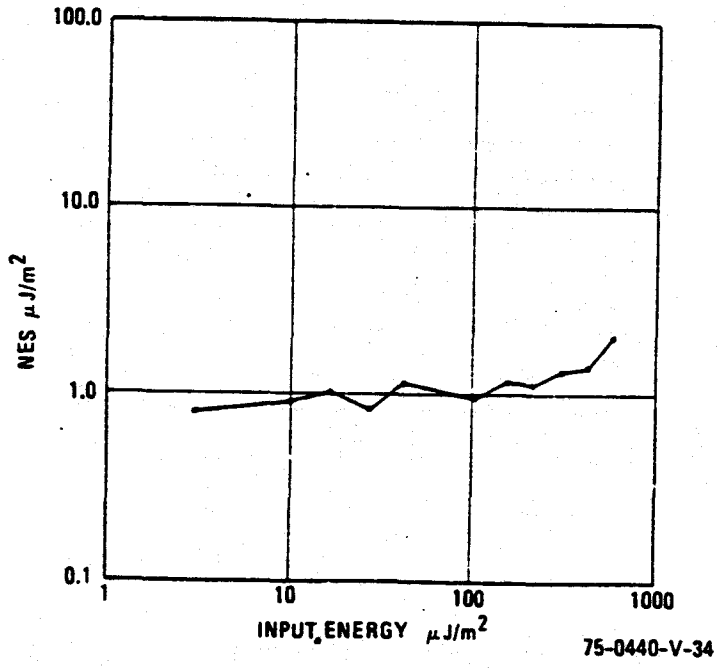

Figure 3. Noise Equivalent Signal (N.E.S.) as a Function of Exposure Density E ($\mu J/m^2$) [After reference (7)]

which is illustrated in figure 3. Figure 3 was taken with an exposure time of τ = 1 msec and referenced to a 6000°K blackbody in the 400 nm to 800 nm wavelength band.

3. CMOS SCAN REGISTERS AND ADDRESS CIRCUITRY

Complementary MOS-FET (CMOS) shift registers may be used to scan or commutate photodiode sensors with the advantages of low voltage operation and low power dissipation. The photodiodes operate in the charge storage integration mode in which the photodiode is periodically reversed-biased and reset to a known reference voltage V_R. Figure 4 illustrates a CMOS shift-register composite circuit to control the amplifier address and reset switches. A "one" is input to the first stage of the shift register (SR1) and shifted through successive stages with a 2ϕ register clock (ϕ_A,ϕ_B). The "one" appears at interstage points as gate pulses to the amplifier address switches. In this example the shift register output addresses a pair of photodiodes with a corresponding pair of output busses (i.e., OUT-A, OUT-B). The CMOS shift register is of the dynamic type with the clocks 180 degrees out of phase from each other. The nested reset pulse is generated by an AND gate whose inputs are the external clock ϕ_C and the SR output at the particular stage of interest.

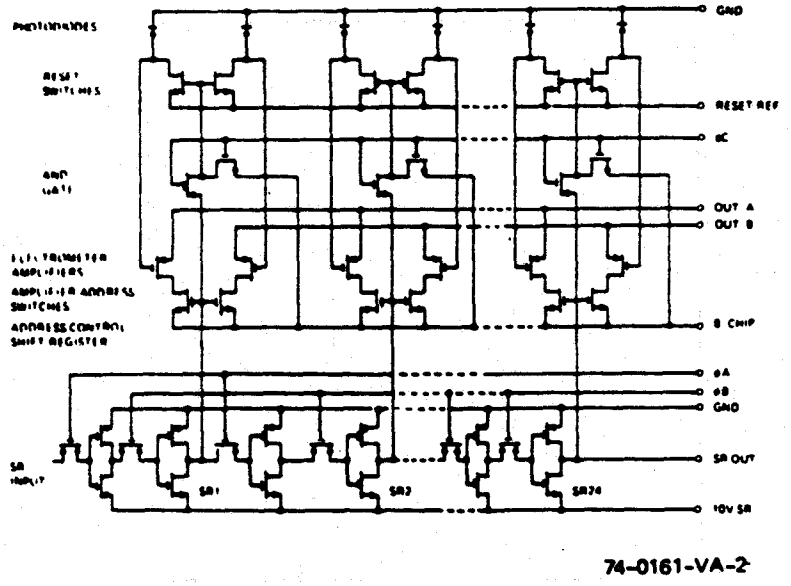

Figure 4. CMOS Shift Register Composite Circuit [After reference (7,8)]

Figure 5 illustrates the photodiode sensor and amplifier combination, which is an enlargement from figure 4. Q_1 is the reset switch, Q_2 the electrometer amplifier, and Q_3 the address switch controlled by the SR output. In this particular linear array each photodiode has an associated p-channel electrometer amplifier. Figure 6 illustrates the sensor timing and signal output waveforms. The output waveform may be divided into three distinct time periods:

(1) READ SIGNAL of n^{th} integration time

(2) RESET photodiode for $n+1^{th}$ integration time

(3) READ initial condition of $n+1^{th}$ integration time and subtract from step (1)

The "READ SIGNAL" voltage is a function of the initial conditions (voltage) in the nth integration time, leakage (I_L) and signal (I_S) current, and electrometer amplifier gain (g_m). The output voltage e_o may be related to the charge Q_G on the gate of the electrometer by

$$e_o = \frac{R_f g_m Q_G}{C} = \frac{R_f g_m}{C} (I_L + I_S)\tau \qquad (24)$$

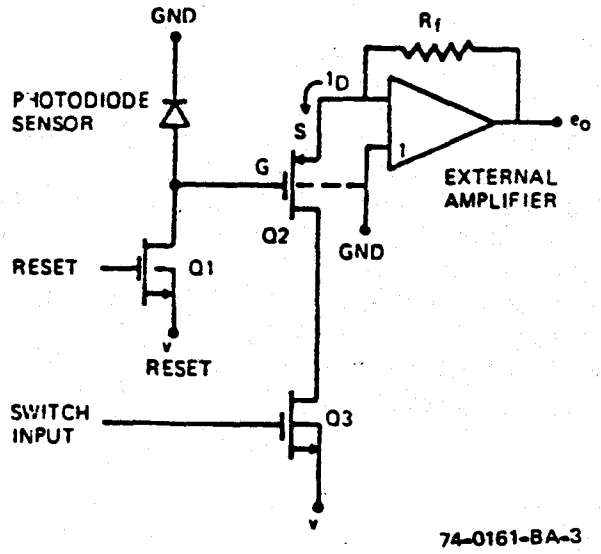

Figure 5. Equivalent Circuit of Photodiode Sensor and Amplifier [After reference (7,8)]

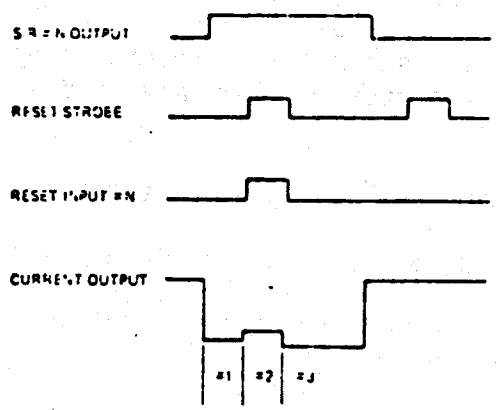

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Figure 6. Sensor Timing and Output [After reference (7,8)]

where C is the capacitance from the gate electrode of Q_2 to ground and τ the integration time. The transconductance g_m of the electrometer is related to the physical properties of the structure by the expression,[3]

$$g_m = \frac{\bar{\mu}_p}{X_o} \left(\frac{W}{L}\right) K_o \epsilon_o (V_{GS} - V_T) \qquad (25)$$

where $\bar{\mu}_p$ is the hole mobility, X_o the oxide thickness, $K_o\epsilon_o$ the dielectric constant of the oxide, (W/L) the width-to-length ratio, V_{GS} the gate-to-source voltage, and V_T the device threshold voltage. In the reset interval (#2) the electrometer output is a measure of the reset voltage level (i.e., $V_{GS} = V_R$). In the (#3) interval the electrometer output is a measure of the initial condition for the start of the integration or exposure time. The initial condition interval (#3) differs from the reset interval (#2) by the addition of feedthrough signal voltage

$$\Delta V = \frac{C_{GD}}{C_{GD}+C} V_R \qquad (26)$$

where C_{GD} is the gate-to-drain feedthrough capacitance of the reset switch Q_1. The difference between (#3) and (#1) intervals is a measure of the accumulated signal and leakage currents over the exposure interval as expressed by equation (24).

4. PMOS SCAN REGISTERS AND ADDRESS CIRCUITRY

P-channel MOS-FET (PMOS) shift registers, which use the so-called "bootstrapping" or varactor principle,[9] may be employed to scan photodiode sensors with the advantage of extremely low power dissipation. Figure 7 illustrates a varactor PMOS shift register with the storage node "bootstrapped" by the varactor. This particular shift register AND's the clock pulse and the data pulse to provide a scan pulse to actuate the address switch and transfer the stored photocharge from the addressed photodiode to the bus line B_1. Figure 8 illustrates the clock waveforms, data, and address pulses provided by the scan register. The address pulses are provided for each 1/2 stage of the shift register and the shift register only dissipates power in the stage with the data. Thus, the entire shift register has a power dissipation equivalent to a single stage under continuous operation. Figure 7 with a common bus line for many photodiodes is an example of a single amplifier per row of photodiodes in contrast with the single amplifier per photodiode of figure 4.

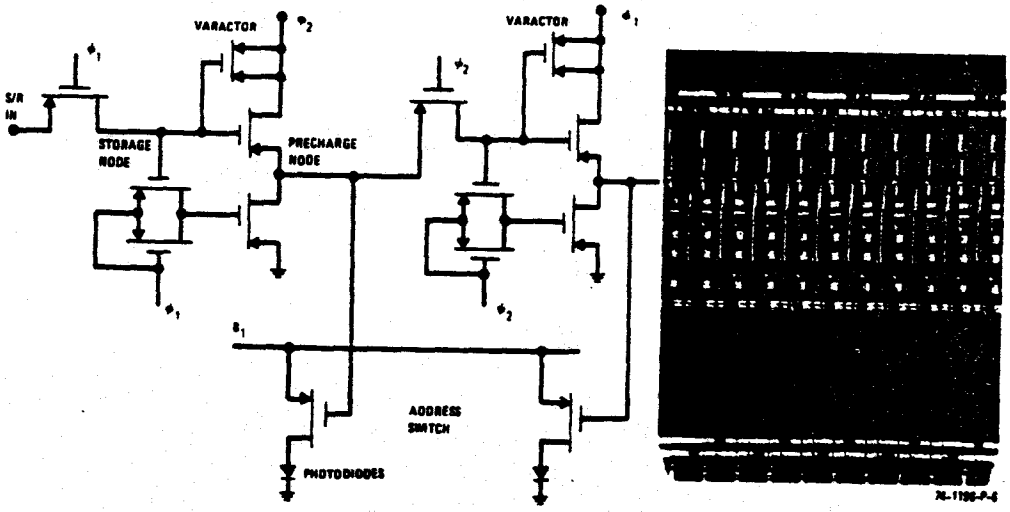


Figure 7. PMOS Shift Register Composite Circuit with Varactor Bootstrapping of Storage Node

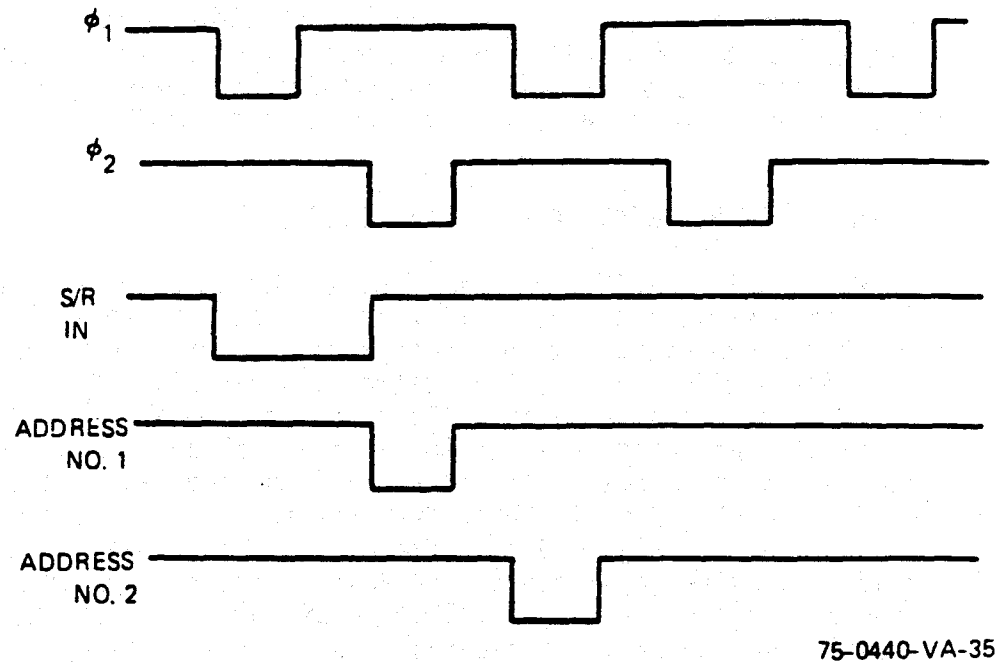


Figure 8. Clock and Address Waveforms for Circuit of Figure 7

The varactor principle used in figure 7 may be explained with reference to figure 9. The voltage "bootstrapped" to the storage node by the varactor may be written as

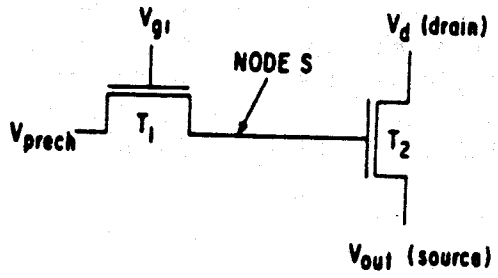
$$\Delta V = \frac{C_b}{C_b+C_S} V_c$$

where C_b is the varactor capacitance of figure 9. C_S the total storage node capacitance, and V_c the clock voltage. The capacitance C_b has two values:

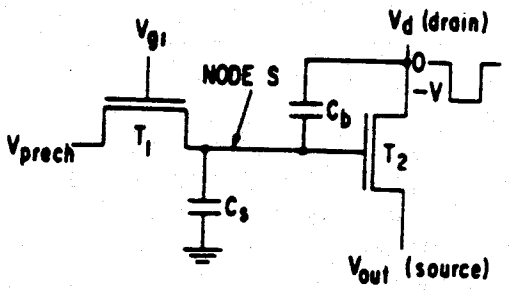
$$C_b = C_o WL' \qquad \text{DATA} = 0$$

$$= C_o WL \qquad \text{DATA} = -V_c$$

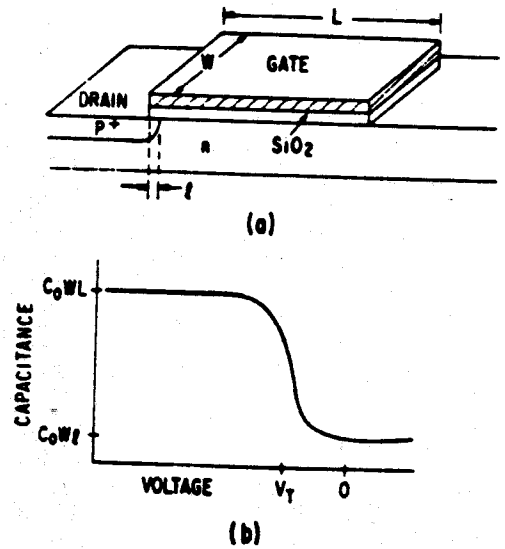
where $L \gg L'$. When the storage node = $-V_c$ the inversion layer under the varactor causes the capacitance C_b to become high effectively coupling a large fraction of the clock voltage V_c to the data node where it adds to the data. Thus, the clocks (ϕ_1,ϕ_2) are coupled "full-strength" (i.e., no threshold-voltage loss) to the address switch resulting in high speed operation.



Storage node S in dynamic MOS circuit



Circuit incorporating bootstrap capacitor C_b



(a) Schematic of MOS varactor. (b) Capacitance as function of voltage for MOS varactor.

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Figure 9. MOS Varactor Principle [After reference (9)]

Another example of a varactor PMOS shift register type is shown in figure 10 where the precharge node is "bootstrapped" with the varactor.[10] This shift register provides a different output scan waveform in which DATA and $\overline{\text{DATA}}$ are used to switch the sensor from one voltage (V_R) to another (V_W) and provide a latching feature. Figure 11 illustrates the characteristic waveforms of data (address No. 1) and data (address No. 2). The usefulness of this circuit lies in the validity of the DATA and $\overline{\text{DATA}}$ in the absence of the clock in contrast with figure 8. Thus, a knife-edge scan may be provided with the circuit of figure 10.

5. PHOTODIODE LINE ARRAYS

Photodiode line arrays have the general equivalent circuit shown in figure 12 with a series address switch controlled by a shift register as discussed in sections 3 and 4. The video output may be common to a row of photodiodes as discussed in section 4, or each photodiode may have its own electrometer amplifier and amplifier address switch. The video output shown in figure 12 may be connected to an on-chip electrometer amplifier and reset switch or this function may be performed off-chip as shown in figure 13. The disadvantage of the method shown in figure 13(b) is the inability to remove the reset noise across the capacitance C, while the method shown in figure 13(a) limits the noise to the

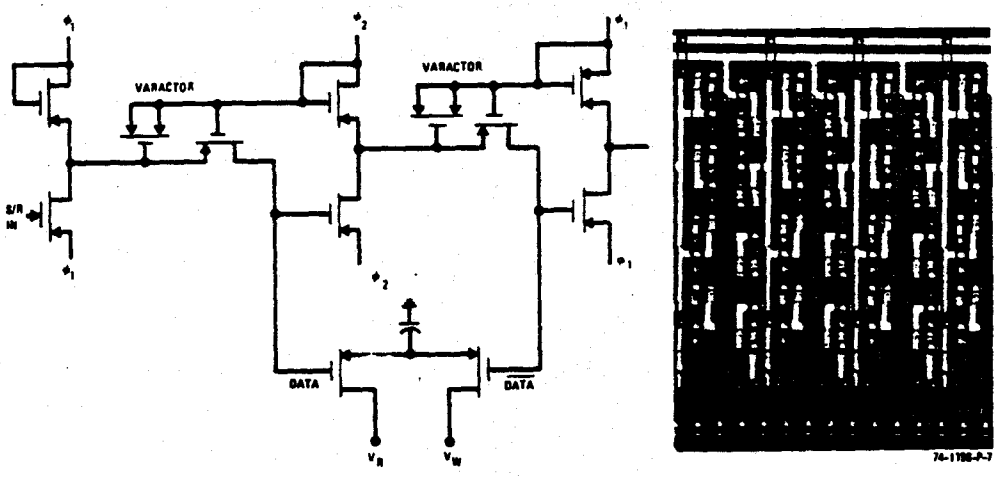

Figure 10. PMOS Shift Register Composite Circuit with Varactor Bootstrapping of Precharge Node

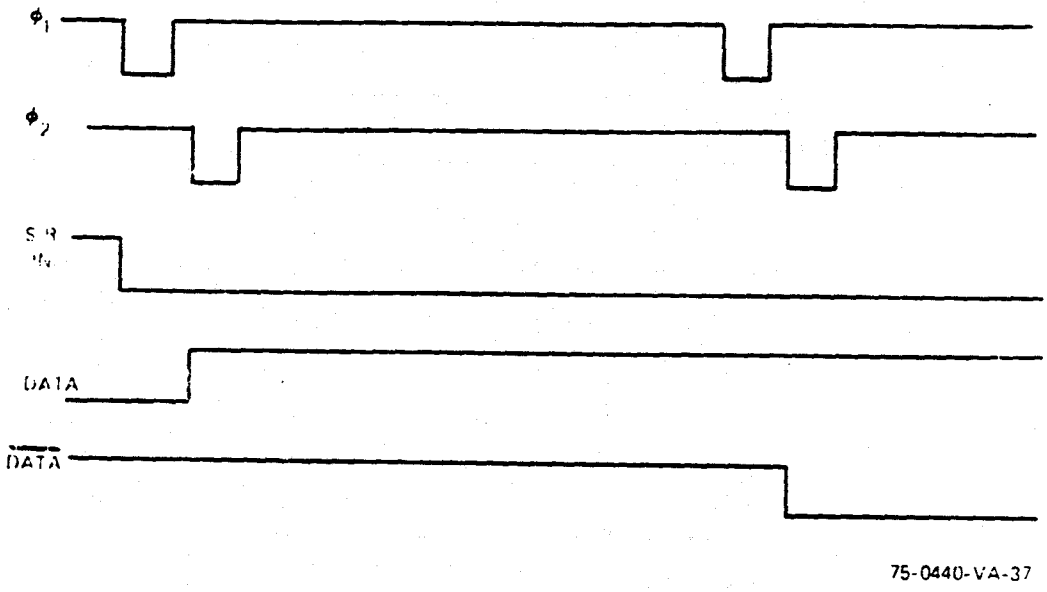

Figure 11. Clock and Address Waveforms for Circuit of Figure 10

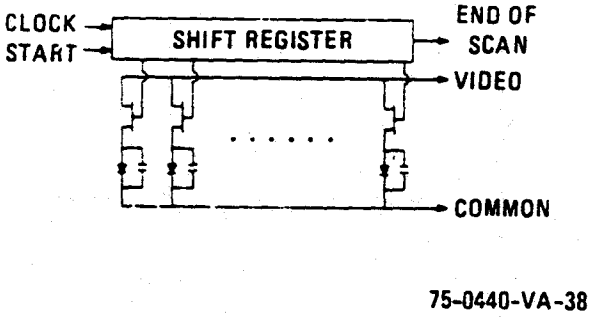

Figure 12. Schematic Diagram of Typical Photodiode Line Scanner

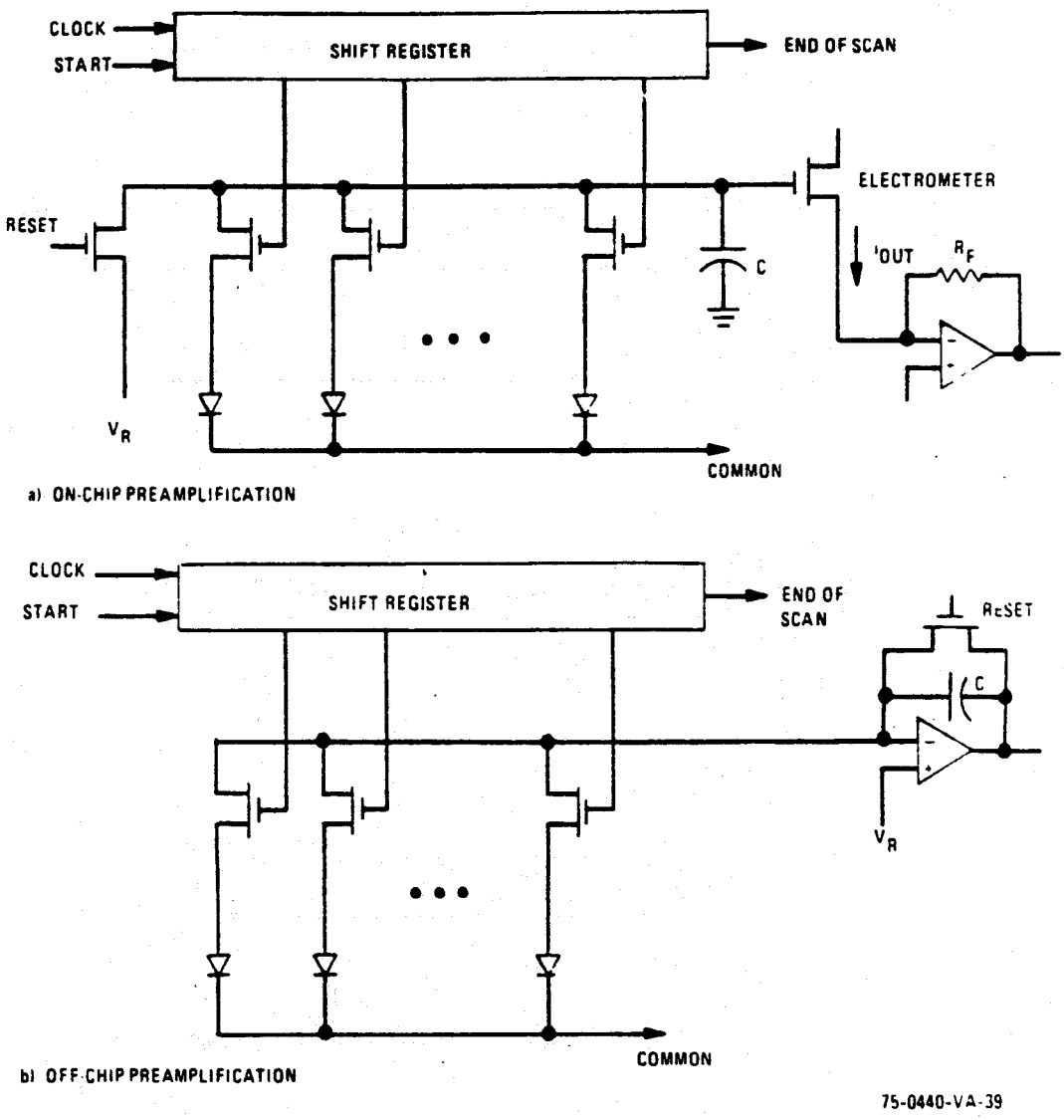

Figure 13. Methods of Preamplification for Photodiode Line Arrays Sharing a Common Preamplifier

diode capacitance C_D, since $C_D \ll C$. A disadvantage of the method shown in figure 13(a) is the need to provide $C \gg C_D$ and hence off-chip noise contributions reflect back to the gate of the electrometer with C/g_m as discussed in section 2.3. Figure 14 illustrates a 256-element photodiode array on 1 mil centers with a 1 mil wide aperture and figure 15 illustrates a 1872-element photodiode array on 15 μm centers (pitch P = 15 μm) with a 16 μm aperture. (See section 4.2 in the chapter entitled "Design of Solid-State Imaging Arrays.) The background in figures 14 and 15 illustrate the light shield and the aperture window of the array.

Figures 14 and 15 are examples of zero-P design; however, to improve the figure-of-merit of the photodiode line array and achieve equal M.T.F.'s at the Nyquist sampling limit [see section 4.1 of the chapter "Design of Solid-State Imaging Arrays"], a bilinear photodiode array may be selected. Figure 16 illustrates such a photodiode array with a 2-P offset in the along-track direction where P = 0.6 mil in the across-track direction. In order to form long line arrays the "butted" assembly technique shown in figure 17 is employed in which the edge of the chip must be placed to within 0.3 mil of the end diodes to maintain image contiquity. Figure 18 illustrates a butted assembly, linear

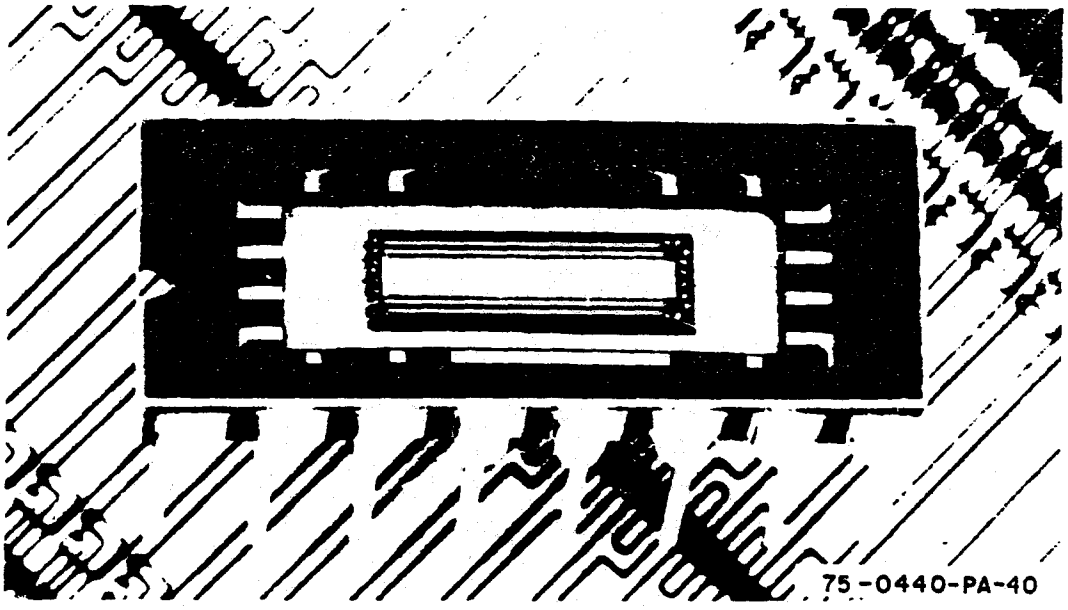

Figure 14. RL-256 Element Photodiode Line Array with Pitch P=1 mil and Aperture Width 1 mil (i.e., $\Delta x = \Delta y =$ P=1 mil) [Courtesy of Gene Weckler, Reticon Corp.]

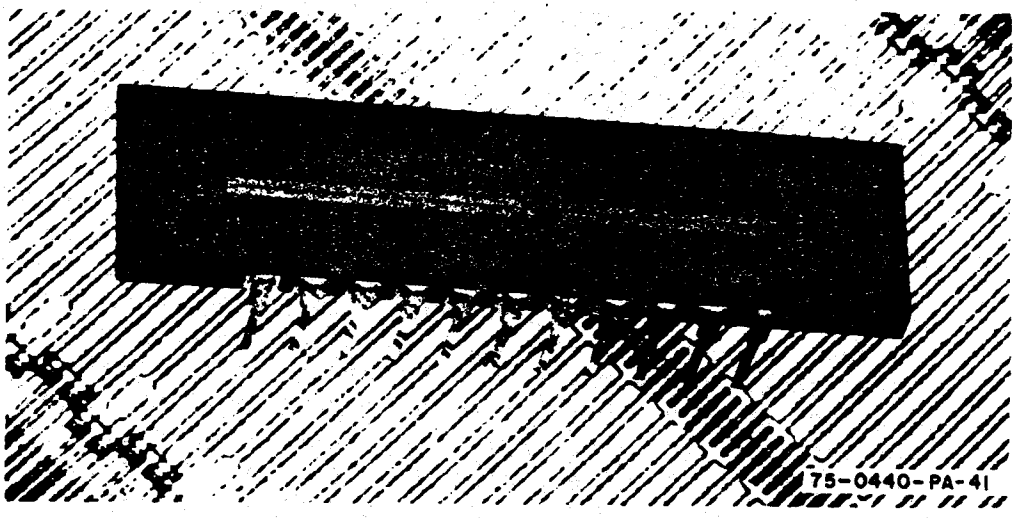

Figure 15. RL-1872 Element Photodiode Line Array with Pitch P=15 μm and Aperture 16 μm (i.e., Δx = P = 15 μm, Δy = 16 μm) [Courtesy of Gene Weckler, Reticon Corp.]

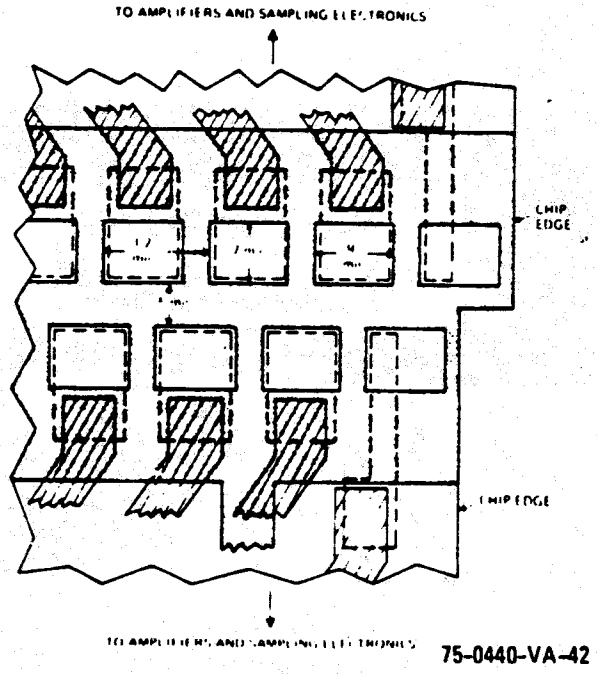

Figure 16. Photodiode Bilinear 2P Array and Chip Edge Geometry [After reference (7)]

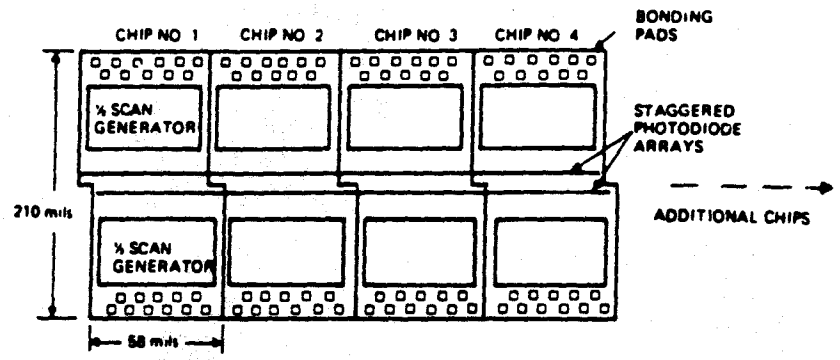

Figure 17. Butted Assembly of Chips with Staggered Photodiode Arrays [After Reference (7)]

array of 1728 photodiodes and associated signal processing for Advanced Earth Resource Observation Applications for NASA/Goddard Space Flight Center.[8,11] Figure 19 is an example of high resolution aerial imaging with such photodiode line arrays. Photodiode line arrays may be used for page reading, film scanning, satellite "push-broom" remote sensing, pattern recognition, spectroscopy, etc.

6. PHOTODIODE AREA ARRAYS

Figure 20 illustrates a schematic diagram of a photodiode matrix array with horizontal and vertical PMOS shift registers to perform the X-Y selection of the photodiode sensor. Each unit cell consists of MOS-FET which serves to "AND" the horizontal and vertical shift register outputs for address of the photodiode sensor. Figure 21 illustrates a 50 x 50 matrix photodiode array with diodes on 4 mil centers in X and Y directions. Figure 22 illustrates a self-scanned array (SSA) of 12 x 38 photodiodes in an Optical Character Recognition (OCR) Wand System for 2-dimensional character imaging. The OCR Wand is passed over the data, either left-to-right or right-to-left, and the characters are

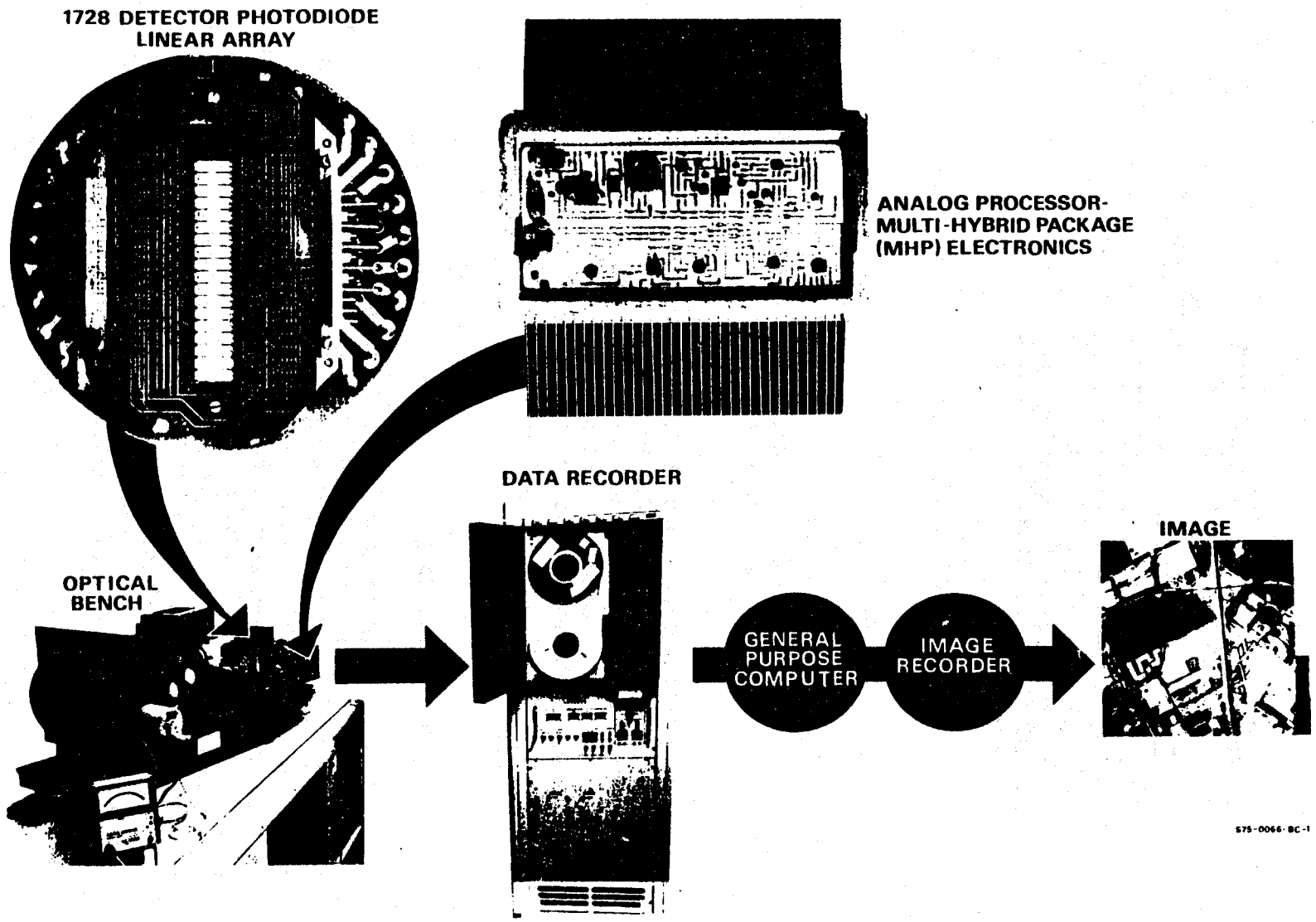

Figure 18. Breadboard Linear Photodiode Array [Reference (11)]

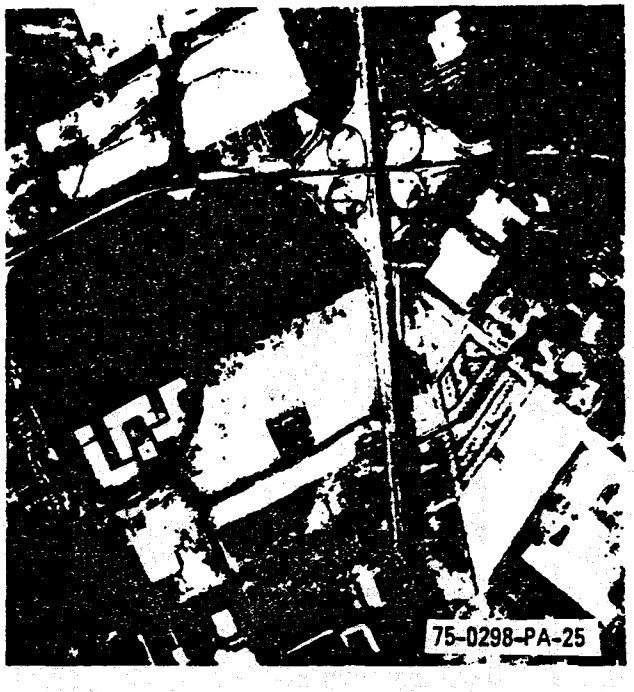

Figure 19. High Resolution Aerial Imaging with Photodiode Line Arrays (reference 8) [Clover Leaf Expressway Inter-Change] Taken with a Scene Translator

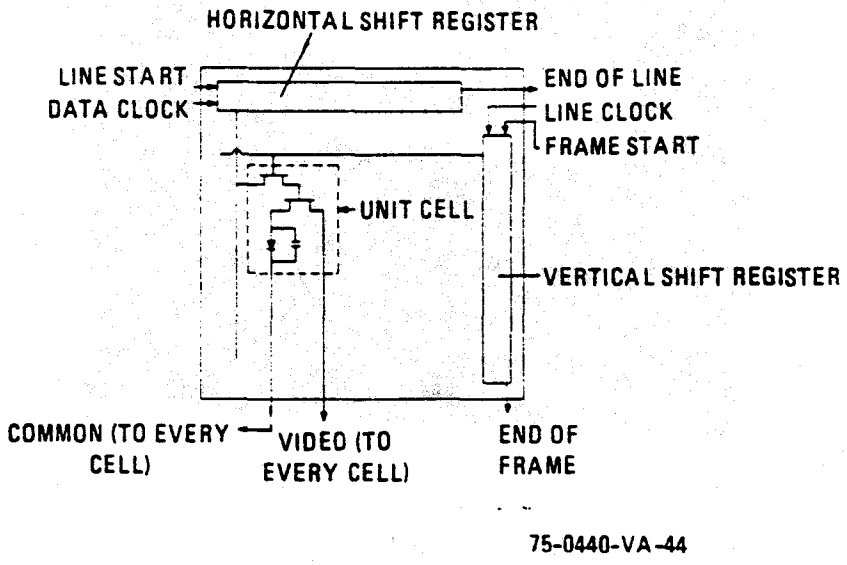

Figure 20. Schematic Diagram of Photodiode Matrix Array (Courtesy of Gene Weckler, Reticon Corp.)

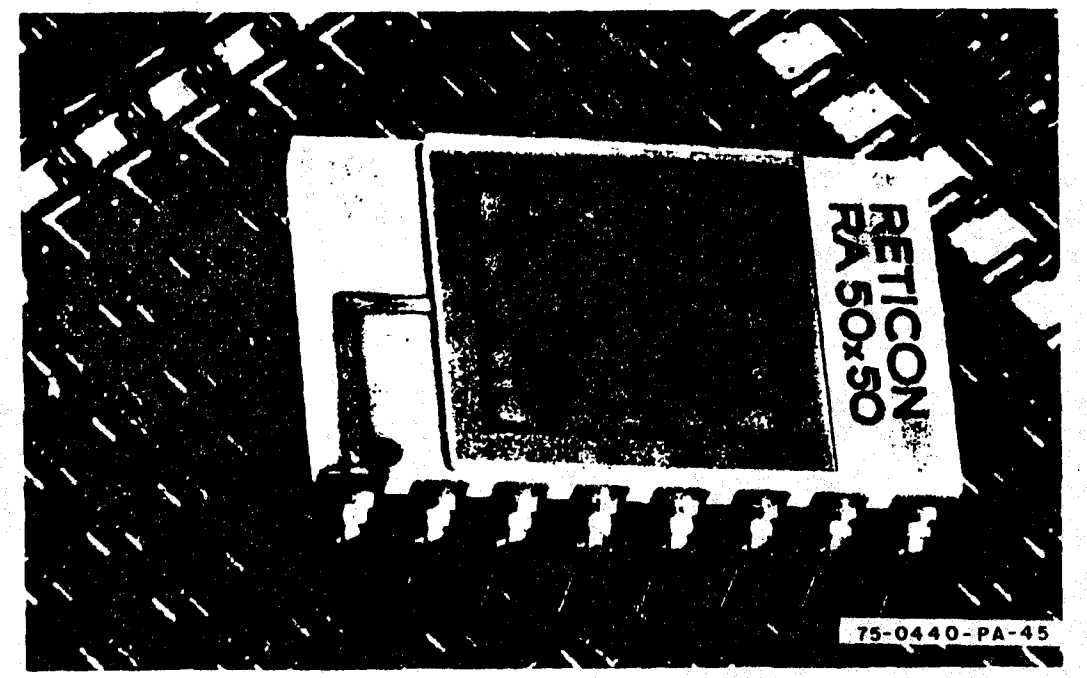

Figure 21. RA 50 x 50 Matrix Photodiode Array
(Courtesy of Gene Weckler, Reticon Corp.)

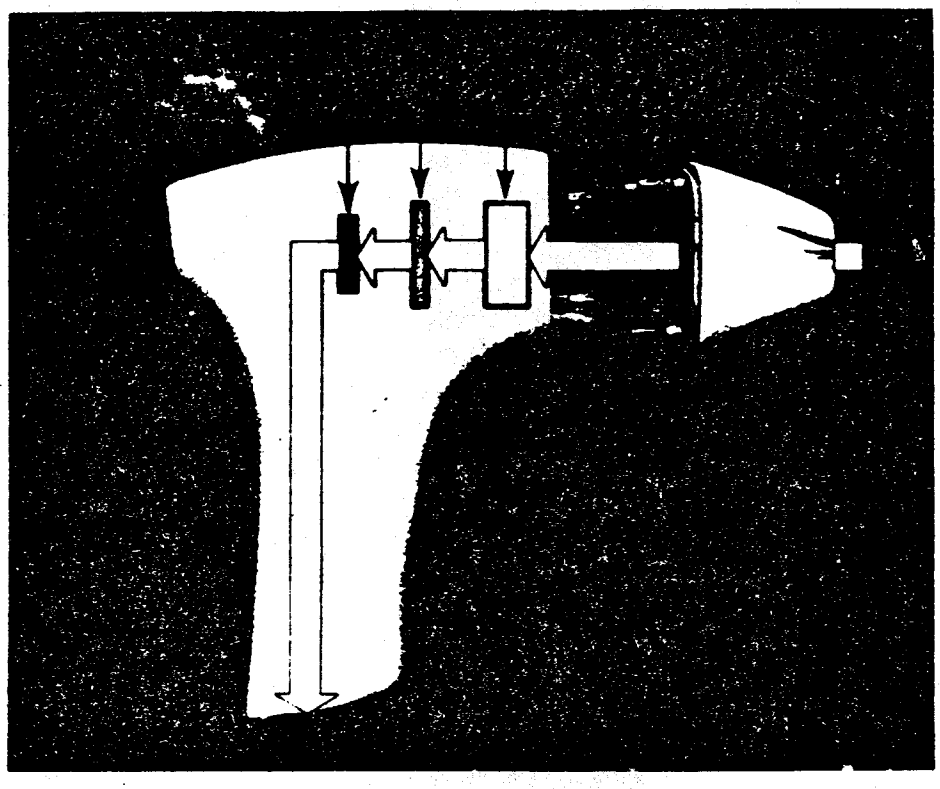

Figure 22. Hand-Held (OCR) Wand 12 x 38 Photodiode Self-Scanned Array (SSA) for Character Recognition (Courtesy of Dick Van Tyne, Recognition Equipment, Inc.)

recognized, edited and transmitted to a data recording system. Decentralized data collection can be performed for point of sale, inventory recording, production control, postal data, airline tickets, etc. Figure 23 illustrates a set of numerics made from a C.R.T. screen with the video processed from the matrix array to modulate the Z-axis of the C.R.T.

Figures 22 and 23 illustrate the use of low resolution photodiode matrix arrays for pattern recognition.

7. SPECIAL PURPOSE PHOTODIODE ARRAYS

Figure 24 illustrates a circular 64-element photodiode array for such applications as tracking, alignment, automatic focusing, etc. The 64 photodiodes are equally spaced on a 2-mm diameter circle with a 0.1 mm x 0.1 mm element size as shown in figure 25. The light sensing area is an annulus with an outer radius of 1.05 mm and an inner radius of 0.95 mm. The elements are scanned by a PMOS shift register/ring counter with a two-phase clock drive as shown in figure 26. The time required to scan a complete circle is $64/f_c$, where f_c is the clock frequency.

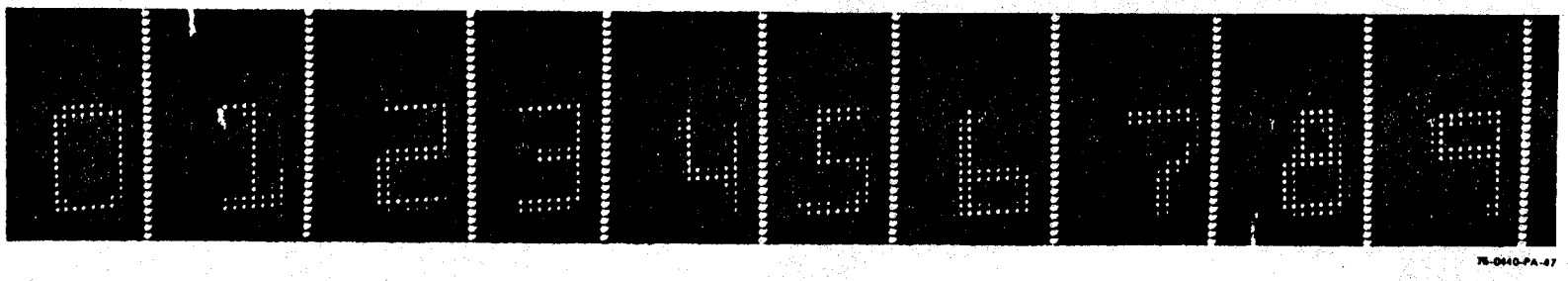

Figure 23. Numeric Characters Imaged on a 12 x 38 Photodiode Matrix Array (Courtesy of Dick Van Tyne, Recognition Equipment, Inc.)

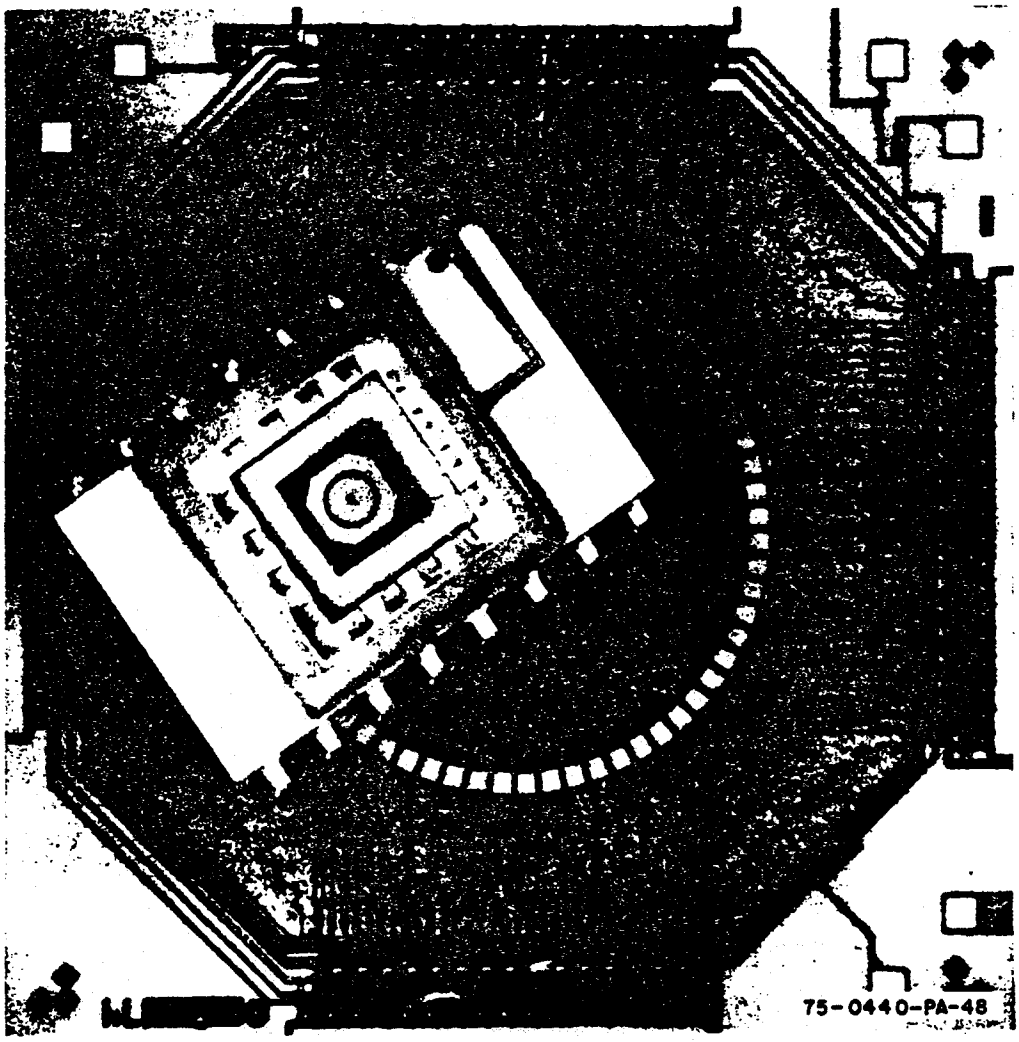

Figure 24. RO-64 Self-Scanned Circular Photodiode Array
(Courtesy of Gene Weckler, Reticon Corp.)

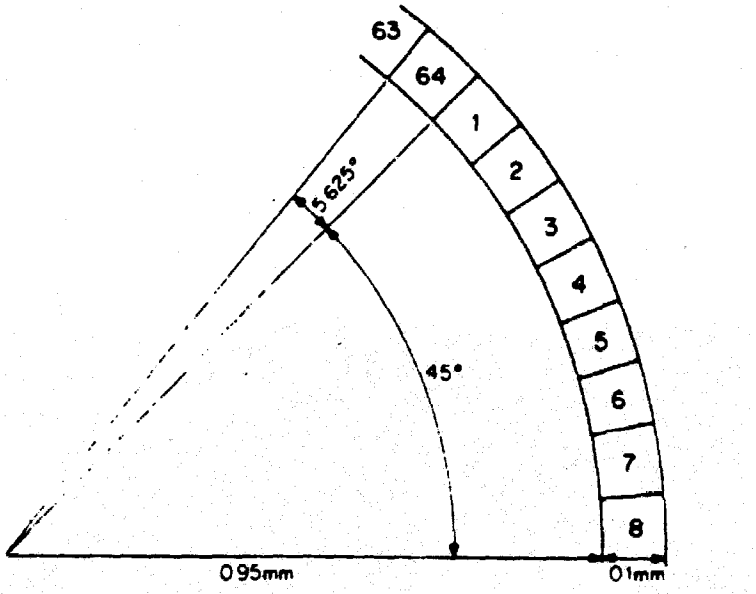

Figure 25. Circular Photodiode Geometry

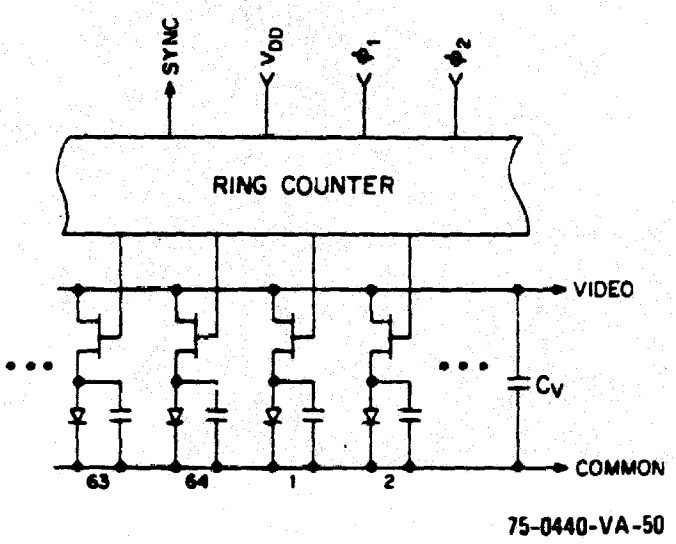

Figure 26. Ring Counter Driven Circular Array

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