1990 IEEE Workshop
on
Advanced Solid-State Imagers

May 18-20, 1990

Columbia University's Arden House

Harriman, New York

USA

Foreword

This workshop is aimed at drawing together engineers and scientists active in solid-state imager research and advanced development. The workshop is to provide a focus for in-depth discussion of present limitations, recent advances, and future directions for imagers. Despite the relatively small size of the imager R&AD community, opportunities for substantial discussion of common issues between persons pursuing different materials and wavelength regimes are too infrequent. It is the intent of this workshop to promote cross-fertilization of concepts and ideas between sub-disciplines, and to allow us to expand our indiviudal horizons beyond our present scope of activities.

To this end, a series of 20 invited talks spanning a spectrum of imaging activities has been planned to seed discussion. In addition, a contributed short presentation session with a poster reception has been included. The location of the workshop, Columbia University's Arden House, was chosen to foster an informal atmosphere. This former mansion of the Harriman family is located 45 miles north on New York City on a wooded mountain top overlooking Harriman State Park and is a self-contained conference center. Arden House was reserved exclusively for this weekend workshop.

This workshop was made possible by the sponsorship of the IEEE Electron Device Society, and is hosted by the NSF Center for Telecommunications Research at Columbia University. On behalf of my co-chairman, Prof. Walter F. Kosonocky of NJIT, and myself, I would like to thank the speakers and participants for what promises to be a most interesting forum.

Eric R. Fossum
Workshop Organizer

Department of Electrical Engineering
Columbia University
New York, New York 10027

May 18, 1990

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Lester Kozlowski, Rockwell International Science Center

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1990 IEEE WORKSHOP ON ADVANCED SOLID-STATE IMAGERS

May 18-20, 1990
Harriman, New York

AGENDA

Friday, May 18, 1990

3:00-5:30 pm — Arrival and check-in
5:30-6:30 pm — Reception. East room.
6:30-7:30 pm — Dinner served. Dining room.
8:30-9:30 pm

Welcome
Eric Fossum, Columbia University
General remarks
Walter Kosonocky, NJIT
Future trends in solid-state imagers
Gene Weckler, EG&G

9:30-11:30 pm — Bar is open. East Room.

Saturday, May 19, 1990

7:30- 8:30 am — Breakfast is served. Dining room.
9:00-10:30 pm

Outstanding issues in imagers
Bruce Burkey and Tom Lee, Kodak Research Laboratories
The 4096x4096 CCD imager sensor
Dick Bredthauer, Ford Aerospace
CCD imagers for HDTV
Albert Theuwissen, Philips Research Laboratories

10:30-11:00 am — Coffee break
11:00-12:30 pm

CCD imagers for HDTV application
Hirosi Tanigawa, NEC Microelectronics Research Labs
The use of two-dimensional electrical model with current flow to design a CCD vertical anti-blooming pixel
Dan McGrath, Polaroid Corporation
New radiation problems in CCDs
Bruce Woodgate, NASA Goddard Space Flight Center

12:30-1:30 pm — Lunch is served. Dining room.
2:00-3:30 pm

CCD and MOSFET randomly accessed imagers sensors: smart scanners
Savaas Chamberlain, DALSA Inc.
Present and future roles of high performance charge transfer devices detectors in spectrochemical analysis
Bonner Denton, University of Arizona
Micropattern detectors in particle physics
Erik Heijne, CERN EF-Division

3:30-5:00 pm — Open discussion and recreation.
5:00-5:30 pm — SHORT PRESENTATIONS

Shallow buried-channel CCDs with built-in drift field
Analisa Lattes and S. Munroe, MIT/Lincoln Labs
5-V Uniphase CMOS/CCD process for mixed-signal processing
S. Munroe, Analisa Lattes, D. Whitley and D. Arsenault, MIT/Lincoln Labs

Transient simulation of millimeter-wave CCDs
Rick Colbeth, Varian
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Frank Deluccia, Aerospace Corporation
2DEG CCDs for advanced III-V detectors
Jong-In Song, Columbia University
2D meander channel CCD scanner imager on GaAs with photoconductive detectors
Pete Kosel, N. Bozorgebrahimi, L. Bechtler, R. Poore, Univ. Cincinnati
Noise and charge trapping in CCDs
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Some large format CCD imagers for scientific applications
John Geary, Smithsonian Astrophysics Observatory
Low light level imaging
Paul Beaudet, Westinghouse
Avalanche amplifying solid-state imager
Takao Ando and Hiroyoshi Komobuchi, Shizuoka University
CCD image reorganization for compression
Sabrina Kemeny, Columbia University
CCD focal-plane image half-toner
El-Sayed Eid, Columbia University

5:30-6:30 pm Reception for Poster Discussion. East room.
6:30-7:30 pm Dinner is served. Dining room.
8:00-10:00 pm

Focal-plane image processing
Eric Fossum, Columbia University
On-focal-plane signal processing
Marv Kollodge, Honeywell Systems and Research Center
CCD's retinas
Alice Chiang, MIT Lincoln Laboratories
Z-plane technology for advanced solid-state imagers
John Carson, Irvine Sensors

10:00-11:30 pm Bar is open. East room.

Sunday, May 20, 1990.
7:30-8:30 am Breakfast is served. Dining room.
9:00-10:30 am

High frame rate CCD imagers and UV sensor development
Gary Hughes, David Sarnoff Research Center
Large area Schottky barrier IR FPAs
Jae Kim, Loral-Fairchild
Direct readout of HgCdTe focal plane arrays
Lester Kozlowski, Rockwell International Science Center

10:30-11:00 am Coffee break.
11:00-12:30 pm

New hetrojunction LWIR detector options
Joe Maserjian, Jet Propulsion Laboratory
Quantum well infrared photodetectors (QWIP) for arrays
Chris Allyn, AT&T Bell Laboratories
GaAs readout development for IR FPAs
Nick Doudoumopoulos, Hughes Aircraft Company

12:30-1:30 pm Lunch is served. Dining room.
1:30-2:00 pm Checkout and departure.

Future Trends in Solid State Imagers.

Gene Weckler
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Predicting the future direction of solid state imagers development is not easy. It is not merely the technology that will determine the course. Real world factors like, who will fund it? Who will use it? What is the market? And what are the alternatives will all influence the future? Predictions of the future are generally based on the knowledge of the past, therefore, a review of the major milestones on image sensor development will be presented. The presentation will be informal and open with the hope that everyone will participate.

OUTSTANDING ISSUES IN IMAGERS

T. H. Lee and B. C. Burkey

Microelectronics Technology Division
Eastman Kodak Company
Rochester, NY 14650

CCD image sensors are found in a broad range of applications in consumer, industrial, commercial, defense and scientific arenas. These sensor applications are almost always very demanding. These applications also most always require a compromise in some sensor performance feature and/or are subject to limitation in one or more aspects of performance: signal, noise, spectral response, anti-blooming, smear, data rate, etc. This presentation will outline some of these trade-offs and limitations, and the state-of-the-art as related to some of the above CCD image sensor performance issues.

The 4096x4096 CCD Imager Sensor

R.A. Bredthauer
Ford Aerospace
Newport Beach, California

The design and performance of a 4096x4096 pixel scientific charge-coupled device (CCD) imager is discussed. This is the highest resolution area imaging array manufactured. The device utilizes a 7.5 micron pixel fabricated with three levels of polysilicon. Success with earlier high resolution imagers (1024 and 2048) led Ford to explore a very large 4096x4096 device.

The imager has an active area of over sixteen million 7.5 micron square pixels. A horizontal readout register is located at both the top and bottom of the array. Each register has a single output at one end. The outputs are diagonally opposed from each other giving the chip 180 degree rotational symmetry. Thus if one output fails, the package can be rotated and the device operated with the remaining output. Alternately, one half of the image area can be masked off enabling the device to be used as a 2048x4096 frame store imager.

A standard floating diffusion is used to sense the signal from each horizontal readout register. The node is linked to a single-stage source follower output MOSFET. A geometry of 6x55 microns achieves an output sensitivity of approximately 1.5 micro-volts per electron. Amplifier linearity is better than 0.5% over the sensor's dynamic range. Dark current generation rates using MPP are less than 27 pA/cm^2 at room temperature. Charge transfer efficiency (CTE) for the 4096 imager has been measured at greater than 0.999995. This performance is consistent with smaller Ford CCDs indicating CTE for the 4096 imager is bulk state limited. A photon transfer curve was used to establish low level noise of the output and full well charge capacity. Initial measurements demonstrated a noise floor of 5-10 electrons. Full well capacity was shown to be at least 10,000 electrons when operated in the multi-pinned phase mode. Quantum efficiency has been measured with both thick (5000 A) and thin (1500 A) polysilicon gates. The thin polysilicon shows improved response from 400nm to 700nm.

The 4096 is the first CCD fabricated that can directly compete with the resolution capability of photographic film. The resolution power of the imager is truly remakable. For example, two football fields set side-by-side can be resolved to 1 inch/pixel. The device will see use in high resolution still photography, graphic arts, photo retouching, planetary mapping, and astronomy.

CCD-IMAGERS for HDTV

Albert J.P. Theuwissen,
Phillips Research
Eindhoven, The Netherlands.

High performance CCD-imagers for HDTV-applications require a high resolution combined with a high light sensitivity. These characteristics can be achieved by:

1. high pixel rates on large chips, and

2. simple cell construction with a high aperture ratio.

The paper to be presented will deal with a 1 inch frame-transfer CCD-imager suited for the European HDTV-standard (1250 lines, 50 fields, 2:1 interlacing). The following issues will be addressed:

the large RC-values of the poly-Si CCD-gates make a fast frame transfer impossible. How can this problem be solved, and how is it solved in FIT sensors?

high pixel rates require a high frequency of the output register and a high bandwidth output amplifier. These requirements can be relaxed by a charge packet multiplexing technique.

CCD-chips with details less than 1μm require a 5x or 10x stepper to minimise mask errors, but the large chips in combination with a 5x or 10x reticle require large field of view steppers. This problem can be solved by using separate reticles for the image and storage section of the sensor, and stitching them together on the wafer.

image cell geometry, which fulfills the function of light conversion site and CCD transport channel and which is built on the vertical anti-blooming and charge reset diffusions.

CCD IMAGERS FOR HDTV APPLICATION

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In the past decade, CCD technologies were successfully implemented in studio/industrial-use cameras, as well as in home-use video cameras. CCD imagers, with up to 380,000 integrated pixels, are commercially available, and higher density imagers are requested for electronic still camera systems. On the other hand, for future TV systems or HDTV systems, CCD imagers integrated with more than 2-Million pixels will be installed in an image pick-up system. Four CCDs, with from 1.3 to 2-Million pixels, have been reported by Japanese manufacturers. However, no CCD has sufficiently good characteristics for use as a studio HDTV camera. For example, higher sensitivity and lower smear level should be realized. Many basic technologies have been proposed to achieve better characteristics. Higher sensitivity, for a dark level imaging, will be accomplished by overlaying a monolithic micro lens array, and by an overlaid photoconversion layer. Smear level will be decreased by strictly shielding the photodiode peripheral area, by increasing the internal electric field around the diode area, and by adding a field memory area (FIT architecture). An unwanted fixed pattern noise will be diminished by the future precise pattern rule, and by the fabrication process lowering the dark current level. For a higher signal-to-noise ratio and a higher dynamic range, the optimum design for the vertical CCD read-out register will be investigated, as well as the three dimensional micro machining to the substrate; a trench register structure, for an example. In the HDTV application, internal power consumption, due to a high speed clocking in both horizontal and vertical directions, and to the finite resistivity in poly-Si electrodes, increases the die temperature, followed by a dark current increase. An alternative electrode material (metal-like material) could be used to reduce the resistivity. Moreover, a poly-Si/Al double-layer gate (cross electrode wiring with low resistivity material) effectively decreases the resistivity, even when using the conventional poly-Si transfer electrode structure.

When designing the HDTV camera, other technologies should be investigated; a video signal processing circuit and an optical system. In a video circuit, Reflection-Delayed Noise Suppression (RDS), improving S/N, could be applied instead of the conventional Correlated Double Sampling (CDS). For optical components, lower lateral chromatic aberration, in a full focal length range for a zoom lens and in a full object distance range, would be expected.

A high performance CCD imager for HDTV applications will be developed, with a rapidly progressing DRAM technology backing. Then, the HDTV camera with CCD will be put to practical use in the near future.

THE USE OF A TWO-DIMENSIONAL ELECTRICAL MODEL WITH CURRENT FLOW TO MODEL A CHARGE-COUPLED DEVICE VERTICAL ANTI-BLOOMING PIXEL.

R. D. McGrath, Polaroid Corporation, 21 Osborn Street, Cambridge, Mass. 02139

Imagers for consumer cameras require small pixels with large charge-handling capacity and anti-blooming. The small size makes the task of electrical modeling inherently two-dimensional. The use of static anti-blooming adds the additional complication that during exposure the electrical potential in the pixel is determined by the anti-blooming current [1] and thus a model that incorporates currents is required. This presentation will discuss the use of the two-dimensional device-analysis program TMA CANDE to handle this problem.

A model to handle the vertical anti-blooming pixel must have several capabilities as follows: (1) It must allow the construction of a two-dimensional structure with a top dielectric, with a gate bias and with physically reasonable doping profiles. (2) It must allow the existance of multiple regions of the same type, but with different quasi-Fermi potentials. (3) It must allow the existence of free electron and hole charge and must allow current flow of one carrier type. (4) It should determine potential, charge concentration and current densities as a function of bias conditions.

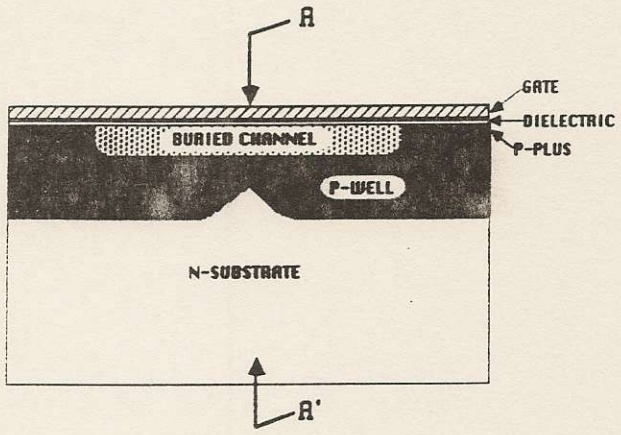
A charge-coupled device vertical anti-blooming pixel can be fabricated by positioning a p-type well diffusion in an n-type substrate, and by patterning p-plus channel stops and a n-type buried channel in the well (Figure 1). Above this structure a dielectric is formed and a polysilicon gate is patterned. The device is biased with the channel stops defining the ground potential, the substrate set positive, and the gate varied between an off voltage below the channel stop bias and an on voltage between the channel stop and the substrate biases. The structure is mostly depleted with the only free holes being in the channel stop and the only electrons being those deep in the substrate and those captured in the buried channel.

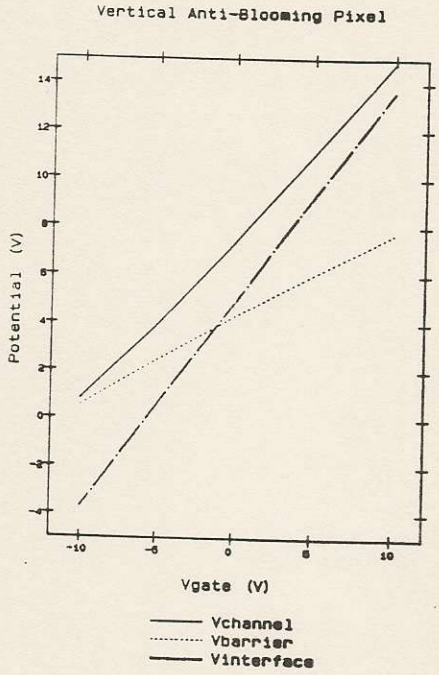
The electrical modeling is carried out for three cases of each set of doping distibutions, gate structure, and substrate and p-well bias (Figure 2). The first corresponds to the off-gate bias and solves for the existence and value of the off channel potential (Figure 3). The second is the solution of the on-gate bias with electron current and is used to determine the dependence of anti-blooming current on channel potential. This is accomplished by interrupting the gate in its center and locating a small contact to the channel through which current can be monitored as the channel bias is varied. From this dependence the channel potential for the saturation level, that which corresponds to the loss of one electron per readout period, and the channel potential for the overload condition can be found. The third is an electrostatic solution of the on-gate bias and is used to determine the dependence of charge-handling capacity on channel potential (Figure 4). From this the charge handling capacity at the saturation channel potential can be determined.

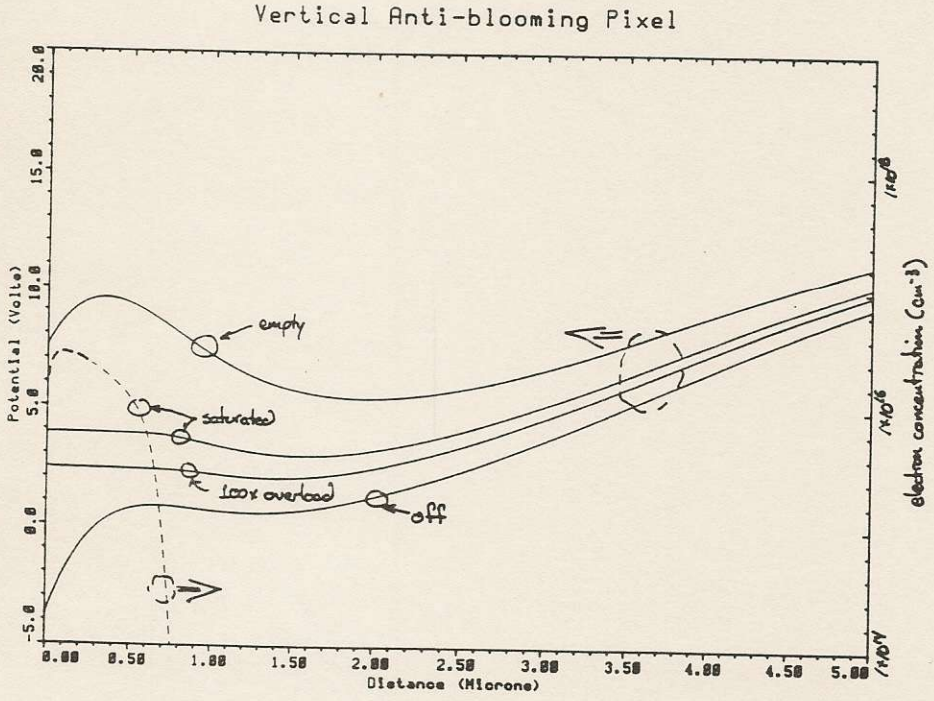
The criteria for a functional pixel include the following: (1) That a potential maximum exist for the off-gate condition. This is so that charge generated in the off-phase will drain into the on-phase and not be lost to substrate. (2) That the anti-blooming barrier height in the overload condition for the on-phase channel potential is higher than the channel potential for the off-phase channel potential. This is the requirement that the vertical anti-blooming will work. (3) That the channel potential for the on-phase at saturation is higher than the potential at the interface. This is required to prevent transfer loss due to interface trapping. (4) That the charge handling capacity meet performance specifications. All of these criteria can be evaluated using the above methodology with CANDE.

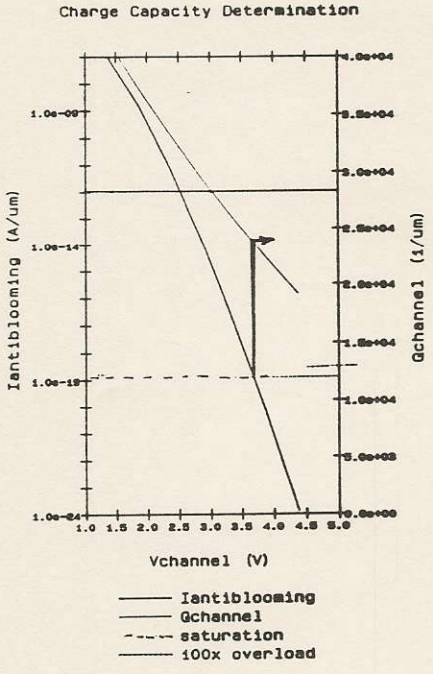
[1] M.J.H. van de Steeg *et al.*, IEEE Trans. Electron Devices, **ED-32**, 1430-1438 (1985)

VERTICAL ANTI-BLOOMING PIXEL









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New radiation problems in CCDs

Bruce E. Woodgate

Abstract

Energetic gamma rays and protons cause damage in CCDs, producing ionization and displacement damage, primarily decreasing their charge transfer efficiency (CTE) and increasing their dark noise.

Gamma rays primarily cause ionization damage. The effects of this can largely be avoided by inverting the phases with respect to the surface. Then an extra implant is required to restore the full well, called the MPP implant. Protons cause both ionization and displacement damage. Inversion cannot protect against displacement damage because it occurs throughout the detector, including the depletion region. The amount of displacement damage varies strongly with proton energy, being much higher at low energies especially below 1 Mev, and when the proton is stopped inside the detector. Fortunately the lower energy protons are more easily removed by shielding. The CTE degradation produced is worse at lower charge levels since a small charge is relatively more depleted by the many small traps produced, and the parallel CTE reduction is less at cooler temperatures as the trap lifetime becomes long compared with the readout time. A narrow extra implant down the middle of the channel, the mini-channel, allows small amounts of charge to be readout while encountering fewer traps than in the whole channel, so both the CTE and dark noise are degraded less. Some reduction of dark current has been observed within a few days at room temperature after a proton irradiation.

CCD AND MOSFET RANDOMLY ACCESSED IMAGE SENSORS: SMART SCANNERS

Savvas G. Chamberlain †

DALSA INC.
CCD IMAGE SENSORS

Abstract

Research is presently carried out on CCD and MOSFET randomly accessed solid-state image sensors. These sensors which can be regarded as "smart sensors" have their roots in self scanned MOSFET linear and area arrays. Some of the problems associated with MOSFET image sensors are very much present in this "new technology". Such problems include, poor charge transfer efficiency, KTC noise, fill-factor, dynamic range and others.

The availability of VLSI fabrication technology and applications such as machine vision, instrumentation, HDTV and scientific applications renewed interest in randomly accessible linear and area photodetector arrays operating in the visible spectrum.

In my talk I shall briefly review some of the current work which different companies are presently carrying out, revisit the self scan MOSFET arrays, highlight their problems and techniques used to address the solution of these problems. I will deal in detail with methods to improve charge transfer efficiency, KTC noise, and fill factor.

It is very much interesting to see an old technology resurfacing and been developed as "new technology" for specific applications.

† On leave from the University of Waterloo, Waterloo, Ontario, Canada.

PRESENT AND FUTURE ROLES OF HIGH PERFORMANCE CHARGE TRANSFER DEVICE DETECTORS IN SPECTROCHEMICAL ANALYSIS

M. Bonner Denton, Department of Chemistry, University of Arizona, Tucson, AZ 85721

Recent advances in the capabilities of state-of-the-art array detectors offer exciting new frontiers for exploration. The latest generation of solid state detector arrays, including charge coupled devices (CCDs), charge injection devices (CIDs) and new hybrid devices, are becoming available in a variety of formats ranging from prototype single element devices targeted to compete head on with photomultiplier tubes (PMTs) to devices containing in excess of sixteen million detector elements. In between lie a host of very high performance detectors capable of outperforming more conventional approaches. New architectures, materials and processing techniques are yielding devices with lower readout noise, reduced crosstalk and improved quantum efficiencies. Recent prototypes have demonstrated promising results from the infrared through vacuum ultraviolet to the x-ray region. Use of unique readout modes, including binning, rapid scan, destructive and nondestructive readout, etc., will be considered. The impact of these detectors on a number of spectroscopic techniques will be discussed. Several applications for improved chemical analysis, including rapid scan, fluorescent and atomic spectroscopy, will be presented as applications to describe a variety of design and software considerations. In each case, the impact of the new capabilities will be demonstrated through examples of experimental system performance. Present and future trends in spectroscopic analysis will be considered.

Micropattern Detectors in Particle Physics

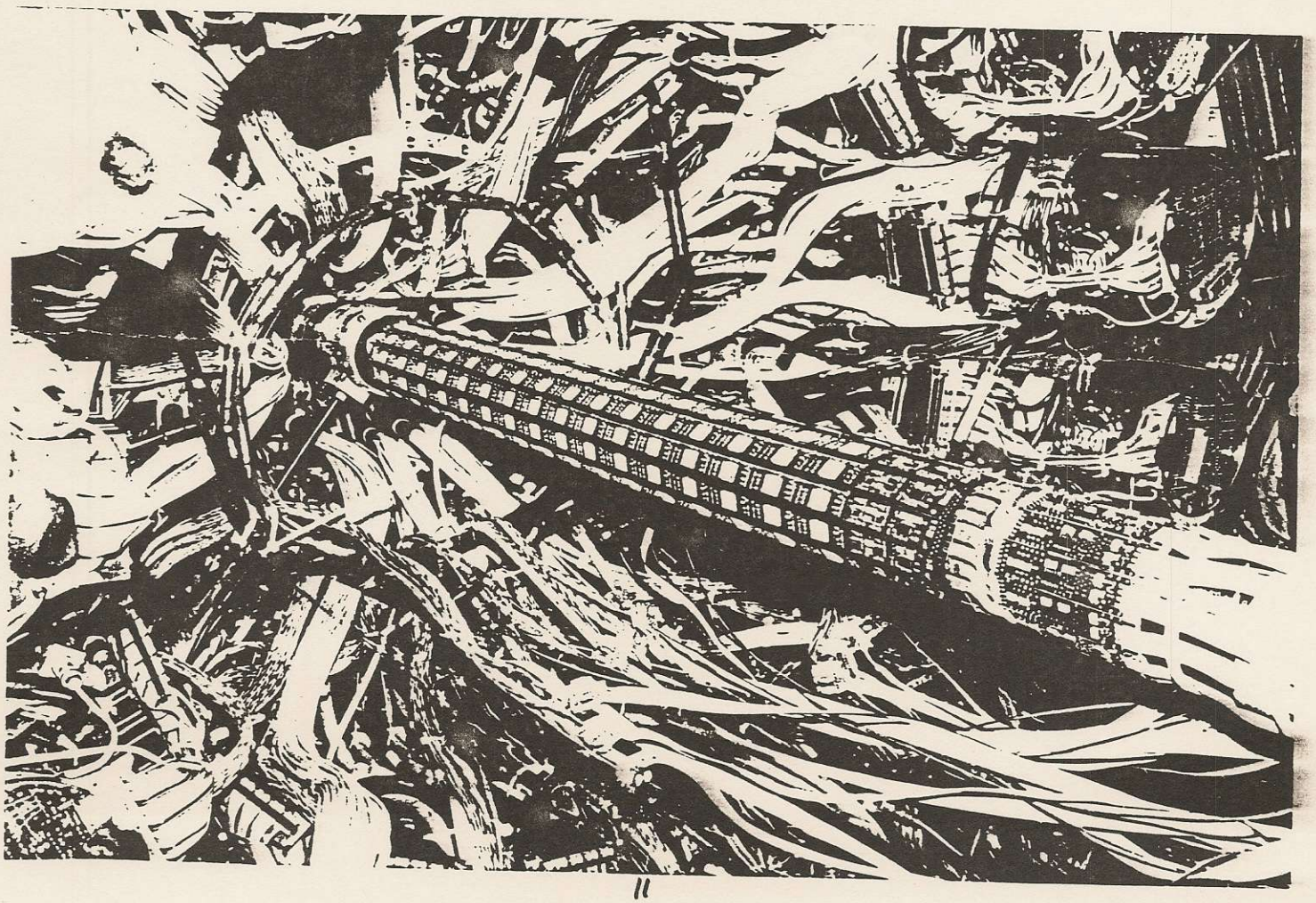
Erik H. M. Heijne CERN EF - Division

Abstract

Microelectronic devices are finding increased use in particle physics experiments both for detection and for information processing. They resemble in several aspects the advanced solid state imaging sensors and processors that are presently developed, e.g. pixel size, signal processing, addressing mode, etc. However, they are specific in that they have to deal with sparse information and have to look at non-recurrent, non-redundant images which occur at uninterrupted rates of 50 to 100 MHz. In order to obtain charge signals of 10000 e-h pairs (2 fC) from the ionizing particles of interest, the 'photodiode' array has to be built on high resistivity silicon. A depletion thickness of 100 um to 300 um can be achieved.

Two approaches can be distinguished in the development of the so-called silicon pixel detectors. The first uses a matrix of charge integrating elements which can be periodically read out by adressing of these elements. The advantage is that such a structure can be based on a hybrid integration of already existing circuits as developed e.g. for IR imaging.
In the second, one attempts to integrate within the space of a pixel a fully active microcircuit with low-noise signal processing, comparator and memory element. The active pixels can identify themselves if they have been hit, and a hierarchically organized readout system may allow extremely fast information extraction.

Several practical systems are to be described, of which one is pictured below. It is a 3000 element tubular matrix, covering 1000 square cm, with superimposed CMOS readout circuits. The signal peaking time is 800 ns, and the readout of all channels is multiplexed. The total in-situ power dissipation is 4 W.



Shallow-Buried-Channel CCDs with Built-In Drift Fields*

A.L. Lattes, S.C. Munroe
Lincoln Laboratory, Massachusetts Institute of Technology
Lexington, Massachusetts

Abstract

The performance of CCDs is limited by the residual charge that is left behind after the bulk of the charge packet has transferred by self-induced drift. In the absence of drift fields the electrons will transfer by thermal diffusion, which is a very slow process. The CCD speed can be enhanced by designing structures with strong fringing fields between gates, such as deep-buried-channel CCDs. Deep-buried-channel delay lines have indeed been demonstrated at record speeds (hundreds of megahertz) but they have several disadvantages that may ultimately limit their usefulness. For example, the shape of the potential wells is distorted, degrading linearity and affecting the overall signal-processing performance of the CCD. Furthermore, the charge-handling capacity decreases as the channel moves into the bulk and at least 10-V clocks are required. These 10-V clocks are not only difficult to generate at high speed, but are incompatible with the 5-V technology necessary for the high-performance on-chip support circuits that interface with the CCD. To overcome these disadvantages we have designed, fabricated and tested shallow-buried-channel delay lines (channel depth = 300 nm), operated with 5-V two-phase clocks, with a built-in potential gradient (generated by a step implant in the storage gates) to improve the charge transfer efficiency. The effect of the step implant is dramatic. Long-gate CCDs (26-μm storage gates) with built-in drift fields are five times faster (12 MHz) than the uniform CCDs. In addition, the electric field overcomes imperfections and bulk trapping in the channel, resulting in an improved performance even at very low speeds. Short-gate CCDs (7-μm storage gates) with the built-in drift fields were tested up to 315 MHz (the limit of the existing clock drivers) with no measurable degradation in the CTE, while the equivalent uniform CCDs degrade at 230 MHz. These results are consistent with two-dimensional computer simulations, which predict 250 MHz and 400 MHz operation for the uniform and step-doped CCDs with 5-V clocks. The storage step implant is a simple processing step that provides the CCD designer an additional degree of freedom previously unavailable. In addition to lowering the required clock voltages, the built-in drift fields allow CCD gates or shift register lengths to be increased while preserving speed.

*This work is sponsored by Lincoln Laboratory Innovative Research Program

5-V Uniphase CMOS/CCD Process for Mixed-Signal Processing*

S.C. Munroe, A.L. Lattes, D.B. Whitley, and D.R. Arsenault
Lincoln Laboratory, Massachusetts Institute of Technology
Lexington, Massachusetts

Abstract

We have developed a 2-μm CMOS process to allow integration of high-performance analog, digital, and discrete-time analog (CCD and switched-capacitor filter) circuitry. Such capability will allow us to design very sophisticated mixed-signal chips in which every function is optimally implemented. The basic process is a double-polysilicon (both levels active), double-metal,n-well CMOS process that allows high density and a high level of integration. MOSFET gate oxide is sufficiently thick (50 nm) to guarantee reliable operation with ± 5-V power supplies, which are the new standard for analog signal processing. The process also supports high-performance, uniphase CCDs operating with standard CMOS logic swings (ground and + 5-V rails). With this arrangement the charge packets under the unclocked "dc" phase can be sensed nondestructively with floating-gate taps.

Design of the CCD buried channel to enable 5-V operation (clock, drain, source) presented the greatest challenge in this process development. Our previous buried channels were analyzed using the process and device simulation programs SUPREM and CANDE. The analysis indicated that much of the buried-channel implant was inefficiently used since it did not contribute to making the charge packet larger but made the channel potential too positive for 5-V uniphase operation. Using SUPREM and CANDE, we were able to design a shallow buried channel profile that retained the high charge density required for good dynamic range (2,000 electrons/μm^2) while simultaneously achieving channel potentials and well depths compatible with 5-V uniphase operation. Measurements on CCD test structures are consistent with our calculations and have verified that the charge capacity of the new buried channel is not compromised with this new process. CANDE simulations of the CCD indicate that, for the 6.5-μm transfer gate lengths used, the fringing fields are strong enough to allow clock rates greater than 100 MHz. Furthermore, the process was designed to be compatible with our step-doping technology,[1] which allows us to build in the drift fields necessary for even higher-speed charge transfer.

Characterization of this CMOS/CCD process is nearly complete, and we are well into the design of a CCD-based correlator (a 58-K MOSFET chip) that will use our new process to achieve 5×10^{10} operations per second with 100-MHz clocks. The 5-V compatibility of the CCD opens up many possibilities that were previously impractical. For example, many short CCDs could be operated in parallel under control of a master 5-V clock to perform multiple-valued logic functions or act as neurons in a neural net. The ability to integrate all three signal-processing domains in an optimal fashion will also enable us to integrate on a single chip a large fraction of complex systems, such as spread-spectrum receivers.

1. Shallow-Buried-Channel CCDs with Built-In Drift Fields, A.L. Lattes, S.C. Munroe, to be presented at this workshop.

*This work is sponsored by NASA Goddard Space Flight Center.

Transient Simulation of Millimeter Wave CCD's

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A two-phase CCD capable of operating at millimeter wave frequencies is proposed. Results of transient simulations in PISCES indicate that such a device based on existing InAlAs/InGaAs HEMT technology, with 0.5μm gate lengths, can achieve CTE of 0.999997 at 40 GHz. Simulation results are given for an AlGaAs/GaAs device at 0.2 and 20 GHz, and for an InAlAs/InGaAs device at 40 and 80 GHz. These simulations show that the charge packet is moving largely at Vsat and that gate length, as in FET's, is the critical parameter to high frequency performance. However, unlike the case for FET's, high-performance devices with a total transfer length of 1 um, which can be defined by optical lithography, can achieve operating frequencies greater than 50 GHz. In addition to the CTE results, the process tolerance and power consumption of this device are also explored.

GaAs/AlGaAs MQW Dectors

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The Aerospace Corporation

GaAs/AlGaAs multiple quantum well (MQW) detectors with $D^* = 10^{13}$ cm$\sqrt{\text{Hz}}$/W at 10μm and 20K have been demonstrated. These detectors exhibit excellent reproducibility, uniformity, and radiation hardness. With further improvement in performance, particularly quantum efficiency, this technology may become competitive with more mature technologies such as Hq Cd Te and extrinsic silicon for low-background applications.

2DEG CCDs For Advanced III-V Detectors

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With the maturing of molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD), the responsive spectrum of detectors has been extended by the bandgap engineering of various III-V material systems. Although bandgap engineered detectors are still in their infancy, various types of detectors are emerging. The advanced detectors include heterostructures and multiple quantum wells utilizing internal photoemission, strained layers, and resonant tunneling. As the technology of the advanced detectors matures, there has been an increasing demand for monolithic readout multiplexers for detector arrays for scientific imaging applications.

GaAs and related heterostructure CCDs are primary choices for the readout multiplexer for the advanced III-V detectors since most of the detectors can be integrated on a GaAs substrate. Two-dimensional electron gas (2DEG) heterostructure CCDs are attractive for high performance readout applications since they have several advantages over conventional buried-channel CCDs: a larger charge handling capacity (larger dynamic range), a higher electron mobility at low electric field (higher transfer speed and reduced clock swing requirement) and low temperature (improved low temperature performance), and an integrability with high performance 2DEGFET circuitry.

2DEG resistive-gate CCDs were fabricated on both uniform- and planar-doped AlGaAs/GaAs heterostructures. The CCD was a four-phase, 32-stage delay line (1 um wide electrodes spaced by 4 um with a 100 um channel width). Electrical characterization of the CCDs was performed at various frequencies and temperatures. Both CCDs exhibit high charge transfer efficiency (CTE) over their respective operating ranges. At room temperature, the uniform-doped structure had a CTE of 0.999 for clock frequencies between 13 MHz and 1 GHz (our test station limit). The gate leakage current of this structure prevented testing below 1 MHz. The planar-doped structure resulted in a reduction of leakage current by a factor of 300 at room temperature, thus extending the low frequency limit by a similar factor. The CTE of the planar-doped structure was also increased and was measured to be 0.9997 at 130 kHz.

The 2DEG CCD shows promise for use in high speed analog signal processing and readout applications as well as in low frequency imaging readout applications. In order to investigate the feasibility of monolithic integration of 2DEG CCDs with advanced III-V detector arrays, a new multiproject mask set was designed. Multiplexers for different types of detectors (photoconductors and photodiodes) with various detection methods (direct and indirect detection) and signal coupling schemes (direct injection and gate modulation) are included. 32-stage linear arrays with a 28 um by 28 um pixel size and a four-phase clock scheme for different detection methods and signal coupling schemes are designed. A 32x32 2-D array for the direct detection method was also included. By utilizing appropriate portions of the mask, different multiplexers can be fabricated on different detector structures for experimentation. Through monolithic integration of 2DEG CCDs with advanced engineered bandgap detectors with the new mask, significant advancement in the understanding of 2DEG CCD focal-plane arrays for advanced III-V detectors is anticipated.

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2D Meander Channel CCD Imager Scanner on GaAs with Photoconductive Detectors

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ABSTRACT

Two-phase meander-channel CCD shift registers have become widely used as the standard charge readout devices in 2D silicon-based solid state image scanners. This type of CCD register provides the largest fill-factor in front surface scanners and the need for only two electrode phases produces the simplest driver electrode interconnect scheme. A way has now been found for producing similar 2-phase meander-channel CCD shift registers on GaAs using a novel fabrication process. This process is based on the use of (a) anodic oxidation for producing very thin dielectric isolations between closely packed Schottky barrier metal electrodes and (b) recessed gates to produce self-aligned potential barriers between the adjacent charge wells of the meander channel.

In addition, the semi-insulating property of GaAs has been utilized to produce high speed photoconductive sensors which are simple to fabricate since they require very little inherent processing. A typical design for such an imager has a unit cell size of 33.5 um x 18 um making it possible to stack over 160,000 such cells into a 1 cm^2 chip area. This is comparable to state-of-the-art CCD scanners presently available in silicon. However, the GaAs versions are capable of providing far superior operating speeds.

At the present time all CCD structures have been produced by implantation of active device regions into semi-insulating GaAs which today is readily available in sizes up to 4 inches diameter with defect densities as low as $10^3 cm^{-2}$. This fabrication process is basically compatible with the standard implantation process used in the production of standard digital integrated circuits in GaAs.

NOISE AND CHARGE TRAPPING IN CCDs

Buried channel operation of CCDs and MOSFETs is aimed at improving charge transfer efficiency and reducing the noise floor. Dramatic improvements have been obtained but the understanding of the remaining problems is still limited.

Our model of an ideal depletion mode MOSFET predicts that interface traps will give a low frequency (L.F.) noise with a $1/f^2$ spectrum due to traps with an activation energy between half the bandgap and that of the intrinsic carrier density. This noise component is found in all depletion mode MOSFETs. However there is also a 1/f component which can be predicted less accurately and is strongly dependent on the details of the device design and manufacture. This latter component has all the characteristics of inversion mode devices and is generated by traps deeper in the oxide.

The excess 1/f noise is much greater in MOSFETs in CCDs than some discrete MOSFETs. We have also found complex ageing effects which affect the noise level of some depletion mode MOSFETs as a function of the history of temperature and bias. Increased noise levels generated by impact ionisation in the channel due to temporary increase of the drain voltage to 5V at reduced temperatures may take many hours to recover to their original value. This noise level is related to the efficiency with which holes can be removed from the depletion region under the channel. Second order effects due to traps in and around the other boundaries of the channel have also been studied.

It is also found that all depletion mode devices exhibit L.F. noise due to bulk Si traps as in JFETs. Our studies of noise in devices as a function temperature and device parameters has enabled us to characterise energy levels and capture cross sections of these traps at densities considerably lower than can be detected by DLTS methods. These findings can then be applied to explain the behaviour of traps in and around the CCD channel as a function of clock duration and temperature.

The transition from the transient field conditions that apply to the CCD channel to the steady state conditions in the output MOSFET is particularly interesting. In order to obtain a detailed balance of all charges it is necessary to include the holes from the p-type dopant in the channel which accumulate in the potential wells above the cahannel and are responsible for the excess 1/f noise. We are also seeking an explanation for the long periods required for clocking out the background (leakage) current in the CCD. Some tentative suggestions for the mechanisms which limit the charge transfer efficiency are being proposed.

References

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SOME LARGE-FORMAT CCD IMAGERS FOR SCIENTIFIC APPLICATIONS

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Abstract

Several large-format CCD's have been designed and are in process at the Ford Aerospace fabrication plant. One is an edge-buttable 2048 X 2048 device that will allow a 2 X 2 array to be formed with an imaging area measuring more than 61 mm on a side and with only 400 microns dead space between arrays. Another is a 3072 X 1024 CCD with both floating diffusion and non-destructive read floating gate amplifiers. Also included are smaller arrays of 2688 X 512 and 1200 X 800 in the chords of the wafers. All of these designs were accomplished by a non-specialist scientist using AutoCAD on an inexpensive PC, a level of customer interaction with CCD manufacturing not previously available.

LOW LIGHT LEVEL IMAGING

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ABSTRACT

The Westinghouse Sensor System Technology group low light level development programs in the visible (.3 to .9μ) and mid-wave IR will be described. Preliminary theory and results on low leakage virtual phase devices and low noise amplifiers will be presented. Description of a 2K x 2K starring array at 18μ pitch with front side illumination at high quantum efficiency will be given.

An InSb very low NEΔT mid-wave IR camera having a 128 x 128 area array bump bonded onto a silicon processor for low background application will also be described.

Avalanche Amplifying Solid-State Imager

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The possibility is investigated of an avalanche amplifying solid-state imager. A special designed 5-pixels Si avalanche photo-diode (APD) array operated under a charge storage mode is built.

In below-breakdown operation, photo-electric conversion characteristic is divided into two regions. The slope of the curves γ in these regions is corresponding to γ=1 and 0.5, respectively. Increasing reverse bias applied to the APD, the nonlinear conversion region equivalent to γ=0.5 become dominant and be practically independent on an inherent gain of the APD. These properties are due to self-quenching of the gain. It is found that the variation of the responsivity of the array caused from the inherent gain non-uniformity is drastically decreased and approaches to the level roughly equal to a half of the pixel capacitance uniformity.

The reduction of the variation is more successful for the array having smaller pixel capacitance. The fact is important for applying the APD to an imaging sensor.

In above-breakdown operation, magnitude of the output signals is regardless of incident light input, while the rate at which the output signals are observed during a given time interval is modulated in proportion to it. Consequently, photon-counting imaging can be feasible.

It is concluded that the array could be applicable over a wide field from extremly low-light level imaging to normal video camera use.

CCD IMAGE REORGANIZATION FOR COMPRESSION

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The design of four CCD-based chips for the reorganization of image data for lossless image compression is presented. A 256 x 256 buried channel frame-transfer device with 15 um^2 pixels has also been designed. Conventionally, imagers deliver pixel data in a raster-scan sequential format. Typical of many image processing tasks, the image coding scheme used in our lossless compression algorithm requires 3 x 3 pixel neighborhood blocks with the center pixel arriving first. Several techniques for accomplishing this type of neighborhood reconstruction (NR), consisting of both row and pixel reordering operations are described. The CCD NR circuits are designed to operate at a 30 Hz frame rate with minimal power dissipation (< 10 uW) and real-estate (< 250 x 400 um^2). Differential output provides off-chip electronics with data suitable for coding and compressed transmission. Two of the CCD NR chips are designed for hybridization to the CCD imager within a standard 68 pin package, while two are integrated with the imager on the focal-plane.

CCD FOCAL-PLANE HALF-TONER

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Half-toning is the process of transforming continous-tone images into bi-level images for display on devices that are binary in nature. Error diffusion is an adaptive half-toning algorithm developed by Floyd and Steinberg that provides high spatial resolution at low contrast.

In this presentation, a charge-coupled device-based imager/processor chip for producing half-toned images using error diffusion is described. The chip is a monolithic integration of a frame-transfer imager and a half-toning processor. The pixel size of the 256 X 256 pixel buried-channel three-phase imager is 12 X 12 um^2. The pipelined surface-channel processor is projected to operate at 25 MHz. The chip is projected to achieve real-time operation (if needed) at a frame rate of 30 frames per second. The architecture is also suitable for large format line imagers.

The chip is currently in fabrication using a triple-polysilicon, double-metal process. The first level of metal is used for wiring while the second one is devoted to light shielding the non-imaging part of the chip. Selective implantation is used to integrate surface- and buried-channel devices.

Focal-Plane Image Processing

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Abstract

This talk describes recent activities at Columbia in the merging of image aquisition and image preprocessing functions on the same chip, or focal-plane image processing. Such on-chip signal processing finds application when either simple processing is readily accomplished using charge-transfer devices, as in the case of image reorganization and local neighborhood reconstruction, or when the throughput and/or power requirements of the system can not be easily achieved with standard digital signal processing.

The tools used to realize on-chip signal processing in the analog charge domain are presented first. The major tool is termed wire transfer, and allows the topological crossing of charge-domain signals using metallic wires. Other tools include charge packet splitting, routing and comparison.

The signal processor can either be serial, fully parallel, or semi-parallel[1]. These architectural approaches are described and illustrated with activities in progress at Columbia. Serial processors include image reorganization for a compression codec[2] and image half-toning[3]. Semi-parallel architectures may be useful for non-uniformity correction (NUC) and gamma circumvention. A CCD-based programmable gain control circuit (functionally equivalent to a multiplying D/A converter) with 10 bit resolution and 8-bit accuracy will be described for NUC. Fully parallel architectures yield the highest potential throughput at the expense of layout complexity and unit cell size. A single-instruction, multiple data (SIMD) parallel array processor has been designed and fabricated. The unit cell has been tested and found to be functional with medium performance. This real-time image processor chip will be described.

1. E.R. Fossum, "Architectures for focal-plane image processing," Optical Engineering 28(8), 865-871 (1989).
2. S.E. Kemeny, et al., see abstract in this program.
3. E.S. Eid, et al., see abstract in this program.

Abstract

On-focal plane signal processing
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The need to consider on-focal plane signal processing is mission or application driven. Because real estate is at a premium on or near the detector focal plane and, for cryogenic detectors cooling is critical, one would not normally choose to add to the complexity of the focal plane array or add to the cooling requirement. Assuming a cooled detector array, the primary drivers for on-focal plane processing are the very large amounts of data that have to be processed in real time and the need to transport picowatt signals from the focal plane array region into a warmer and electromagnetically noisy environment. These factors transform into design requirements for very wideband data transmission, the possibility of detector signal contamination by noise and mechanical, thermal, and electrical problems imposed by the large number of discrete detector output leads. In this case an option is to perform a number of the signal processing functions at or near the detector array and at or near the detector operating temperature to minimize the above possibilities. In fact, all functions performed in real time on each detector (time dependent processing) are good candidates for consideration for on-focal plane processing. The intent is to perform that processing which will reduce the output data rate.

The solution to on-focal plane signal processing is an on-going activity. There are presently a number of development programs sponsored both by the military and by universities. A detailed exposition on all of these programs is beyond the scope of this paper. In this paper I will address the program activity within Honeywell Systems and Research Center. In our basic approach we use CCD technology to construct processing components which use charge for arithmetic operations and charge transport interconnect for data transmission. The Parallel Image Processor (PIP) was developed in the early 1980s to perform basic automatic target recognition (ATR) functions. A few years later we developed an analog array processor (AAP) which was twice as large and included more complex functions, in particular more capability was provided to read data in and out of the array. More recently we have proposed more advanced concepts to enhance and optimize the architecture and components for on-focal plane processing for infrared mosaic sensors. These concepts will be briefly described along with a discussion of both the requirements drivers and design trade-offs.

CCD Retina

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The integration of signal processors with photosensors makes it possible to perform simultaneous, parallel computations on each pixel in real time. An interline-transfer area imager can be designed with integrated CCD signal-processing elements between neighboring pixels to simulate a solid state or a biological system with locally connected interactions between its neighboring cells. In particular, a retina can be designed to perform such computations as time derivatives of temporal-varying pixel intensity function and minimization of the global energy function due to local spatial intensity interactions. The retina can be used for image restoration of a corrupted, noisy optical input, and also for motion detection. A solid state retina capable of restoring and segmenting an noisy image is described here. Given a measured image, assuming the measurement is a corrupted or a distorted version of the original image, the purpose of this device is to reconstruct or restore the original, uncorrupted scene by estimating its maximum a posteriori (MAP) distribution.

In general, intensities of neighboring pixels in an image are correlated: the probability function for the intensity of a given pixel is fully specified by the intensity values of its neighboring pixels. This image attribute can be modeled by a local pixel-intensity probability distribution function such as Markov random fields (MRF). Furthermore, the Hammersley and Clifford theorem can be used to prove that the pixel intensity of an image is a MRF if and only if its joint distribution function is a Gibbs distribution. Images generated by sensors such as video cameras or radar sometimes are distorted or contain a noise term introduced by the measurement process. It can be shown that the posteriori distribution function of a measure image can also be expressed as a Gibbs function with an equivalent energy function. The image restoration task is to estimate the original noiseless image by computing the MAP distribution. In practice, to solve this MAP problem, it is more convenient to work directly with the energy function and to compute the minimum energy state rather than maximize the a posteriori distribution function.

It should be noted for a 128×128-pixel 256-gray level image, the total number of possible energy states is 256^{16384}. To find a minimum from all the possible states is a formidable task. By means of the Metropolis algorithm, the minimum energy state can be estimated by simulated annealing or stochastic relaxation. Using this approach, Geman and Geman have demonstrated good image restoration and segmentation results. For VLSI implementations, it is preferable to use a gradient descent method to minimize the energy function, which allows us to derive a set of simultaneous dynamic equations for updating pixel intensities. A minimum energy state can be estimated by using an iterative method simultaneously updating each pixel intensity in a way that the rate of change of intensities of a given pixel equals to the gradient of the energy function evaluated at the pixel site.

Z-PLANE TECHNOLOGY FOR ADVANCED SOLID STATE IMAGERS

ABSTRACT

Z-PLANE TECHNOLOGY HAS BEEN UNDER DEVELOPMENT FOR A LONG TIME FOR ADVANCED MILITARY SENSOR APPLICATIONS. IN RECENT YEARS, THE TECHNOLOGY HAS MATURED RAPIDLY, OWING IN PART TO A BOOST RECEIVED FROM COMMERCIAL APPLICATIONS OF ITS ELECTRONICS PACKAGING ASPECTS. THE STATUS OF THE TECHNOLOGY IS REVIEWED, IN TERMS OF DETECTOR ARRAY SIZE, SIGNAL PROCESSING FUNCTIONALITY, AND PERFORMANCE. SOME INTERESTING RECENT DEVELOPMENTS ARE DISCLOSED, INCLUDING A POWERFUL IMPLEMENTATION OF AN IMAGING NEURAL NETWORK. Z-PLANE TECHNOLOGY IS ESSENTIALLY A PACKAGING CONCEPT WITH INTRIGUING NEW SIGNAL PROCESSING ARCHITECTURE POSSIBILITIES THAT CAN BECOME A SIGNIFICANT PART OF THE SENSOR DESIGNERS REPERTOIRE.

High Frame-Rate CCD Imagers and UV Sensor Development

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The design for two high fill-factor CCD arrays for optical signal processing applications is described. The imaging registers have 1024 x 1024 and 512 x 512 pixels and achieve virtually 100% optical fill factor through the use of substrate thinning and back illumination. High frame-rate readout is obtained by the use of a dual storage register and multiple floating-diffusion output ports resulting in reduced readout frequency. On-chip correlated double sampling amplifiers are implemented to reduce the readout noise and simplify off-chip analog signal processing. Both chips include anti-blooming drain structures and ESD protection circuits.

A new virtual UV detector structure is described which has demonstrated stable, high quantum efficiency from wavelength of 140 nm to 900 nm. The construction of this detector is compatible with virtual gate technology for frontside illumination and thinned backside illuminated frame transfer imaging

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LARGE AREA SCHOTTKY-BARRIER IRFPAs

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ABSTRACT

We describe two PtSi Schottky-barrier infrared focal plane arrays; they have 488x512- and 244x256-element monolithic interline transfer CCD architectures. The unit cell of these devices is 25(V)x31.5(H)um. Each diode has a photosensitive area of 282um^2, around which a lightly doped guard-ring suppresses the edge leakage. NEDT and low-frequency MRT measured less than 0.1K with f/1.8 optics, 3.4um longpass filter, and 30 frame/second integration rate under 300K background radiation. The quantum efficiency is approximately 1% at 4um. The high-frequency photoresponse nonuniformity was measured with less than 0.4% rms across the array. The charge handling capacity of about 500Kel and a blooming control feature makes these devices useful for a wide variety of scene temperatures. The signal dynamic range is approximately 63dB against a 300K background.

DIRECT READOUT OF HgCdTe FOCAL PLANE ARRAYS

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Abstract

Photovoltaic HgCdTe is an especially flexible material offering high performance over a wide range in operating temperatures and spectral regions. As a result, hybrid HgCdTe FPA technology represents not just one IR device, but a continuum of high performance products. Rockwell is committed to developing PV HgCdTe focal plane arrays for applications requiring both high sensitivity and only a few or many thousands of elements. Our SWIR (2.5 μm) and MWIR (up to 5.5 μm) 256x256 hybrid focal plane arrays are the most sensitive, tv-resolution devices yet reported. Uses for these and other devices include the military, astronomy, medical diagnostics, spectroscopy, passive and active surveillance, robotics, and many others not yet contemplated. Depending upon requirements, HgCdTe FPAs can be optimized for operation at room temperature to well below 77 K.

Discussed in this paper is the methodology in place at the Science Center for designing and developing high density mosaic readouts and hybrid FPAs. Topics include a brief discussion of the use of producible alternative substrates (to CdTe) for HgCdTe epitaxy (PACE); 1/f noise data for PACE material; the use of direct readout switched-FET readouts for IR FPAs; design methodology and characterization of 128x128 readouts for high background LWIR/MWIR applications; and data describing the design and performance of the MWIR 256x256.

New Heterojunction LWIR Detector Options*

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We investigate a heterojunction internal photoemission (HIP) approach that potentially offers LWIR photovoltaic detector performance (single pixel) that is competitive with the best of other approaches being considered. Most significantly, our approach also offers a relatively simple device technology that promises producible and uniform FPA's. We emphasize an exciting mechanism based on intervalence band absorption. We investigate both III-V and Si-based heterojunctions grown by molecular beam epitaxy (MBE) in which the barrier can be tailored to the desired cutoff wavelength. In addition, MBE allows one to optimize the device structure with precise control of doping profiles and layer thicknesses, and perform band structure engineering by control of composition and heterojunction strain.

We also consider free carrier absorption in heterojunctions. Acceptable absorption coefficients can be achieved in very heavily n^+ doped semiconductor layers ($\approx 10^{20}$ cm^{-3}). However, in this case the appreciable filling of conduction band states leads to a Schottky-like photoresponse with a gradual (quadratic) turn-on above threshold. A more satisfactory approach would be to use p^+ doping so that with the higher density of states in the heavy hole valence band there would be a narrow band of occupied states. This gives the desirable effect of a more rapid (linear) turn-on above threshold. Unfortunately, the higher hole effective mass also reduces (inversely) the free carrier absorption. For this and other reasons, the intervalence band absorption process looks much more promising.

The valence band structure of GaAs (and closely related alloys) is particularly attractive for achieving an optimum effect. The light and heavy hole bands become parallel at values of wave vector **k** away from the zone center, separated by a constant energy of about 80 meV along the <100> directions. The parallel E-**k** behavior leads to a large joint density of states and correspondingly, a large absorption coefficient α for photon energy $h\nu$ equal to this separation (corresponding to wavelengths $\approx$15 μm). This effect requires heavy doping (>10^{19} cm^{-3}) so that states are occupied to sufficient values of **k**. Extrapolation of theoretical work of E.O.Kane and published absorption data suggest $\alpha > 10^4$ cm^{-1} for our case of interest. Theoretical calculations are in progress to extend Kane's early work.

Some interesting features are immediately evident. The selection rules for these transitions *prefer normal incidence of light* (giving a $\sin^2\theta$ distribution of **k**-directions, where θ is the angle from the field vector in the plane of the layer). Furthermore, photoexcitations between the <100> E-**k** bands generate the dominant **k**-directions normal to the heterojunction interface of (100) oriented material. We have the opportunity of tailoring the interband separation to the desired value of $h\nu$ and matching with an optimum (slightly smaller) heterojunction barrier ϕ. In this case the conservation of transverse momentum at the interface is satisfied for most **k**-directions of photoexcited holes. Holes excited in the

* This work was sponsored by NASA and SDIO/IST.

reverse direction can be redirected in the forward direction by reflection from a higher barrier (e.g., AlGaAs/GaAs). Therefore, inelastic scattering losses can be minimized with an optimum layer thickness to achieve a maximum quantum efficiency η.

In the case of Si-based structures, we can still utilize transitions to the split-off valence band. In this case we lose some of the above advantages, but still retain strong absorption (large matrix element) and favorable selection rules. We can also use band structure engineering through control of composition and interface strain to optimize the intervalence band transition energies relative to the heterojunction barrier (i.e., the cutoff wavelength).

Preliminary results on $Si_{1-x}Ge_x/Si$ heterojunctions are encouraging (see T-L. Lin, next session) and work on $In_xGa_{1-x}As/\ Al_xGa_{1-x}As$ heterojunctions is just getting under way. The opportunity exists for fabricating photovoltaic detector structures designed to achieve maximum η and the limiting thermionic emission dark current at the heterojunction. To minimize inelastic scattering loss of photoexcited holes while still obtaining adequate absorption per layer (e.g.,>1%), the p^+ layers must be of some optimum thickness (e.g.,≈60 nm). The total absorption can be enhanced by multiple passes; for example, two passes with a single reflector or 2N passes in an optical cavity structure (as commonly done with SB detectors). The HIP structures can also be configured as two stacked diodes connected in parallel (straightforwardly with planar technology) to gain another factor of two.

Based on the above considerations, we project $\eta > 0.10$ in optimized detector structures. The thermionic emission limited detectivity [$D^* \rightarrow (\eta/h\nu)(2J_o/e)^{-1/2}$, where $J_o = 120(m^*/m)T^2\exp(-\phi/kT)$ A/cm^2] becomes $D^* > 4\times10^9$ cm-Hz$^{1/2}$/W, for 15μm peak response ($h\nu$=82 meV), with $\phi = 0.9h\nu$ and T=65K. This gives a noise equivalent differential temperature NEDT<0.01K for a background temperature of 300K (assuming f/2 optics, 50μm square pixels and 30Hz bandwidth). Therefore, even with relatively low η, the thermionic emission dark current of HIP detectors provides excellent pixel performance. Most important, the simplicity of the HIP structure offers real promise for producibility and uniformity which often are the limiting factors for FPA performance.

Quantum Well Infrared Photodetectors (QWIP) for Arrays

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AT&T Bell Labs is developing a novel IR detector technology based on Band Gap Engineering in the III-V material system. The Quantum Well Infrared Photodetector (QWIP) concept has great promise for application to array-based imaging systems throughout the IR spectrum. QWIP devices in the GaAs/AlGaAs materials system have been fabricated with response in the 8-12 micron (LWIR) band and can be designed for longer wavelengths.

QWIP technology has the necessary elements for successful application in IR imaging. QWIP devices have well behaved dark-current IV relationships, responsivity, wavelength response tunability (by growth parameters), device speed, uniformity of parameters, and radiation hardness. The extension of the present state-of-development to large arrays is likely to succeed, based on the success of GaAs IC technology. A 16K GaAs SRAM is similar to a 128x128 QWIP array in chip size, with considerably less fabrication complexity.

In addition to conventional IR array applications, the QWIP concept makes possible unique new system capabilities not available with present LWIR technologies. Full monolithic integration of sensor, readout, and processing circuitry is possible with QWIP, as is development of multi-spectral detector arrays.

The talk will present a review of the research results obtained on the GaAs/AlGaAs QWIP devices and will present a path to development of QWIP arrays and supporting technologies.

GaAs READOUT DEVELOPMENT FOR IR FPAs

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Alternate materials (to Si) for IR FPA readout development have become of interest for several IR imaging applications. The three primary benefits sought from an alternate readout technology are thermal compatibility with the detector material, a high speed to power ratio and enhanced radiation hardness. GaAs is one alternate readout technology currently being pursued at Hughes which satisfies all three of the above criteria.

A detailed discussion for the motivation behind GaAs as an IR FPA readout technology will be presented. The key to demonstrating GaAs as a viable technology is the development and control of a cryogenic GaAs fabrication process. Hughes' GaAs process features, uniformity and yield will be discussed. Once a yielding, uniform process is established, a thorough understanding of the cryogenic FET performance must be developed for readout circuit design and simulation. Key performance parameters of Hughes' FETs, for IR FPA applications, will be presented. Finally, input circuit architecture considerations relative to current device performance and uniformity will be discussed.

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