CTR

Center for Telecommunications Research

1986 IEEE

WORKSHOP

ON

CHARGE COUPLED DEVICES

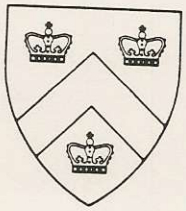
School of Engineering and Applied Science

Columbia University

1986 IEEE

Workshop on Charge Coupled Devices

Columbia University's Arden House
Harriman, New York



October 24–26, 1986

Foreword

This workshop is aimed at exploring the directions charge-coupled device (CCD) research has taken in the past few years and where it is headed in the years to come. The all-invited technical program provides for an in-depth look at the recent progress of CCD research in signal processing, imaging, and device technology. The attendance size of the workshop has been limited and program time has been set aside to promote open and fruitful discussion among scientists working in this field.

The location of the workshop was chosen to be Columbia University's Arden House, the former Mansion of the Harriman family, which was given to Columbia in 1950. Located 48 miles north of New York City on a wooded mountain top overlooking Harriman State Park, it is an ideal setting for a topical workshop of this size. Arden House is a self-contained conference center featuring baronial elegance with wood paneled libraries and blazing fireplaces. It has a UN style auditorium, dining rooms, indoor and outdoor recreational facilities, and overnight accomodations. Arden House was reserved exclusively for this weekend workshop.

This workshop was made possible by the sponsorship of the IEEE Electron Devices Society and the Columbia University Center for Telecommunications Research. The assistance of the Columbia University Microelectronics Sciences Laboratories is also gratefully acknowledged.

Eric R. Fossum
Workshop Chairman

Department of Electrical Engineering
Columbia University
New York, New York 10027

October 24, 1986

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WORKSHOP ON CHARGE-COUPLED DEVICES
Harriman, New York

AGENDA

Friday, October 24, 1986

p.m. 3:00- 5:30 Check-in and Registration. Main entrance/library
5:30- 7:00 Reception. East room.
7:00 -8:30 Dinner served. Dining room.

8:30-10:00 CCD "MEMORIES"
Michael Tompsett, AT&T Bell Laboratories

10:00-11:30 Bar is open. East Room

Saturday, October 25, 1986

a.m. 7:30-8:30 Breakfast is served. Dining room.

8:50-10:30 Opening Remarks
Eric Fossum, (Workshop Chairman) Columbia Univ.
RADAR SIGNAL PROCESSING
Alice Chiang, MIT Lincoln Laboratories
HIGH SPEED SILICON CCD'S
Ken Petrosky, Westinghouse
RECURSIVE FILTERING
Thomas Vogelsong, General Electric

10:30-10:45 Coffee Break

10:45-12:45 IR IMAGING
Walter Kosonocky, RCA
UV IMAGING
Jim Janesick, JPL
UV IMAGING
Nelson Saks, NRL
X-RAY IMAGING
George Ricker, MIT

p.m. 12:45-2:00 Lunch is served. Dining room.

2:00-3:30 FOCAL PLANE CONVOLUTION
Paul Beaudet, Westinghouse.
CHARGE-COUPLED COMPUTING
Eric Fossum, Columbia University
NEURAL NETWORKS, IMAGE PROCESSING
Jay Sage, MIT Lincoln Laboratories

3:30-3:45 Coffee Break
3:45-5:30 Afternoon Recess
5:30-6:30 Social Hour. East Room.
Hosted by Ron Perry, Pulse Instruments, Inc.
6:30-7:30 Dinner is served. Dining Room.

AGENDA (cont.)

p.m. 8:30-9:30 DISCUSSION - THE FUTURE OF CCDs:
MORE THAN A PRETTY PICTURE?

9:30-11:30 Bar is open. East Room.

Sunday, October 26, 1986

a.m. 7:30-8:30 Breakfast is served.

8:50-10:30 Announcements
ACOUSTIC CHARGE TRANSFER
Jim Willhite, Gould
ACOUSTIC CHARGE TRANSFER
Michael Hoskins, Electronic Decisions
SPATIAL LIGHT MODULATOR
Barry Burke, MIT Lincoln Laboratories

10:30-10:50 Coffee Break

10:50-12:15 HIGH SPEED GaAs CCD'S
Raj Sahai, Rockwell International
VERY LOW DARK CURRENT
Dan McGrath, Texas Instruments
HIGH RESOLUTION COLOR
Bruce Burkey, Kodak
WAFER-SCALE IMAGING
Morley Blouke, Tektronix
Closing Remarks
Eric Fossum (Workshop Chairman), Columbia Univ.

p.m. 12:30-1:30 Lunch served. East Room.
1:30-2:00 Checkout and departure.

A CCD Matrix-Matrix Product Radar Processor

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A CCD matrix-matrix product device (MMP) which is capable of performing the functions of high-speed sampling, input and output buffering, data transposition, weighting and Doppler filtering for a pulse Doppler radar is described here. The MMP device under consideration is based on the recent development of a parallel processing architecture for CCDs and a high-speed, low-power CCD multiplying D/A converter (MDAC). Using this processor, it is possible to perform about one billion real arithmetic operations per second. Such capability should result in a smaller, lower power and higher throughput signal processor than would otherwise be obtainable.

Two versions of MMP devices have been fabricated. The MMP-A device includes a 32-stage CCD tapped delay line, 32 CCD MDACs, 32 × 32 accumulators (arranged in groups of 32), 32 × 32 sample buffer, and a parallel-in-serial out (PISO) output shift register. The tapped delay line performs the function of a sample-and-hold, converting the continuous-time analog input signal to a sampled analog signal. The MDACs share a common 8-bit digital input which is represented in 2's complement notation, the output of each MDAC goes to a corresponding accumulator(ACC). At each stage of delay, the sample data is coupled to a corresponding MDAC/ACC processor for multiply-add operations and all of the input samples are processed in parallel. The PISO CCD is used to reformat the output data stream. The device is fabricated using a double poly, double metal buried channel CCD process. The MMP-A can be used to process returns of a burst waveform with as many as 32 range samples collected for each pulse in the burst. The MMP-B can handle only 16 range samples in parallel.

Using this device as a pulsed-Doppler radar processor, the computational Doppler resolution and the number of pulses processed by the device are fully programmable. Processing simulated video from 42 coherent pulses with a frequency resolution of $2\pi/420$ has been demonstrated. A strong target and weak targets with an amplitude 30 dB below the strong one have been simultaneously resolved by the processor, which indicates that the device has about 40 db dynamic range. The experimental evaluation reported here was done at an input sampling rate and internal computation rate of 5 MHz. Additional high speed testing is planned to determine the upper limit on processing throughput.

HIGH SPEED SILICON CCDs

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The peristaltic CCD was devised by Esser to facilitate high speed charge transfer. The PCCD is a device structure which by design utilizes the electric fringe field between adjacent gates to move the last fraction of charge being transferred. This is achieved by the design of the gate length and the thickness of the N-channel. It is known that the maximum fringe field between two adjacent planar gates at different potentials on top of a depleted semiconductor occurs at a depth approximately equal to half the gate length. Consequently, to achieve high transfer efficiency the last fraction of charge to be transferred within the channel must by physically positioned at this depth. This positioning is determined by the thickness of the N-region in an N-channel device and is about half of the N-region thickness. Therefore, a CCD designed for high speed transfer which has a 3.5 micrometer gate length requires a 3 to 4 micrometer N body. This reason gives rise to the sometimes used description of peristaltic CCDs as a deep buried channel device. Typical buried channel devices designed principally to avoid surface state trapping have N - P junctions on the order of 0.1 to 0.3 micrometers.

Westinghouse has been examining the use of peristaltic CCDs for use in radar systems for a number of years. Their use as a transient recorder or analog buffer is very attractive for capturing a wideband signal for subsequent A/D conversion in a high resolution converter, and processing at more conventional speeds with established hardware.

There is a general reluctance to use PCCDs at high speeds due to a few minor operating difficulties. The relatively high electrode capacitance make driving the devices difficult. A fixed pattern noise due to non-uniformities along the CCD are made extremely noticeable by the fast/slow operation which caused each packets of charge to reside in the CCD for a different time increment. The coupling of logic transitions which produces the clock waveforms also appears as fixed pattern noise. Transfer inefficiency also has a major impact on the signal processing.

Different circuit techniques have been implemented which address these problems. ECL to 8v clock drivers have been designed which can handle both the fast/slow transients and the high capacitance loads at greater than 200MHz. Devices have been designed and fabricated that have operated over 500MHz (80 stages), and 200MHz dual channel devices for use in complex I, Q processing have been fully characterized.

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CHARGE-DOMAIN INTERGRATED CIRCUITS

FOR SIGNAL PROCESSING

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A new class of integrated circuits, called charge-domian devices, has been developed for performing enhanced monolithic signal processing. All signal-processing operations are accomplished by splitting, routing and combining charge packets, thus overcoming many of the limitations of alternative devices, such as charge-coupled device (CCD) split-electrode transversal filters, and switched capacitor filters. Charge manipulation techniques are described, which allow poles as well as zeroes of a transfer function to be implemented efficiently, leading to infinite impulse response monolithic filters suitable for high-frequency applications.

Several test filters, including a narrow-band bypass filter, have been demonstrated. The 8-pole bandpass filter exhibits a passband width of 1 percent of the clock frequency and over 70-dB stopband attenuation on a chip only 2.0 X 2.7 mm in size. Since only charge-coupled device delay-line-type operations are used, the device clock rate is only limited by the inherent charge transfer inefficiency. Clocking speeds of up to 15 MHz have been demonstrated using surface channel devices. These charge-domain devices are useful in applications ranging from radio IF to video signal processing with a high level of integration achievable on a single charge-domain integrated circuit.

"Schottky-Barrier IR-CCD Imagers"

by

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Schottky-barrier focal plane arrays are the only infrared imagers that are fabricated by the well established silicon VLSI process. Therefore, at the present time they represent the most mature technology for large-area high-density focal plane arrays for many SWIR (1 to 3 μm) and MWIR (3 to 5 μm) applications. PtSi Schottky-barrier detectors (SBDs) were developed for operation in the MWIR band at a temperature of 77 to 80K. These SBDs can be designed for operation at 77K with a dark current density in the range of 1.0 to 20 nA/cm^2. Pd_2Si SBDs were developed for operation with passive cooling at 120K in the SWIR band. Although the PtSi SBDs have rather low quantum efficiency (0.5 to 1.0% at 4.0 μm), however, because of very low readout noise, the IR-CCD imagers with PtSi SBDs are capable of 300K thermal imaging with a noise equivalent (NEΔT) of less than 0.05K. The noise floor of the SBD arrays is limited by the SBD dark current shot noise.

With the support of RADC, Hanscom AFB, MA, RCA Laboratories developed a 160 x 244-element PtSi Schottky-barrier IR-CCD imager with 80 (H) x 40 (V)-μm^2 pixels and 39% fill factor for operation at 30 frames/s with standard TV field interlace.[1] Excellent quality thermal imaging and NEΔT of less than 0.1K were demonstrated with this staring imager for operation at 30 frames/s, with f/2.3 optics, and with an additive type (one point) pixel corrector which averages 16 reference frames to produce the correction video signal.

A brief review of the progress in the development of Schottky-barrier focal plane arrays will be complemented by a video tape demonstration of the performance of the 160 x 244 IR-CCD imager.

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1. W. F. Kosonocky, F. V. Shallcross, T. S. Villani, and J. V. Groppe, "160 x 244 Element PtSi Schottky-Barrier IR-CCD Image Sensor," IEEE Transactions on Electron Devices, Vol. ED-32, No. 8, August, 1985, pp. 1564-1573.

UV IMAGING

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Pasadena, California 91109

Until recently, the usefulness of the charge-coupled device (CCD) as an imaging sensor was thought to be restricted to rather narrow boundaries of the visible and near IR spectrum. However, since the discovery of backside charging and the CCD flashgate, the full potential of CCD performance is now realized. Indeed, these techniques not only allow the CCD to be used directly in the UV, EUV, and soft x-ray regimes, but they have opened up new opportunities in optimizing charge collection processes as well. In this paper, we discuss in detail the technique of backside charging and flash gate, describing its properties, use, and future potential as it applies to the backside-illuminated CCD.

"Radiation-hardened MNOS CCD technology for
hybrid infrared focal plane arrays",
Nelson Saks (NRL) and David Seib (Rockwell Int.)

Silicon MOS CCDs are often used as multiplexers in hybrid infrared (IR) focal plane arrays. In the hybrid configuration, the CCD is bonded to an array of IR-sensing diodes and must operate at cryogenic temperatures (10-150 K). However, MOS radiation effects are much worse at low temperatures compared to room temperature and, consequently, CCD failure by ionizing radiation occurs at relatively low total exposures (typically about 10^4 rad). In addition, the problem is made worse because conventional MOS hardening approaches are ineffective at cryogenic temperatures. We describe a fabrication technology which utilizes a metal-nitride-oxide-semiconductor (MNOS) gate insulator for hardened cryogenic CCDs. Hardened MNOS CCD multiplexers are shown to survive 1 Mrad total dose.

"CCD's for UV Imaging"
N.S. Saks, J.T.Bosiers*, D. McCarthy, M.C.Peckerar, and D.J.Michels
NRL and *Sachs-Freeman Associates

This paper describes the development of backside illuminated, deep-depletion CCD's optimized for imaging in the ultraviolet (UV). 32 x 32 CCD area imagers have been fabricated at NRL using the "deep-depletion" approach. Fabricated CCDs have reasonable characteristics with high transfer efficiency but poor (high) dark currents (30-100 nA/cm^2). A quantum efficiency of 20% at 1216A was obtained on the best devices by appropirate treatment of the CCD backside, namely, implantation of a backside P+ layer and controlled etch back of the layer. A model is presented to describe the UV detection process at the CCD backside and factors controlling the UV quantum efficiency. Data showing resolution achieved in the UV will also be presented.

X-RAY IMAGING WITH CHARGE-COUPLED DEVICES

George R. Ricker

MIT Department of Physics
and
Center for Space Research

Silicon charged-coupled devices as imagers for X-rays with energies in the range 0.1 keV < E_x < 10 keV will be discussed. Such imagers have the important property of providing *both energy resolution* ($E_x / \Delta E_x$ ~ 50 for E_x ~ 5 keV) and *spatial location* (nearest pixel ~ 20μm) for *single detected photons*. Using a low-dark current device such as the Texas Instruments TI4849 virtual-phase CCD (i_D ~ 10 pA/cm^2), an X-ray CCD camera can operate with modest cooling (T ~ -30° C) and still achieve spectroscopic performance comparable to that achieved with an LN_2-cooled state-of-the-art Si (Li) diode detector. The photon quantum efficiency of current CCD X-ray detectors exceeds 90% near 3 keV. Presently, research efforts are directed toward:

- Reduced readout noise, with a goal of ~3 e^- rms (presently achieved: ~7 e^- rms).
- Improved low energy X-ray response, through the use of thinner gate structures in frontside-illuminated devices, or through backside control gates in backside-illuminated devices.
- Increased high energy quantum efficiency, through the use of high resistivity silicon.
- Area increase through device mosaicing, which will also permit conformance to the curved focal plane of typical X-ray optical systems.

X-ray CCD sensors have a wide range of possible applications. In particular, their use as an astronomical sensor for the NASA Advanced X-ray Astrophysics Facility (AXAF), a large space telescope to be launched during the mid 1990's, will be discussed.

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FOCAL PLANE CONVOLUTION

ABSTRACT

A two-dimensional convolution is a linear combination of neighboring picture elements (pixels). The array of coefficients of the convolution is called the Kernel, and may have positive or negative elements. Convolutions are useful signatures for pattern recognition and for image enhancement. Some convolutions are elements of vectors and tensors from which rotationally invariant scalar signatures can be contracted.

Time multiplexing and space multiplexing Focal Plane Convolvers will be introduced. In these devices charge packets from pixel sites on the focal plane are multiplexed and sampled to produce an array of output signals corresponding to convolutions of arbitrary Kernels. The differences between time multiplexing and space multiplexing techniques will be discussed in the context of a simple edge extraction operator whose Kernel is

$$\begin{bmatrix} -1 & -1 \\ +1 & +1 \end{bmatrix}$$

Other CCD devices which complement this technology will be discussed. They include:

- Squaring Circuits
- Charge Replication Circuits
- Equal Variance Mapping
- Triangular Gate Technology

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CHARGE-COUPLED COMPUTING

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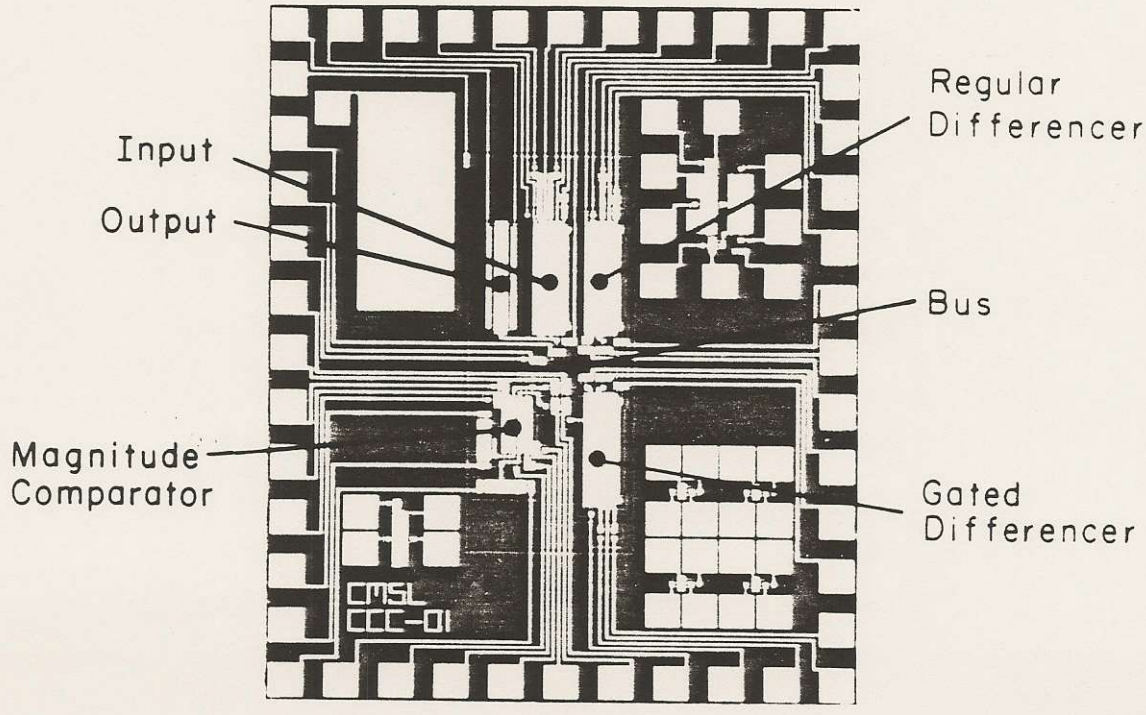
Real-time machine vision for mobile robots requires approximately 100-500 operations per pixel frame. For modestly sized focal plane array imagers, this could require in excess of 50 million operations per second. Spatially parallel image pre-processing on the focal plane may be one way to achieve such throughput without excessive power or weight cost.

We have been investigating the use of charge-coupled device circuits for forming a simple, general purpose pixel preprocessor suitable for application on the focal plane. The first such charge-coupled computer we have fabricated and tested is shown below. A 10 μm design rule, aluminum gate, diffused junction, open-gap process was used. The computer has a diffused central bus linking I/O circuits, a charge-packet differencer, a charge-packet magnitude comparator, and a second differencer which is gated by the comparator. The circuits are functional and operate well at clocking frequencies exceeding 2 MHz. The operation of each of these circuits is described in the presentation.



UNCONVENTIONAL APPLICATIONS OF CHARGE COUPLING: IMAGE PROCESSING AND NEURAL NETWORKS

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ABSTRACT

Charge-coupled devices have been investigated extensively for applications in three primary areas: memory, signal processing, and imaging. In those applications the charge-coupled device (CCD) stores information or signals in the form of charge packets and moves that information from place to place using charge-coupling techniques. A common feature in the operation of CCDs in these applications is careful maintenance of the integrity and individuality of each charge packet. In this talk I will describe two application areas in which (1) charge coupling is used not only to move information from one well to another but to perform some information processing operations and (2) the identity of individual charge packets is not maintained.

The first area is image processing. Here the CCD not only serves as the light detecting device but also performs some operation on or analysis of the image. We have been investigating three such applications: Gaussian convolution for edge detection, intensity histogram analysis, and image-image correlation. In this talk I will describe only the Gaussian image convolver.

Gaussian convolution is the computationally intensive step in the difference-of-Gaussians edge-detection algorithm used in machine vision systems. Our CCD directly generates images convolved with any of a wide range of Gaussian kernel functions. The Gaussian convolution is produced using an unconventional clocking sequence in which neighboring charge packets are deliberately mixed together in a controlled way. We will describe how this technique is implemented for one- and two-dimensional images and will show results obtained using a standard, commercially available CCD imaging chip.

The second application area is artificial neural networks, parallel computing systems modelled after the structure of the brain. These networks comprise a large number of relatively simple computational elements (neurons) with connections (synapses) to many or all other elements. The information content of the system is embodied in the pattern of synaptic interconnection weights, and information processing results from the collective response of the coupled system. We will describe an artificial neural-network integrated circuit that learns patterns and recalls them associatively. The synapses in the circuit use metal-nitride-oxide-semiconductor (MNOS) analog nonvolatile memory elements to store the weighting coefficients. Charge-coupling techniques are used both for coupling the neurons during readout and for controlling the state of the MNOS elements during learning.

ACOUSTIC CHARGE TRANSPORT DEVICES

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The incorporation of Acoustic Charge Transport (ACT) devices into signal processing systems promises great savings in cost, weight, and size as well as increased functional performance and reliability in both military and commercial systems. GRC has been working for the last year to develop the ACT technology using GaAs for use in signal processing systems.

The ACT device is a device which is fabricated on a weakly piezoelectric semiconductor with a long channel region into which charge can be injected and in which the charge is transported by an acoustic wave and in which the charge may be detected.

The ACT is superficially similar to SAW devices fabricated on semiconductors. In an ACT device, the SAW merely serves as a charge transport mechanism, as long as the amplitude of the SAW generated electric field is sufficient to trap the charge carriers. Attenuation of the SAW does not affect the signal.

In terms of its operation an ACT device can be compared to a CCD with a fixed clock rate. The electric fields confining the signal charge in an ACT are similar in function to the gates of a CCD. However the ACT structure is simpler than that of a CCD since there is no requirement for a complex charge-transfer structure with a multitude of gates, well defined gaps, and electrical crossovers. The dynamic range and the noise figure for a single-tapped ACT device have been estimated as 68dB and +4.5dB, respectively, and the dynamic range increases as ten times the log of the number of taps. Thus the potential accuracy of ACT devices is orders-of-magnitude better than SAW devices and may be as high as digital processors which work at much lower effective computational rates.

Gould Research Center, United Technologies, and EDI are presently working on advancing the state of ACT technology. The state-of-the-art of ACT is primitive at best. Only the most rudimentary signal processing functions have been implemented with ACT's. This is partly due to the fact that the device is so new and partly due to the fact that the device came from the device physics community rather than the systems community. It is expected that the systems community will have great interest in the device as applications become more evident. One of the most powerful applications is its use as a tapped analog delay line. Since the ACT is a sampled analog device, it can combine the flexibility of digital filters with the analog capabilities of continuous filters. They can perform many of the functions of digital filters with digitizing the signal. The promise of high speed GaAs, analog and digital circuits integrated with ACT's is an exciting prospect.

A test chip containing nine different ACT devices has been designed and devices have been fabricated on GaAs. The initial test chip has devices aimed specifically at providing information on the use of ACT structures in signal processing areas such as optical detection, chirp-z transformations, waveform shaping, electri-cally programmable transversal filters and analog-to-digital conversion. Certain ancillary FET processing devices such as source follower amplifiers, analog compar- ators, and power FET's have been included on this chip set.

Devices with sampling rates as high as 700MHz have been fabricated. The materials for these devices are grown by Molecular Beam Epitaxy (MBE) technique at GRC. Additional materials processing and electrical characterization is done at GRC. The fabrication of these devices, the device performance, and possible device application area will be discussed.

Recent Developments in Acoustic Charge Transport Devices

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An overview of the operational performance presently obtained from acoustic charge transport (ACT) device technology is presented. The ACT device is a high speed GaAs charge transfer device in which electron transport is accomplished using the traveling wave electric field of a surface acoustic wave (SAW). The inherently smooth and continuous nature of traveling wave transport results in very high transfer efficiency, large signal bandwidths, low noise, and interference-free charge detection.

Theoretical and experimental investigations of the basic charge injection, transport, and detection characteristics of the ACT device are presented. It is shown that the theoretical models are in good agreement with experimental results for charge capacity, charge injection current-voltage characteristics, and non-destructive charge sensing transfer functions. Experimental charge injection studies demonstrate the high speed automatic signal sampling capabilities of the ACT device.

The operational performance obtained from recent architecture ACT delay lines, transversal filters, and wide bandwidth correlators is presented. Transfer efficiencies in excess of 0.99994 have been measured in ACT delay lines with 375 equivalent transfers at 360 MHz effective clock frequency. The low noise and large blocking dynamic range performance of ACT transversal filters is illustrated. It is shown that the ACT device is an attractive vehicle for implementing a variety of transversal filter and correlator functions.

Spatial Light Modulators Based on Charge-Coupled Device Technology

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Abstract

A critical need exists in the areas of optical computing and optical signal processing for a two-dimensional spatial light modulator which can be programmed electrically at high frame rates. One approach to realizing such a device is to use the phenomenon of electroabsorption, which is the variation of optical absorption with electric field, in conjunction with a device such as a CCD whose internal electric fields are programmable. An electroabsorption effect has recently been discovered in GaAs/AlGaAs multiple quantum wells (MQWs) which has the requisite speed and is sufficiently strong to yield satisfactory contrast ratios [1]. We have been developing technology for integrating MQW modulators with Schottky-barrier CCDs for a monolithic, high-speed spatial light modulator.

The major portion of our effort has been the development of CCD technology for GaAs and AlGaAs. One area of concern is the gate structure, which has usually been fabricated in a single metal level with lithographically defined gaps between gates. The gap dimensions must be controlled to sub-micrometer tolerances, making this structure difficult for routine fabrication. To alleviate this problem we have developed an overlapping-gate structure which can be fabricated with low temperature processing [2]. As in the case of the polysilicon overlapping-gate process commonly employed in silicon CCDs, the interelectrode gaps are determined by the thickness of an insulating layer rather than by lithographic processes.

Another point of concern in these materials is the much greater concentrations (in comparison to silicon) of deep levels and the accompanying charge transfer inefficiency. To minimize trap-related charge loss we have applied the same quantum well configuration to the CCD channel. In this quantum-well CCD (QWCCD) the charge is confined to a thin (10-20 nm) GaAs layer sandwiched between AlGaAs layers. Results on our initial version of this device show greatly reduced trapping effects [3]. Additional work is in progress to optimize this structure for use with the MQW modulator.

References:

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IEEE CCD Workshop

HIGH SPEED GaAs CCDs, Rajeshwar Sahai, Rockwell International Science Center, Thousand Oaks, CA 91360

October, 1986

ABSTRACT

Recent improvements in the design of GaAs CCDs have enabled its high speed capability to be used for systems applications. We have demonstrated GaAs CCD operation at clock rates exceeding 4 Ghz, with the useful practical range extending to 2 GHz. The large dynamic range and high speed have led to our investigating a programmable transversal filter and integrated CCD multiplexer for high speed readout of detector arrays. Very short sampling time capability also opens up new applications for microwave analog signal processing. In addition, we feel that GaAs CCDs can also contribute to the emerging area of optical computing by providing means to handle 2-D optical signals with reasonably high speeds.

Our work in the above areas will be presented. A programmable transversal filter chip has been built and tested. This chip requires integrating the GaAs CCDs with MESFET ICs to provide on-chip pulse generators, balanced amplifier, programming switches and track and hold circuits. This chip, when clocked at 1 GHz, can filter signals up to 500 MHz. The short sampling time of GaAs CCDs permits direct handling of microwave signals and filtering of the down-converted signal in the baseband on the same chip.

A detector array/CCD multiplexer chip has been developed which consists of 32 GaAs detectors coupled to the CCD multiplexer through individual circuits to carry out photocurrent integration, range compression and reset functions. A dynamic range of 47 dB was measured on these devices for optical input to the detector array. A noise equivalent power level corresponding to only 65 photons was measured. Our other activities in optical signal processing include a recent program to develop a two-dimensional spatial light modulator. Optical modulation is to be provided by absorption cells based on an enhanced electroabsorption effect in GaAs-GaAlAs multiple quantum well layers. The analog signal for modulation will be sampled by GaAs CCDs and will be used to address the individual absorption cells.

VERY-LOW DARK CURRENT CHARGE COUPLED DEVICES

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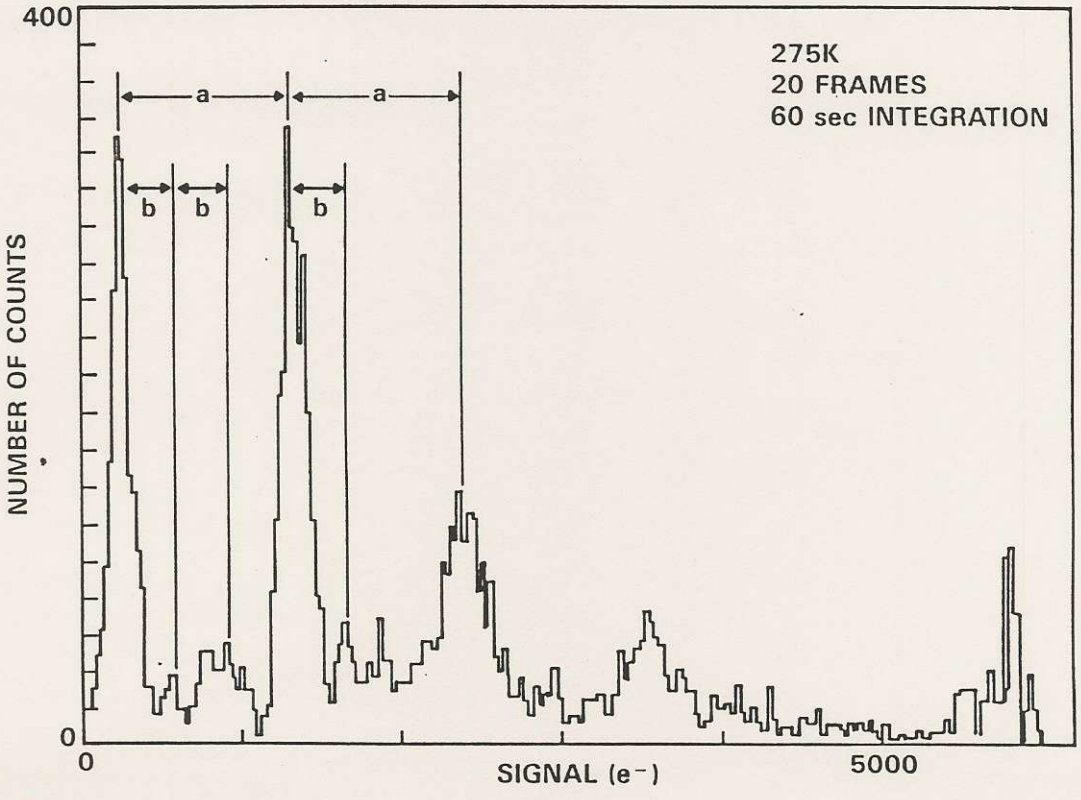
The low level response in a charge coupled device is limited by charge generation at the silicon-silicon dioxide interface and in the bulk silicon. This charge is produced predominately by traps located near the center of the silicon bandgap. In typical multiphase charge coupled devices this process is dominated by the high density of defect sites intrinsic to the interface and is of the order of $5nA/cm^2$. In virtual phase charge coupled devices it is possible to shield the photosite from interface charge generation so that only silicon defects in the bulk contribute charge and the dark current drops by greater than two orders of magnitude.

An analysis of the dark current generation model shows that the low values from the bulk can be accounted for by the presence of only a few defects per pixel. This conclusion is supported by histograms of the dark current which show a quantized structure (Fig. 1). It appears that two types of defects dominate with densities of 1.3×10^9 cm^{-3} and 1.5×10^8 cm^{-3}. The temperature dependence of the peak separation is that expected for dark current. Effective cross-sections for the traps can be calculated and used to speculate on the nature of the trap.

*Present address Polaroid Corporation, 21 Osborn St., Cambridge, MA 02139



High Resolution Electronic Imaging

Bruce Burkey

Electronics Research Laboratory
Photographic Products Group
Eastman Kodak Company

Abstract

The resolution capability of solid state sensors is continually increasing. That resolution increase is being driven by demanding industrial, scientific, and consumer video applications. Two such high resolution sensors are described in this paper.

The first is a 360,000 pixel color-image sensor for imaging photographic negatives. This charge-coupled image sensor consists of a 740 (H) X 242 (V) X 2 image area and dual horizontal output registers. The architecture, spectral response, charge capacity, noise, and image quality of the sensor are discussed. The sensor achieves a charge capacity of 10^6 electrons per pixel and a noise of 200 rms electrons per pixel, for a dynamic range of 70 db. Color capability is obtained by an integral organic color filter array fabricated on the sensor.

The second is an advanced full frame CCD sensor for camera applications. This sensor has 1.4 million picture elements, nearly 6 times as many pixels as other sensors used in today's most advanced video cameras. The individual picture elements in this sensor are 6.8 μm square. This small pixel format provides much higher density than currently avaivable devices. The active image area of the sensor consists of 1320 (H) X 1035 (V) columns and rows, respectively, without interlace, and measures 9 mm X 7 mm, making it compatible with a 2/3" optical format. A single register is used for horizontal readout. The overall chip size is 10 mm X 8.3 mm. Higher resolution sensors such as the one disucssed here are pointing in the direction of electronic photography.

WAFER SCALE CCD's

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Charge-coupled device imagers designed specifically for scientific applications have achieved very high levels of performance, allowing investigation of very low signals over a broad spectral range. Although imagers available for the standard video market perform their tasks very well, the demands of format, frequency, and size force compromises in some of the more important criteria of interest in scientific investigations.

For scientific images, the important criteria are low readout voice, large well capacity, high CTE, MTF, and CCE, low dark current, high quantum efficiency, and wide spectral response. Using a three phase technology, Tektronix has designed two CCD sensors specifically for scientific imaging. These devices have 512 X 512 and 2048 X 2038 pixel formats; the latter device occupies an entire 100 mm wafer. This paper will concentrate on a description of these devices and their performance. Of interest are recent measurements of quantum efficiencies (> 40 percent at 350 nm and > 70 percent at 700 nm) and very low dark current ($<\sim$ 60 pA/cm^2 at room temperature).

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