A CIRCULATING MULTILEVEL CHARGE TRANSFER DEVICE MEMORY WITH ADAPTIVE REFRESHER

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ABSTRACT

An adaptive refresher for a charge transfer device with multilevel storage is described.
The transfer of reference charge samples together with the signal charge samples through a CTD gives the opportunity of cancelling out errors made by the CTD and its interface. This makes it possible to store more bits per cell. To show the operation of the adaptive refresher, a circulating memory has been made on a printed circuit board, using a BBD containing 256 storage cells, Each cell has 32 quantization levels, giving a total storage of 1.28 Kbit.

I. INTRODUCTION

When a CTD is used as a memory, the samples in the CTD have to be periodically refreshed, because of the errors introduced by the CTD. Currently available CTD memories use one bit storage per cell, so a sample is a logic one or a logic zero. At the output of the CTD, the samples are compared with a reference sample midway between "0" and "1" and refreshed. The reference sample is usually transported through a dummy register, to give it about the same deviations as the signal samples that pass through the memory. In this way only the reference level is corrected.

Multilevel storage is far more critical to errors. With no correction the number of quantization steps is very low, because it is determined by all the errors: one quantization step must be more than two times larger than the worst case total error in the circuit. With the above mentioned correction, only the reference halfway between "0" and "1" is corrected. A complete gain and offset correction can be made by sending all the references needed, so 2^n1 for n bit storage per cell, through dummy registers, but this takes more circuitry and chip area.

Another solution is to send only a maximum and a minimum sample, defining the amplitude range of the CTD, through dummy registers. The values of these samples before and after passing the CTD give all the information needed to make all the reference levels required. In this way, all the gain and the offset errors are corrected.

Instead of sending the references through dummy registers, it is also possible to send them through the same CTD as the signal samples pass. This dispenses with the need for extra dummy CTD's and the errors corrected are precisely the errors added to the signal samples. All the errors made by the interface circuits and which are common to both references and signal samples, are corrected for. This principle is tried out with a single 256-cell loop on a printed circuit board. The CTD used here is a normal BBD line with relatively large d.c. shift and gain errors, to show the insensitivity of the adaptive refresher to these errors.

II. DESIGN CONSIDERATIONS

Errors introduced by the CTD

The CTD used is the TDA 1022, a 256-cell BBD line with tetrode struc-

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ture, made by Philips. The charge transfer inefficiency is 1.5×10^{-5} per transfer; this gives about 0.8 % for $n \times \varepsilon$. Without bias the traps give an error of 0.4 %, but with sufficient bias the effect of traps is negligible. The non-linearity of the BBD is less than 0.3 %. Capacitive coupling and clock load give an error of less then 0.4 %. The d.c. relationship between input and output of the BBD is given in figs. 1 and 2 for clock frequencies of 3 kHz and 250 kHz. The frequency dependence is due to leakage currents. This can also be seen in figs. 3 and 4, which show the frequency behaviour with the same data. The slope at low temperatures is due to temperature-dependent thresholds at the input and output of the BBD.

Multilevel storage loop

By feeding the output of the BBD via a refresher back to the input, we have a continuous memory. When the refresher is a quantizer (i.e. a comparator for one level storage), the error made by the BBD between two refresh operations must be smaller than half of the quantization step. Only then can the signal packets be refreshed to their original values. Suppose we have only a d.c. shift error. At T = 30°C this is 3.75 V (see fig. 1). This means that the quantization step would be larger than 7.5 V. As the signal swing is about 6 V, such a memory cannot even store one bit per cell.

We get a better memory when we correct for the reference value midway between the maximum and minimum signal samples, as is normally done. For instance, when 8 V is the corrected reference voltage, we see from fig. 1 that at 30°C the input voltages of 5, 8 and 11 V become respectively 6, 8 and 10 V at the output. This means that two bit storage per cell is already critical and even impossible at 70°C.

But the refresher can be more than only a quantizer; it can also correct e.g. the d.c. level and the voltage gain (the largest errors in this BBD) by means of a level shifter and an amplifier if we know the magnitude of these errors of the specific BBD that is used. Looking at fig. 3, however, we see that the d.c. drift over 60°C is still 1.2 V. This means a minimum quantization step of 2.4 V, so that only two or three levels are possible.

With a correction as given in fig. 5 the d.c. component is decoupled. Supposing that the gain is accurate enough, the remaining error, viz. the temperature dependence of the gain, being 3 % over 60°C, would limit the maximum number of levels to 16. But several points make this circuit less suitable. The gain is not exactly known. The d.c. component of the stored part of the input is not necessarily the same as that of the complete input signal. Because of the long time constant, the loop needs time to adjust to a new input signal before it can read in. And finally, errors made during storage of one sample give a d.c. error for all other samples.

Another possibility for correction is to compensate for the temperature-dependent gain of the output source-follower, but, as the temperature dependence of the input stage and th e leakage currents are still not compensated for, this will only work at higher clock frequencies.

Instead of correcting the signal samples before quantization, it is also possible to correct the references of the quantizer. Using this principle for multilevel storage means dummy delay lines for all the references. Another solution is to send only the maximum and minimum values through dummy registers. As the voltages of these references are known before and after passing the BBD's, the refresher can make the right corrections for the signal, assuming that the BBD's are linear enough. An exact correction is made when the two references are sent as single samples through the same BBD as the signal samples, in time multiplex. A circuit operating on this principle is shown in fig. 6.

By sending the two references periodically, once per loop cycle, the refresher is periodically adjusted, so that temperature and other time-dependent errors are also corrected. Such a circuit is also independent of the specific errors of the BBD used: it automatically adjusts itself to each BBD that is inserted in the loop. Moreover, when the clock frequency is changed, the refresher will also correct for the changing leakage.

The maximum number of quantization errors is now determined by the sum of the errors not corrected. This sum is in the worst case: 0.8 + 0.4 + 0.3 = 1.5 %. This means 3 % for one quantization step, so that maximally 32 levels (5 bits) are possible. Since, owing to and parasitic capacitive coupling, the absolute errors are dependent on the difference between two successive charge packets in the BBD, we can reduce these errors by preventing large jumps in the input signal. That is to say: the slew rate of the input signal has to be limited. For example, if the difference between two successive samples is limited to $\frac{1}{4}$ of full scale, we get a maximum total error of $\frac{1}{4}$ ($\frac{3}{4}$.8 + 0.4) + 0.3 = 0.6 %, which gives the possibility of 64 levels (6 bits). Of course the margin is now so tight that in most cases 5 bits should still be taken. Photo 1 gives an example of a signal stored in the loop with 64 levels per sample.

It is also possible to use a detection that overcomes the problems with charge transfer inefficiency. Such a detection scheme is proposed by Thornber[6].

III. IMPLEMENTATION OF THE CIRCUIT

Block diagram

Fig. 7 shows a block diagram of the loop, with the adaptive refresher, composed of an analog switch, sample- and-holds, AD converter, digital switch and DA converter. Sample-and-holds 1 and 3 pick up the references V'ref 1 and V'ref 2, respectively, from the BBD output and hold them at the respective inputs "reference" and "analog ground" of the ADC till the new references arrive after one circulation. Sample-and-hold 2 is needed to hold the signal during the A to D conversion.

The reference pulses are made by the digital switch. On a command from f_6 (one in each circulation) the output of the switch gives only ones to the DAC, so that V ref 1 appears at its output. Similarly f_5 forces the output of the switch to all zeros, so that V ref 2 is produced. During the rest of the circulation time the DAC is connected to the ADC.

The ADC gives a binary code-word, which is a quantized representation of the position of V'in between V'ref 1 and V'ref 2 (see fig. 8) and not a representation of the absolute value of V'in. This code word is converted by the DAC in an analog voltage V'in, which has the same position, but now in respect of V ref 1 and V ref 2 instead of V'ref 1 and V'ref 2. An equal offset or an equal attenuation of V'in, V'ref 1 and V'ref 2 has no influence on the binary word. So when V in, V ref 1 and V ref 2 are transferred through the BBD, they will appear changed at the output of the BBD due to attenuation, offset and other errors, but after refreshing, V_{in} has again its original value. The quantizing is for the correction of the "other errors". $V_{ref\ 1}$ and $V_{ref\ 2}$ are again generated by means of the switch. As we use a digital switch before the DA conversion instead of an analog switch after it (figs. 6 and 7), the errors made by the DAC are now the same for signal and references, so that these errors are also automatically corrected by the refresher.

Pipelined loop

By correctly controlling the ADC, DAC input buffer and DAC memory, it is possible to assign two memory cells to the refresher, which brings the total memory capacity to 258 cells and makes the loop faster.

Error in $V_{ref\ 1}$

In this circuit the reference sample $V_{ref\ 1}$ is generated by the DAC, when the digital switch resets all inputs on the DAC to logic "ones". But in essence a DAC cannot generate $V_{ref\ 1}$ at its output when $V_{ref\ 1}$ is also the reference of the DAC itself. The largest output, caused by all logic "ones" at the inputs, is: $(2^{-1} + 2^{-2} + \ldots + 2^{-n})\ V_{ref\ 1} = V_{ref\ 1}\ (1\text{-LSB})$. This error of one LSB can be made smaller by using more bits for generating $V_{ref\ 1}$ than for converting the (digital) signal. An exact reference is made when a DAC is used in which the terminal resistor (or capacitor) of the ladder network (= 1 LSB) can also be switched, so that all the current caused by the reference is used and therefore full scale can be given at the output.

Sample-and-holds

Sample-and-hold 2 must have a fast enough acquisition time because this influences the upper frequency. For sample-and-holds 1 and 3 this is not absolutely necessary, because after a few cycles (before read-in) they only have to follow the deviations in $V'_{ref\ 1}$ and $V'_{ref\ 2}$. For these sample-and-holds the droop rate is more important, because they have to hold during a whole circulation period. The droop rate can thus influence the lower frequency of the loop. By choosing larger capacitors for these sample-and-holds we can keep the droop rate low and moreover we average out the disturbances. The sample-and-holds must not be made too slow, because they have to track the changes in $V_{ref\ 1}$ and $V_{ref\ 2}$ due to drift etc.

Analog switch

The analog switch, which controls the read-in/memory function, is not placed directly after the BBD, but in front of sample-and-hold 2, because the loop has to be kept closed for the references.

IV. EXAMPLES

As mentioned before, 64 levels are only possible with a BBD if the difference between two successive samples is limited. Photo 1 gives an example that satisfies this restrictive condition: it shows the stored and continuously circulated part of a triangular input signal. Each cell contains a charge sample in 6 bits (64 levels). On the left we see the reference pulses. The whole contents of the memory is repeatedly read out, as can be seen at the right of the photo.
Photo 2 shows a stored part of a block signal that does not fulfil the above restrictive condition. We see that at the edges of the block, where the differences between successive samples are too large, the memory loop has made errors. Finally, photo 3 gives an example of "transient recording" with the loop. An external BBD, of which the clock was stopped during a minute, is read out relatively fast ($\emptyset_{clock}$ = 10 kHz), and in the same time stored in the loop. The output of the loop now gives repeatedly the contents of the memory, so that a still picture can be displayed on a normal oscilloscope. The photo shows a picture of the spatial leakage currents in the BBD, which was originally empty.

DISCUSSION

As shown, a circulating memory can be made using a BBD with 256 storage cells and with 32 or even 64 quantization levels per cell, if the adaptive refresher is used. However, the circulating memory that has been

made is not representative of the CTD memories available today. It is just an example to show the operation of the adaptive refresher.
For minimum geometry CTD's the effect of, for example, traps will be larger, and will decrease the maximum number of storage levels. Moreover, the complexity of the refresher increases exponentially with the number of bits per cell, so that three to four bits per cell seems more reasonable than, for instance, six.

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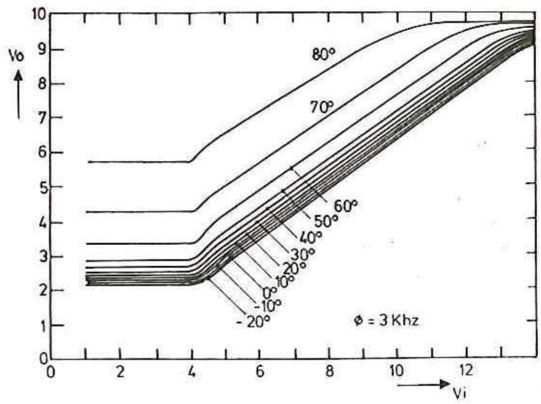

Fig. 1. V_{out} vs. V_{in} for

∅ = 3 kHz

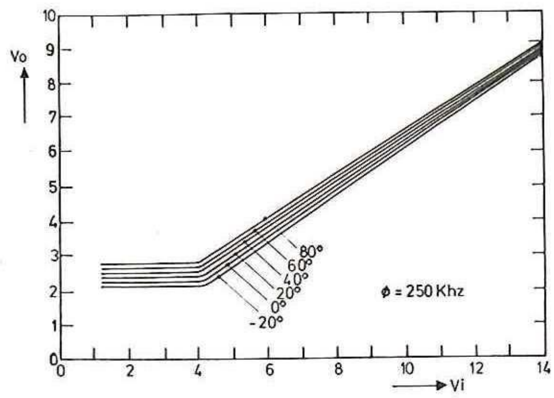

Fig. 2. V_{out} vs. V_{in} for

∅ = 250 kHz

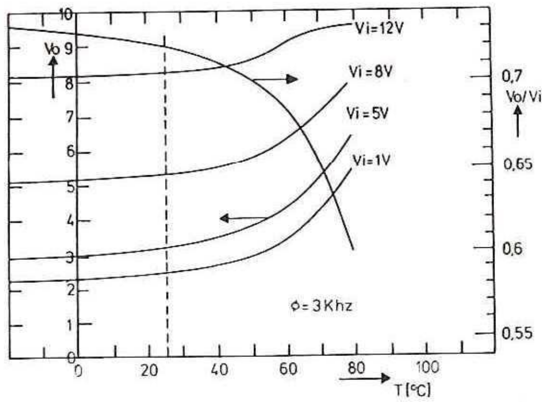

Fig. 3. V_{out}/V_{in} vs. temperature for

∅ = 3 kHz

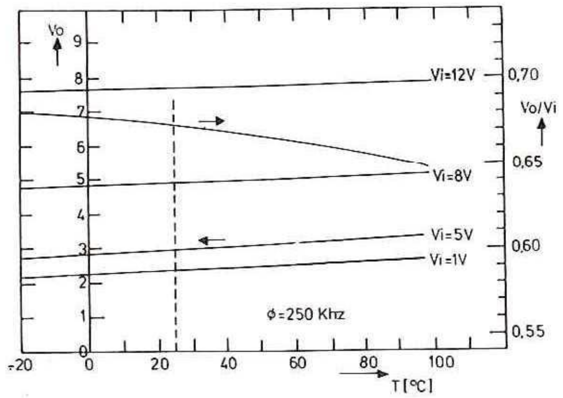

Fig. 4. V_{out}/V_{in} vs. temperature for ∅ = 250 kHz

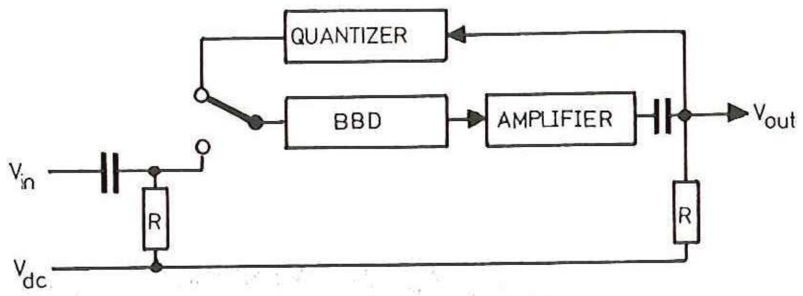

Fig. 5. A.c.-coupled loop

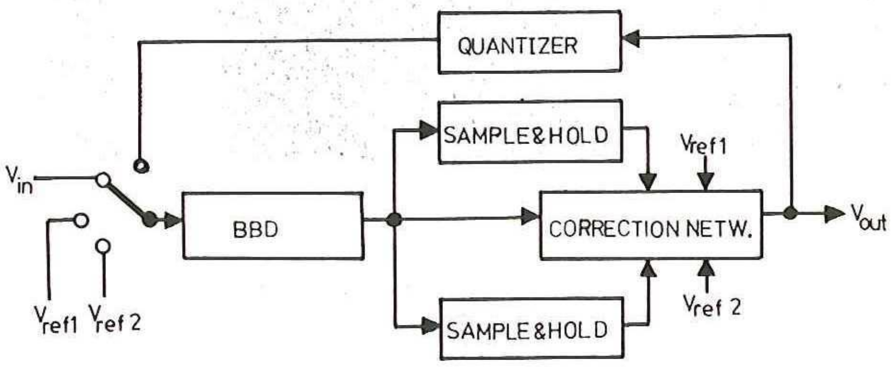

Fig. 6. Loop with adaptive correction network

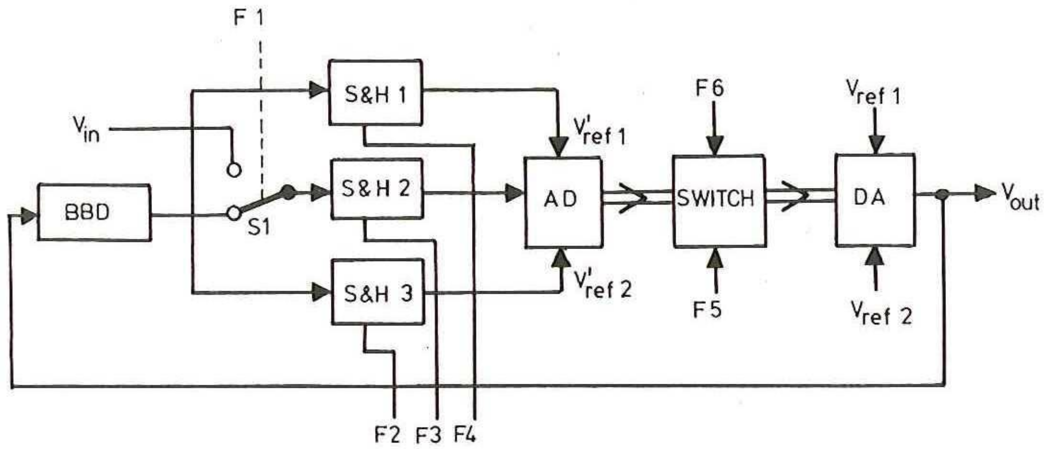

Fig. 7. Implementation of loop with adaptive refresher

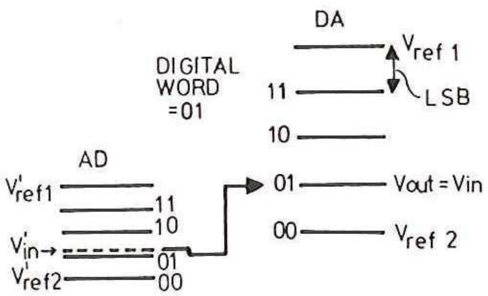

Fig. 8. Voltage correction caused by adaptive refresher

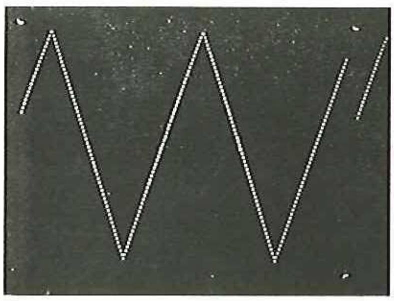

Photo 1. Triangular wave stored with 64 levels per cell.
Hor. 5ms/div.
Vert. 1V/div.

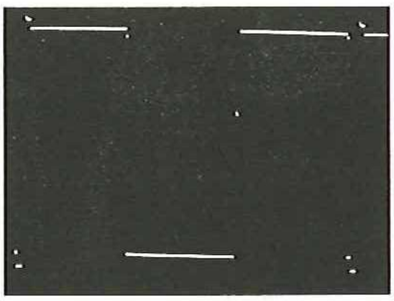

Photo 2. Block wave stored with 64 levels per cell.
Hor. 5ms/div.
Vert. 1V/div.

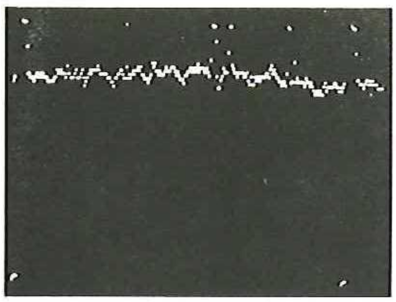

Photo 3. Stored leakage measurement with 64 levels per cell.
Hor. 3ms/div.
Vert. 1V/div.