THE APPLICATION OF CCD'S IN MULTIPLE-VALUED LOGIC

Hans G. Kerkhoff* and Henk Dijkstra*

ABSTRACT

The advantages and disadvantages of using multiple-valued logic in integrated circuits are discussed. The benefits of applying CCD's in the implementation of multiple-valued circuits are explained. The combination of a few basic multiple-valued logic (MVL) functions makes it possible to implement any MVL function. Three basic functions in four-valued logic have been designed, fabricated and tested. These are the minimum, maximum and complement functions. The latter has also the feature that it is able to regenerate the logical value. It is explained why four-valued logic is preferred at this moment. The CCD design principles however can also be applied for multiple-valued logic with other radices. The design considerations and operation principles of the devices are presented, and the performance data given.

INTRODUCTION

Research in the field of binary logic CCD's has been carried out since 1972 [1, 2]. In combination with CCD memories, powerful arithmetic IC's can be realized. A CCD however is an analogue device, and it is therefore possible to employ more than two logical values. Carnes [3] suggested using more than two values in CCD memories, in order to increase the information density. His calculations show that a four-level CCD memory using a 4 μm minimum geometry would occupy in area per bit 3.7 times less than a RAM designed with the same minimum geometry. The successful operation of a four-valued CCD memory has already been reported [4].

It would be an advantage if arithmetic operations could also be performed on the same chip, using the same type of information representation. This paper deals with the design and performance of several basic CCD circuits in four-valued logic. If the complete set of basic functions becomes available, it will be possible to perform MVL arithmetic operations.

MULTIPLE-VALUED LOGIC (MVL) AND CCD'S

Multiple-valued signals can offer several advantages over two-valued signals in IC's. As has already been discussed above, a significantly higher information density can be achieved in CCD memories. Also the interconnection problem caused by the limited number of pins available on packages of complex IC's can be diminished if the pins are used efficiently by applying multiple-valued signals [5, 6]. In some cases the number of components and interconnections in a circuit can be decreased effectively, at the cost however of more complex basic devices.

One of the major obstacles in realizing multiple-valued logic circuits is the increased sensitivity to supply voltage variations, noise and process tolerances [7]. In most of the papers dealing with MVL circuits, the value of the radix is restricted essentially to three (in binary logic the radix is two). The circuit concepts discussed in this paper are not fundamentally restricted by the radix.

* Twente University of Technology, Solid-State Electronics Group, Dept. of Electrical Engineering, P.O.Box 217, 7500 AE Enschede, Netherlands.

A radix of four is however favourable for a number of reasons: first, the conversion to binary logic can be easily implemented. Second, the possibility of malfunctioning increases considerably if a higher radix is used, due to smaller noise margins [7]. Also the reduction in area per bit in MVL memories compared with that of RAM's becomes less significant for higher values of the radix [3]. All these arguments may explain the recent interest in research of four-valued logic [8].

Just as in binary logic, one requires a set of basic functions. Any MVL function can be realized by means of proper composition of these basic MVL functions [6, 8]. Depending on the specific applications, a choice of the most efficient set of basic functions can be made. An example of a complete set is listed in the table below:

Name of the function	Symbol	Definition
Minimum	min (x, y)	x if $x \leq y$ else: y
Maximum	max (x, y)	y if $x \leq y$ else: x
Literal	$a_x b$	$\begin{cases} (R-1) \text{ if } a \leq x \leq b \\ 0 \quad \text{else} \end{cases}$
Complement	$\bar{x}$	(R-1) - x
Successor	suc (x)	(x+1) modulo R

R = Radix

This set of functions has been implemented by Dao in I^2L technology [8]. The minimum, maximum and complement functions have their equivalent in binary logic being the AND, OR and INVERT function. The successor and the complement are merely included to make designing in MVL more convenient.

The minimum, maximum and complement circuits have been designed in CCD technology. Beside the compatibility with existing MVL memories, CCD technology is very well suited for LSI chip design, in which MVL is expected to have the most promising prospects. The properties of binary logic CCD's, can also be applied in MVL-CCD's. These are the properties of being able to add charge, to control it by means of another charge using a floating gate structure, and the overflow of charge out of a storage well due to its limited charge-handling capacity [1, 2].

The information in MVL-CCD's is represented by four different amounts of charge. These charge packets are integer-valued multiples (0, 1, 2 and 3) of the unity-charge packet Q_E. The difference in magnitude between the charge packets has to be sufficient for reliable detection of the distinct charge packet levels, even when the normal process tolerances, the variations in the supply voltages and noise are taken into account. In the present designs a unity-charge of 0.3 pC was used. This results in a storage area of 650 μm^2 if normal voltage levels are assumed and a pseudo one-phase clock is used.

The input circuit employs the "fill-and-spill" principle, and the output circuit consists of a floating diode connected to a charge-sensing amplifier in order to achieve a linear charge to voltage conversion.

THE MINIMUM, MAXIMUM AND COMPLEMENT FUNCTIONS

The schematic drawing in fig. 1, shows the principle of the minimum and the maximum functions. Their operation is based on the almost linear relationship between the charge in storage well 3, and the potential of the floating gate f on top of it (see fig. 3). The floating gate f is connected to the barrier gate b. A computer simulation of the floating gate behaviour is shown in fig. 3. A reset voltage of 8 V on the floating gate has been assumed.

As can be seen in fig. 2, the charge handling capacity of well 4, is determined by the floating gate potential and therefore by the size of the charge packet in 3. The four lines drawn under barrier gate b in fig. 2, indicate the different surface potential levels that are possible in this circuit.

If, for instance, the charge in well 3 has the logical value <1>, then well 4 is able to contain one unity-charge Q_E etc. The operation of the circuit in fig. 1 will be demonstrated for input charges X and Y having the logical values <2> and <3>. After the transfer of the input charges from the storage gates 1 and 2 to the respective storage wells 3 and 4, the charge <2> under 3 will change the potential of the floating barrier gate b, and will reduce the charge handling capability of well 4 to 2 Q_E. Because the charge packet in 3 has the logical value <3>, one Q_E will have to spill over from well 4 into well 5. Finally the charges in the wells 3 and 5 are added together in 6 resulting in the maximum output, and the residual charge <2> under well 4 is transferred to 7 resulting in the minimum output.

A schematic drawing of the complement circuit is presented in fig. 4. Each of the storage wells 2, 3 and 4 has a charge handling capacity of $1.Q_E$, and is separated by two barriers b. There are three floating gates situated on top of these wells. They control the injection of charge from the source S into the wells 5, 6 and 7. These floating gates have been designed in such a way, that a unity-charge packet present in wells 2, 3 and 4 is sufficient to block charge transfer from S into wells 5, 6 and 7 respectively. In 8, the charges in 5, 6 and 7 are added together. If a charge packet with, for instance, the logical value <2> is transferred into well 2, one unity charge will spill over from well 2 into 3, while 4 remains empty (see fig. 4 and fig. 5). As a result, only charge will be injected from the source S into 7. After the addition of the charge contents of the wells 5, 6 and 7 this results in the complement output. In a similar way, the input charges <0>, <1> and <3> will produce the logic outputs <3>, <2> and <0> respectively. This circuit has also the feature of being able to regenerate the logical charge level, because the floating gates f will only prevent the injection of charge from S into the storage wells if the charge levels in the sensing wells 2, 3 and 4 exceed a certain threshold. The surface potential diagram of the complementing "quantizer" is seen in fig. 5. Photographs of the layouts of the minimum, maximum and complement circuits are shown in fig. 6a,b.

MEASUREMENTS

The devices have been fabricated in the n-channel surface CCD double polysilicon process at Twente University of Technology, using 10 μm minimum geometry. In order to test the (analogue) minimum and maximum function, a dc voltage and a triangular shaped voltage of 2 kHz have been applied to the inputs. The clock frequency was 50 kHz. The inputs and the maximum and minimum outputs are shown in fig. 7. The supply voltages and clock pulse amplitudes which were actually applied, differed slightly from the theoretical values, due to clock feedthrough on the floating gate. The delay time τ_d is approximately equal to three times the clock period T_c ($\tau_d \simeq 3$ μs at f_c = 1 MHz). The effective area of the combined minimum and maximum circuit is 0.028 mm^2 and the power dissipation 118 μW at 1 MHz (excluding in and output buffers). At 60°C, and using a clock frequency of 10 kHz, the devices still operated satisfactorily.

In order to show the regenerating features of the complement circuit, a low frequency linear ramp voltage of 1 kHz was applied to the input. Fig. 8 shows the complementing and "regenerating" behaviour of the circuit.

The power dissipation of the complement circuit is 149 μW, and a chip area of 0.025 mm^2 is required. The delay time τ_d is twice the clock period T_c ($\tau_d \simeq 2$ μs at f_c = 1 MHz). The highest clock frequency turned out to be at least 1 MHz for all devices.

It should be emphasized that a 10 μm geometry had to be used, and no effort was made to minimize the chip area. In future designs with ion-implantation processing, the dimensions will be decreased.

A quaternary to binary logic converter and vice versa, a literal and a successor are under design at this moment. This will result in the availability of a complete MVL basic function set.

CONCLUSIONS

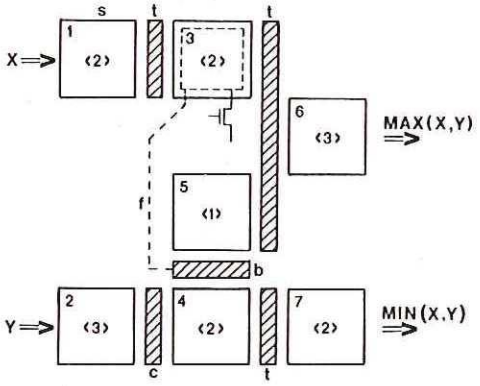
Despite certain problems, the advantages of MVL in IC's justify the research activities in multiple valued logic. The CCD technology turns out to be well suited for MVL design. The feasibility of charge-coupled devices for the implementation of multiple-valued logic has been shown. The design principles can be applied to any radix. The designed minimum, maximum and complement circuits worked successfully. However in the present designs they still suffer from clock feedthrough on the floating gates. It is expected that this problem will be significantly diminished in future designs.

ACKNOWLEDGEMENTS

The authors would like to thank J. Holleman for processing the devices, and O.W. Memelink for his encouragement and discussions.

REFERENCES

1. T.A. Zimmerman, et al., "Digital Charge Coupled Logic (DCCL)", IEEE Journal of Solid-State Circuits, SC-12, No. 5, pp. 473-485, October 1977.
2. H.G. Kerkhoff and J. Jansen, "Experimental Results of Binary Charge Coupled Devices", To be published.
3. J.E. Carnes, et al., "Fundamental Packing Density Limitations of CCD and RAM Memory", Electro 1977, Professional Program, Section 19, CCD Memories, pp. 19.4-1/9, April 1977.
4. ————————, "Multi-level Storage Packs Bits into CCD Memory", Electronics, pp. 7E-8E, September 29, 1977.
5. C.W. Ross, "Reducing System Interconnections with Multiple-Valued Logic", Electronics, pp. 122-124, September 15, 1977.
6. D.C. Rine, "Computer Science and Multiple-Valued Logic, Theory and Applications", North-Holland Publishing Company, 1977.
7. C.H. Séquin and M.F. Tompsett, "Charge Transfer Devices", Academic Press, New York, pp. 238-243, 1975.
8. T.T. Dao, "Threshold I^2L and its Applications to Binary Symmetric Functions and Multivalued-Logic", IEEE Journal of Solid-State Circuits, SC-12, No. 5, pp. 463-472, 1977.
9. K.C. Smith, "Circuits for Multiple-Valued Logic, a Tutorial and Appreciation", Proceedings of the Sixth International Symposium on Multiple-Valued Logic, pp. 30-43, May 25-28, 1976.



= reset most
s = storage gate
t = transfer gate
f = floating gate
b = barrier gate
c = synchronization gate

Fig. 1. Schematic drawing of the minimum and maximum circuit.

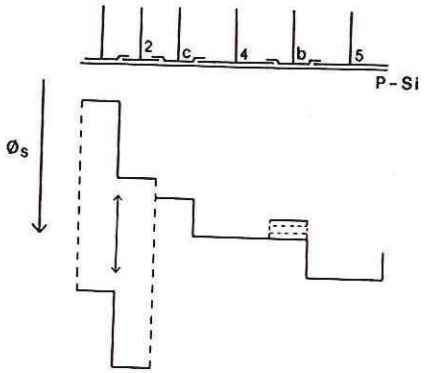


Fig. 2. The surface potential plot of the minimum and maximum circuit

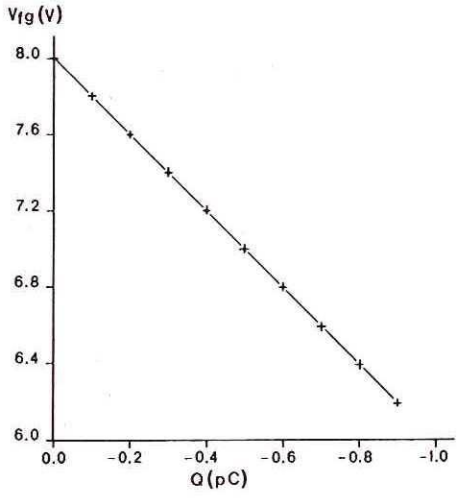
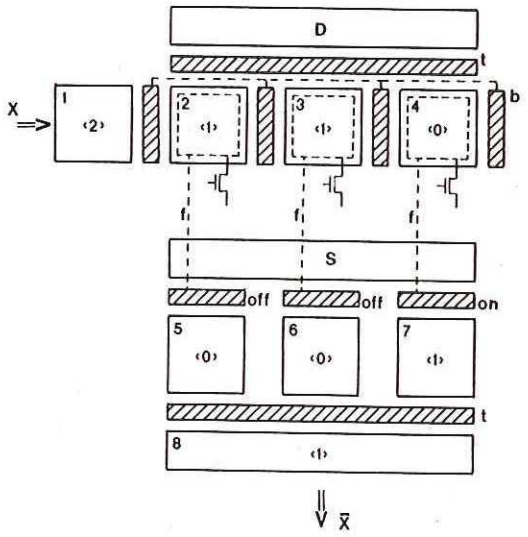


Fig. 3. The floating gate potential Vfg versus the input charge Q in the minimum-maximum circuit.



D = drain
S = source

Fig. 4. Schematic drawing of the complement circuit.

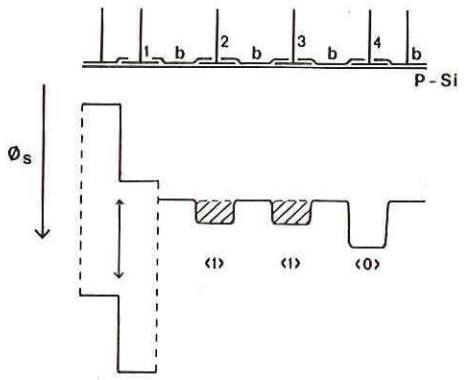


Fig. 5. The potential plot of the complement circuit.

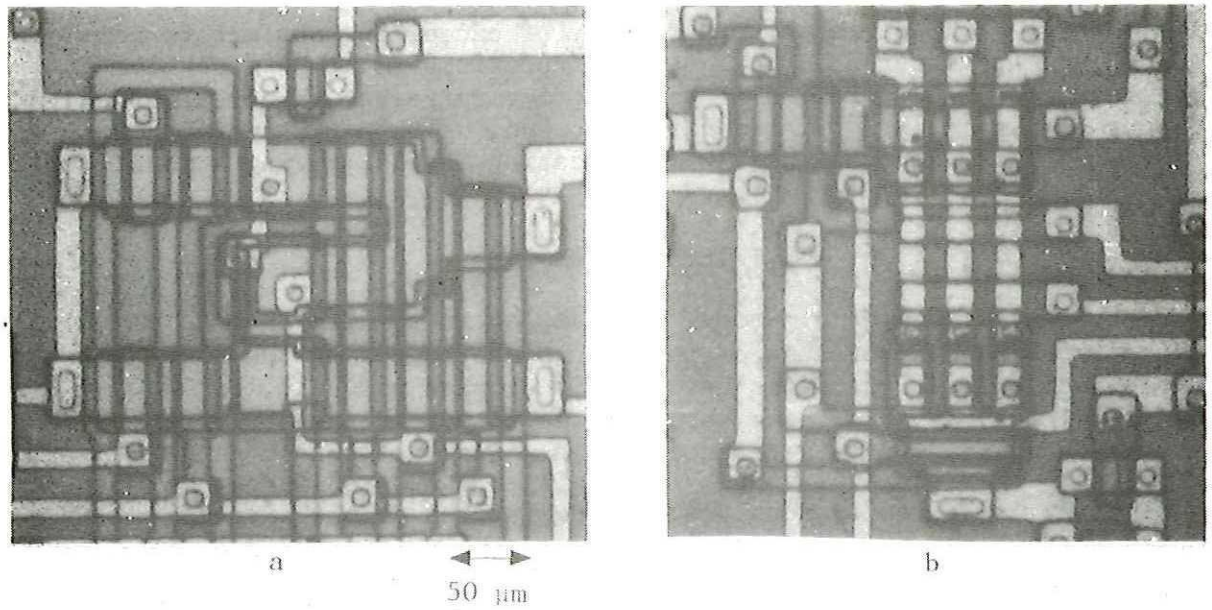


Fig. 6. a. The minimum-maximum circuit.
b. The complement circuit.

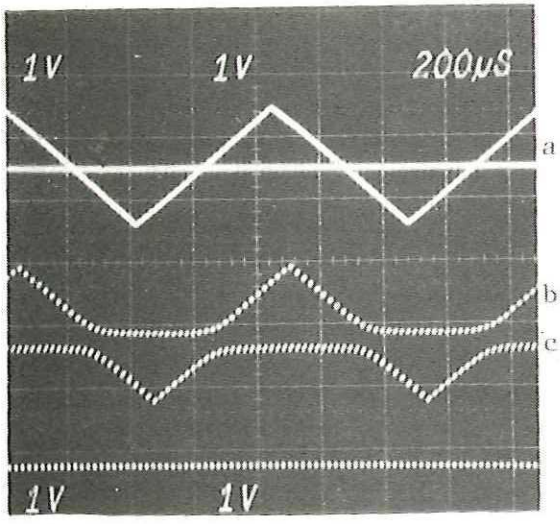


Fig. 7. a. The input signals of the minimum-maximum circuit.
b. The maximum output.
c. The minimum output.

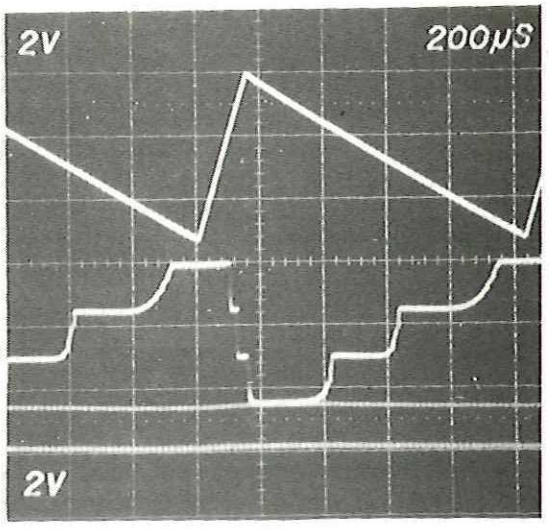


Fig. 8. a. The input signal of the complementing regenerator.
b. The output signal.