A MODEL FOR LIFE TESTING BURIED CHANNEL CCD MEMORIES

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ABSTRACT

A theoretical model has been developed and analyzed to establish conditions necessary for effectively life testing buried channel CCD memories. The analysis shows that buried channel CCD devices should have fewer oxide related failures compared to RAMS due to the reduced and negative field. Life test data taken on 64K-bit CCD memory do not show any oxide related failures in the memory array with an equivalent failure rate at 50°C of 0.004%/1000 hours.

INTRODUCTION

Accelerated life tests are carried out in semiconductor devices to predict the reliability or the meantime before failures (MTBF) of devices in the field. Typically, the devices are subjected to enhanced stress conditions to accelerate the inherent failure mechanisms. The failure rates obtained at the increased stress conditions are then extrapolated to nominal conditions with an acceleration factor based on an activation energy and assuming an Arrhenius type relation. Extrapolation inherently assumes that no new failure mechanisms are introduced at the enhanced stress conditions and the mechanisms are the same as at the nominal conditions. This paper will examine the applicability of some of the enhanced stress conditions used in n-MOS LSI circuits; specifically, memory circuits to buried channel CCD memories.

Reliability evaluation of dynamic RAM circuits have shown that the major failure mode for these devices is oxide breakdown at defects[1]. This comes as no surprise as a high percentage of silicon area in a memory circuit consists of thin oxide gate area. Thus, any effective accelerated testing for memory circuits, should include conditions for overstressing the gate oxide. Oxide breakdown has been found to be weakly temperature dependent[2] (0.3eV) whilst most other failure mechanisms, like crystal defects, metal migration have a strong temperature dependence (1.00eV). With the above discussion it is seen that the accelerated life test should employ stress conditions which would effectively stress the memory area which constitutes about 80% of the thin oxide area of the chip. Physics of the devices are discussed in the next section to determine the stress conditions.

ANALYSIS

In Fig. 1 the potential profile from the gate to the bulk are shown for a RAM cell (or surface channel CCD cell) and a buried channel CCD cell with substrate bias. From Fig.(1a) we see that for RAM cells the oxide field Eox is positive (i.e. VG>VS) and increases with increasing VG and the stored charge Q. Thus, we can conclude the following for n-MOS circuits: (i) V_T shifts due to Na type of contaminants is possible as Eox>0; (ii) high temperatures will decrease wear out time for oxides[3] and increase 'Q' due to leakage current thereby increasing Eox; (iii) increasing VG (or V_{DD}) will increase oxide stress; and (iv) as the data rate or frequency of operation is increased, oxide stress will increase due to increased duty cycle. Thus, to accelerate the oxide related failure mechanisms for n-MOS circuits, life tests should be conducted at a high temperature with higher than nominal voltage

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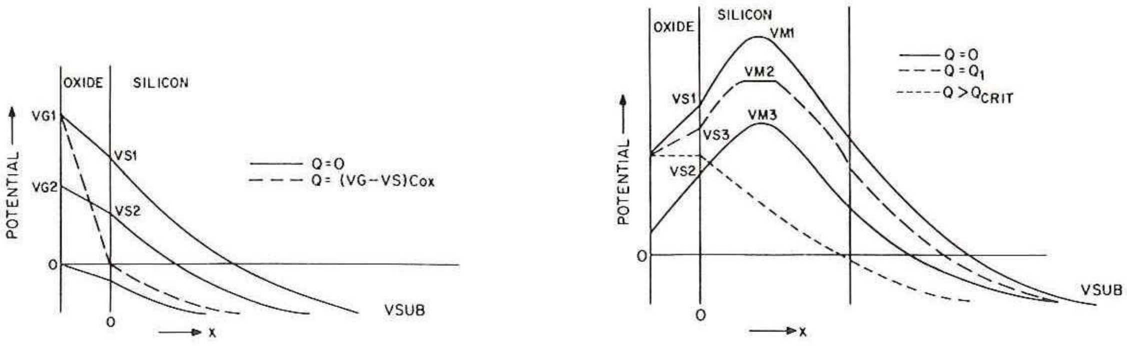
stress with full stored charge (1 or 0) dependent on the internal memory architecture) and at a maximum data rate.



1a. RAM OR SURFACE CHANNEL CCD CELL

1b. BURIED CHANNEL CCD CELL

Referring to Fig. (1.b.), the potential is seen to increase from the gate (VG) reaching a maximum (VM) then decreasing in the bulk to the substrate bias. Thus, the oxide field is negative (VG< VS) and is only a fraction of the applied voltage. As VG is increased, Eox decreases. As charge is introduced into the BCCD bucket, the maximum channel potential VM decreases decreasing the surface potential from VS1 to VS3 for VG = VG1 and Q_1>0, thus decreasing Eox. Eox reduces with increasing Q until it reaches zero at a critical Q = QCRIT beyond which it reverses sign (VS< VG) and increases rapidly. For normal BCCD operation, full bucket charge QF is such that VM is always greater than VS to prevent charge interaction with the surface and Eox reduces with charge.

In Fig. (2) plot of Eox Vs $^{Q}/_{QF}$ is given for the case of a RAM cell and n-BCCD cell. For this analysis the following values are assumed. VFB = -1.0V, VG = 10V, VBB = -5.0V and tox = 1000 Å. The oxide field for the RAM cell was calculated using depletion approximation[4] and assuming an uniformly doped substrate of NA = $5x10^{14}$ cm^{-3} and V_T = 1.0V. Full charge for the RAM cell is QF = $1.75x10^{12}$ cm^{-2}. The n-BCCD curve was obtained by the numerical solution of the Poisson equation[5] taking into account redistribution of the as implanted gaussian profile of the buried layer. Full charge for the n-BCCD (QF = $5x10^{11}$ cm^{-2}) is limited by the implanted barriers of the 2Ø device which is, by design, less than the charge needed for the onset of surface interaction or the maximum possible charge limited by implanted dose.

From Fig. (2) we see that for a full bucket Eox = $-2.9x10^5$ v/cm for n-BCCD which is 30% of the Eox = $1x10^6$ v/cm for the RAM cell. Also for the n-BCCD maximum oxide stress ($-5.5x10^5$ v/cm) of right polarity is present at low temperatures (negligible dark current with Q = 0 and VG = 0). For the corresponding conditions Eox is minimum for the RAM cell.

Let us now consider the effect of temperature and frequency on BCCD. As the stress temperature increases the charge in the buckets increase due to dark current and this increase in Q will alter Eox as discussed earlier. If the temperature is increased such that Q>QCRIT, Eox will become positive and increase rapidly for any further increase in temperature. The temperature at which Q = QCRIT is dependent on the BCCD design and the leakage properties of the device. The dark current build up for a bit is inversely dependent on the frequency due to the decrease in integration time as frequency 'f' increases.

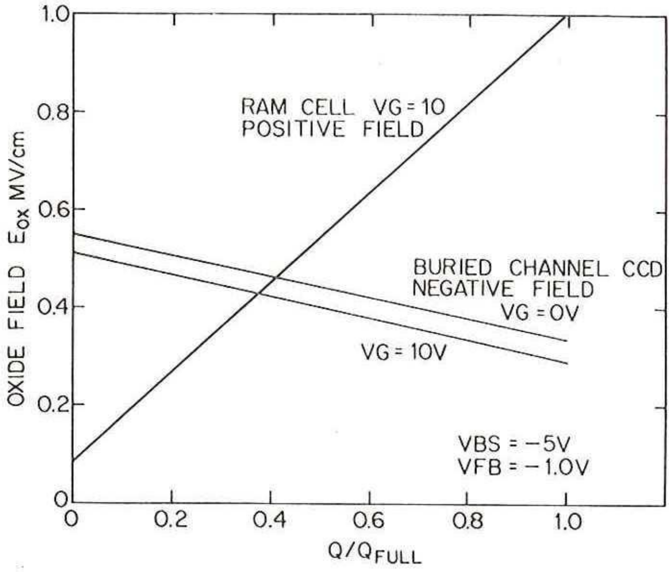


FIG. 2: OXIDE FIELD EOX VS BUCKET CHARGE Q/Q FULL

In CCD's leakage current is normally expressed as the storage or integration time (T_S) required to collect a given amount of charge (say 20% of full bucket). For a serial-Parallel-Serial S.P.S. block of 4096 bits, corresponding to the internal architecture of Fairchild's 64K CCD Memory F464, a data rate of f = 1MHz corresponds to an integration time of 4096/f sec. Charge collected in a bucket during this time is given by:

$$Q = I \left(\frac{4096}{f} \right) \qquad (1)$$

Where the leakage current I can be related to the storage time T_S at temperature T^oK by,

$$Q = 0.2\ QF = I\ T_S \qquad (2)$$

The storage time T_S is exponentially related to the storage time (T_{SO}) at room temperature (T_0)

$$T_S = T_{SO} \ \exp \ -A \left({}^1/_{T0} - {}^1/_{T} \right) \qquad (3)$$

Where A depends on the leakage mechanism and is equal to Eg/2q (Eg = Silicon band gap) when generation recombination within the depletion layer and surface is predominant and equals Eg/q when generation within a diffusion length byond the depletion layer is predominant. In Fig. (3) the experimentally obtained storage time is plotted vs $1/T$. Best fit to experimental data was obtained for $A = 6382/^oK$ ($= \frac{Eg}{2K}$) for $T < 338^oK$ and $10000/^oK$ for $T > 338^oK$.

Combining equations (1), (2), and (3) and Fig. (2), the Eox vs temperature have been plotted in Fig. (4) for a 4096 bit (S.P.S. array). The oxide field for $Q/Qf>/$ was obtained assuming liner extrapolation of the curve in Fig. (2). The figure shows that field reversal occurs at 106^oC for Tso = 200 msec and f = 1MHz whereas it is greater than 130^oC for Tso = 1000 msec and f = 3MHz.

The results in Fig. (4) are true for an isolated CCD bucket where charge builds due to dark current. Let us now consider what happens in a long shift register. At the end of the shift register if the collected dark current exceeds the maximum charge removal rate limited by the bucket size, charge smearing to adjacent buckets and rapid charge build up occurs, leading to local field reversal at a lower temperature.

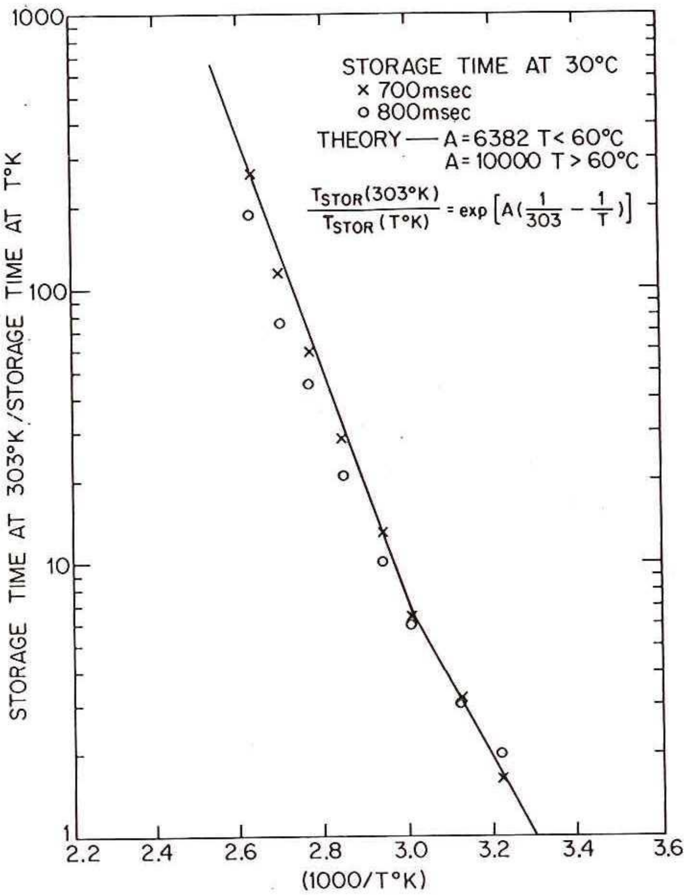


FIG. 3: (1/T°K) vs STORAGE TIME AT T°K NORMALIZED TO STORAGE TIME AT 30°C

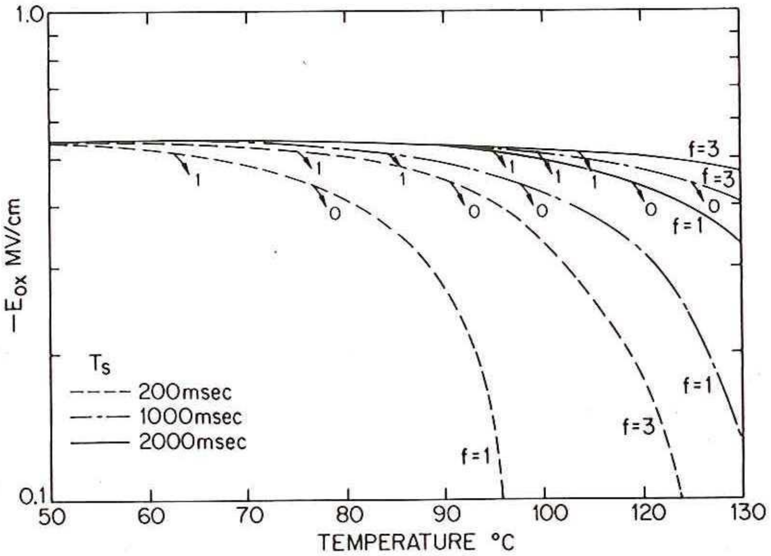


FIG. 4: OXIDE FIELD VS TEMPERATURE IN A BURIED CHANNEL CCD DEVICE

The onset of early field reversal is shown by arrows in Fig. (4). Thus we see that for T_{SO} = 200 msec and f = 1MHz the critical temperature has reduced to 74^{0}C for all '1' input from the isolated bucket value of 106^{0}C. In Fig. (5) the field reversal temperature for a long shift register is plotted against the room temperature storage time for two different 'f' and data patterns. From the figure it is seen that to avoid field reversal for an accelerated life test temperature of 125^{0}C, T_{SO} has to be greater than 2.3 sec. for f = 3MHz and greater than 7 sec. for f = 1MHz. While a storage time of 2.3 sec. is possible, 7 sec. is difficult to achieve. Hence, 1MHz life test at 125^{0}C will always lead to field reversal and enhanced field.

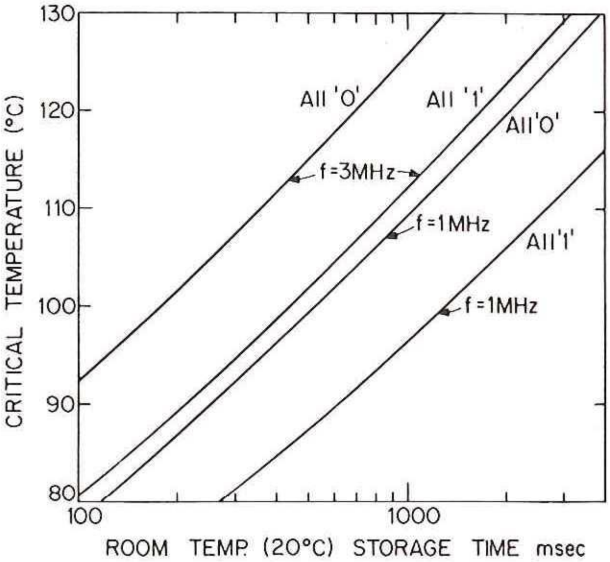


FIG. 5 CRITICAL TEMPERATURE FOR THE ONSET OF FIELD REVERSAL IN A 4096 BIT S.P.S. ARRAY AT 1 AND 3MHz DATA RATE AS A FUNCTION OF STORAGE TIME AT 20°C

CONCLUSIONS

From the analysis of n-BCCD devices we see that during normal operation of n-BCCD devices; (i) instability due to Na^+ ion shift is not possible as the oxide field is negative, (ii) voltage across the oxide reduces with increasing Q and VG and (iii) the oxide field is 50% of the maximum field in RAMS reducing the wear out time(3) and thus increasing the reliability.

If the accelerated test temperature is above the TCRIT of the device, field reversal would make the memory array susceptible to instability and also lead to excessive Eox. Both conditions are non-existant for functional devices and hence care must be exercised in extrapolating these failures to nominal temperatures. A low test temperature with VG = 0 would subject the memory array to maximum voltage stress. But a low temperature stress may not be sufficient to accelerate the failure mechanism for the peripheral circuits of the memory.

Accelerated life test results on Fairchild 464 at 70°C show 0 failures for total device hours of 35,000 and 3 failures at 125°C for total device hours of 95,700. Two of the high temperature failures were identified as ionic contamination in the MOS peripheral circuits, one functionally marginal. No oxide related failures were observed within the memory array. The equivalent failure rate at 50°C based on an acceleration factor of 1.0 ev is 0.004%/1000 hrs. The results indicate the superior reliability performance of buried channel CCD memories over RAMS and agrees with the model presented.

Burn-in of F464 to catch marginal parts was done at three different temperatures, room, 70°C and 125°C. The results showed that 125°C burn-in was needed to effectively weed out marginal parts in a short burn-in time.

The life test and the burn-in data indicate that though a low test temperature is optimum for stressing memory oxide of n-BCCD devices, it is not sufficient for accelerating the failure mechanisms for the peripheral circuits and a higher temperature, 125°C is needed. Based on the analysis of the physics of n-BCCD device discussed in this paper, care must be taken in extrapolating 125°C test results to nominal temperatures.

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