

# DESIGN OF A 262 KBIT CCD CHIP

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With ever faster processors, yet disk speed remaining almost the same, the need for an intermediate secondary storage technology has become apparent. To fulfil this need, a prototype 262 kbit CCD memory component was designed. It is to be fabricated in 2.5  $\mu\text{m}$  n-MOS double silicon-gate technology. Implanting the silicon II transfer gate areas separately allows to adjust the potential difference under silicon I and silicon II electrodes necessary for two-phase clocking operation.

Fig. 1 shows a block diagram of the chip. It is organised as 64 memory arrays of 4 kbit each and carries all the necessary clock generators so that it can be operated from a single low-capacitance clock at frequencies between 1 and 5 MHz.

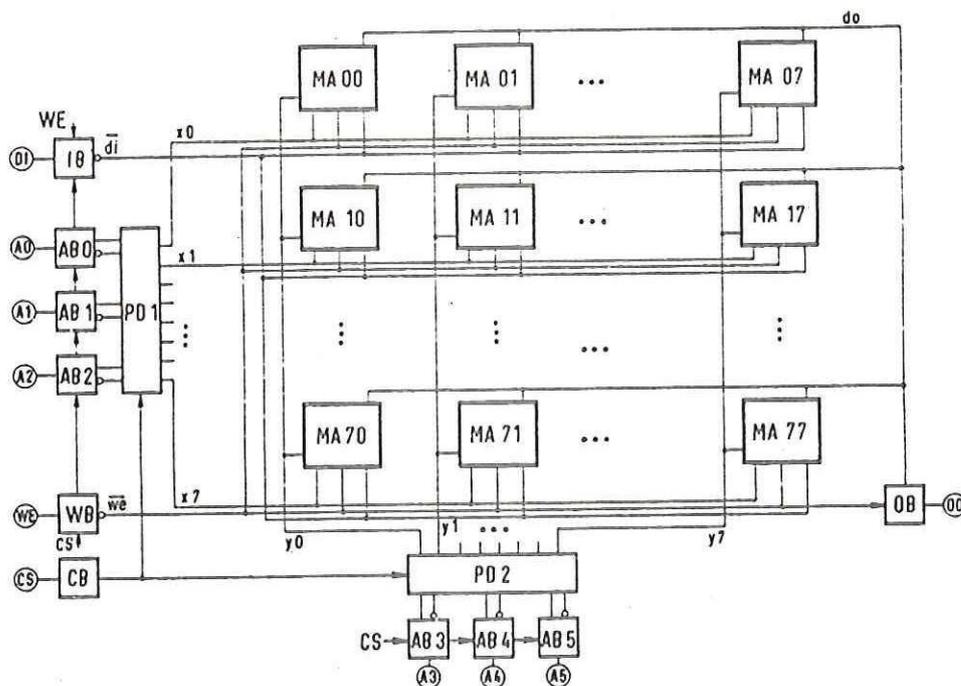


Figure 1. Block diagram of 262 kbit CCD chip

MA Memory Array; IB Input Buffer;  
 AB Address Buffer; PD Predecoder;  
 WB Write-Enable Buffer; CB Chip-Select  
 Buffer; OB Output Buffer

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The memory array uses the Condensed Serial-Parallel-Serial organisation; in the 64 parallel channels the pure 'One-Electrode-Per-Bit' principle is applied which effectively doubles storage density, but requires individual clock pulses for all 64 storage locations.<sup>2,3</sup> Fig. 2 shows a schematic drawing of the memory array.

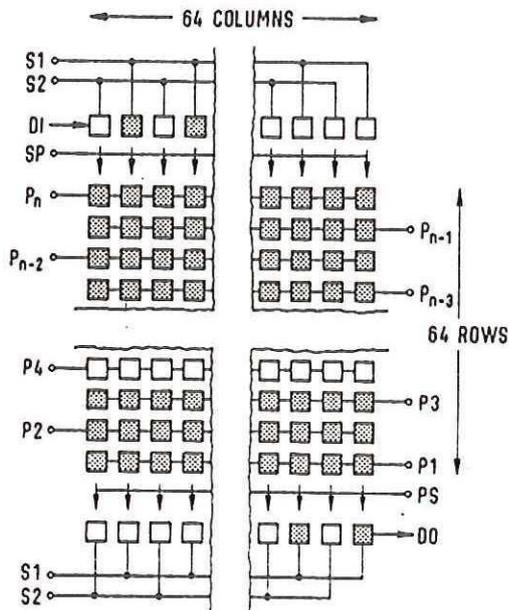


Figure 2. CSPPS memory array using the EPB principle in the parallel channels

S1, S2 two-phase clocks of serial input and output chains;  
P1, P2, ... clocks for parallel channels;  
SP, PS transfer clocks (serial-to-parallel and parallel-to-serial);  
DI, DO Data In, Data Out

The actual layout of the memory array, fig. 3, clearly shows the parallel channels (which are defined in a first implantation step), alternately covered by silicon I and silicon II electrodes (hatched and dotted areas, respectively). Two novel features are included in this layout.

Firstly, information is transferred into (out of) one of two adjacent parallel channels always from (into) the same location of the serial input (output) chain. The transfer clock pulses SP1 and SP2 (as well as PS1 and PS2) are thus completely regular, they occur once every 64 cycles. This is in contrast to the normal CSPPS organisation where irregular intervals of 31 and 33 cycles alternate.

Secondly, additional filler charges are introduced. As usual in surface channel CCDs, the information '0' is represented by a 'fat zero' in order to keep the interface states beneath the surface (traps) always occupied. However, after transfer of the information charges into the parallel channels the input chain would nevertheless run totally empty, and the charge of a following '1' would be diminished. This is overcome by feeding in additional filler charges from the side (electrode VFC) whenever the input chain is emptied (the transfer clock pulse SP3 for the filler charges being the logical OR of SP1 and SP2). The filler charges then precede the next information train, finally flowing into a sink (VDD) at the end of the input chain.

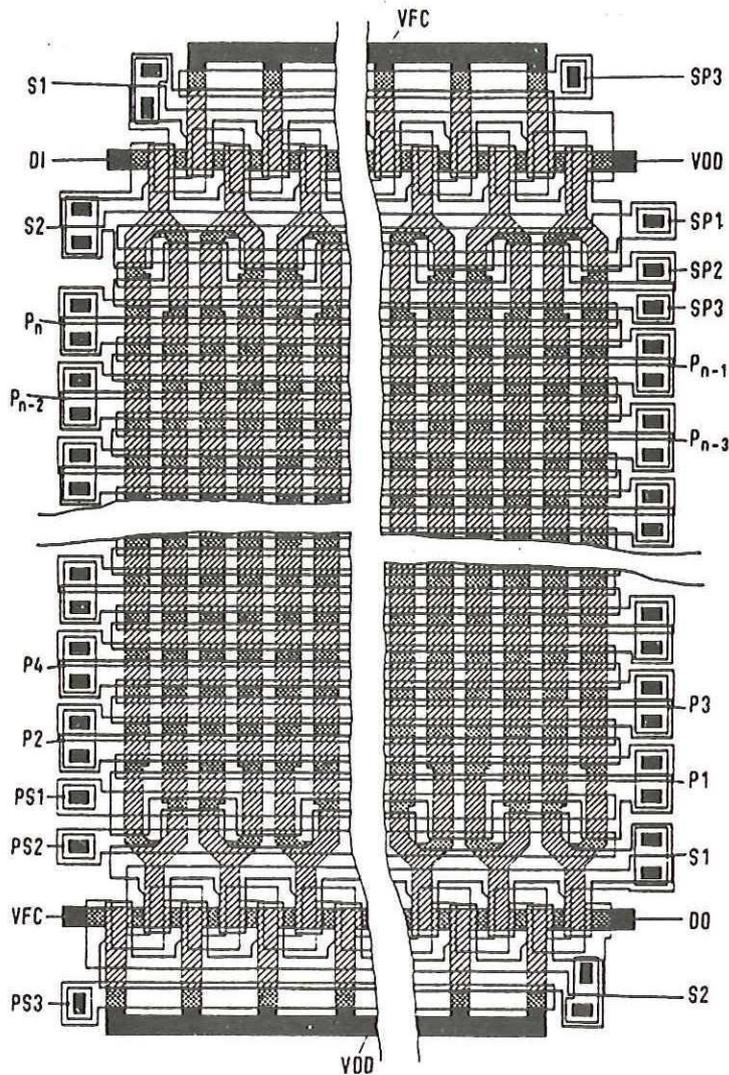


Figure 3. Layout of 4 kbit memory array

In the output chain things are reversed: a single filler charge source (VFC) at the beginning feeds in filler charges which follow the information train; immediately before new information from the parallel channels is transferred (PS3 = PS1 OR PS2), they are all removed simultaneously into a common sink (VDD) located along the chain.

Fig. 4 is a section of the overall timing diagram, showing external as well as internal timing relations. Externally, S1 is the only clock pulse to be supplied; from it S2 is derived internally. All input signals (Chip Select, Addresses A0 through A5, eventually Write Enable and Data In) must be valid between S1 and S2. In case of a read operation, Data Out is valid from the end of the same cycle until the middle of the next one (which at lower shift frequencies will be farther away than drawn). A read-modify-write operation is not provided.

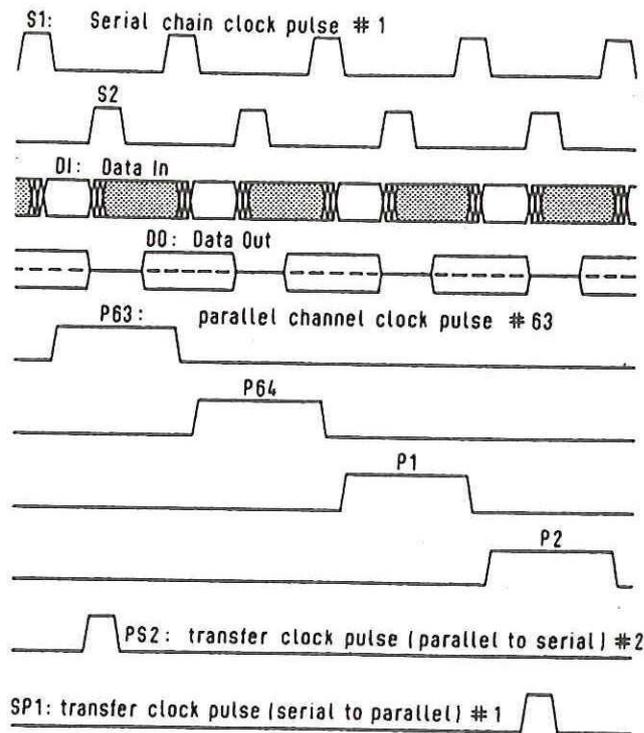


Figure 4. Timing diagram for highest shift frequency

Internally, the 64 individual EPB clock pulses which drive the parallel channels are generated in a pair of shift registers of 32 stages each, located along the sides of the chip. The stages of the left shift register drive all the even electrodes, those of the right shift register all the odd electrodes, the clock lines being drawn across the whole chip.

Since all stages of the two shift registers are accessible, it is easy to derive clock pulses at arbitrary points in time within the whole shift cycle. So e.g. the transfer clock pulse PS2 is the logical AND of P63 and S2 (likewise  $SP1 = P2 \text{ AND } S2$ ).

All these principles of operation were successfully tested with a single 4 kbit memory array on a test chip, fig. 5. In the centre is the quadratic memory array itself with input in the upper left, output together with discriminator and output amplifier in the lower right corner. Along the left and the right edge the clock shift registers are situated (which in this case appear relatively large because they serve only one memory array). Several internal clock generators complete the picture.

While the memory array on this test chip was still an open loop, for the final memory chip it was closed by a refresh station which, based upon xy-decoding, also passes data input or output information.

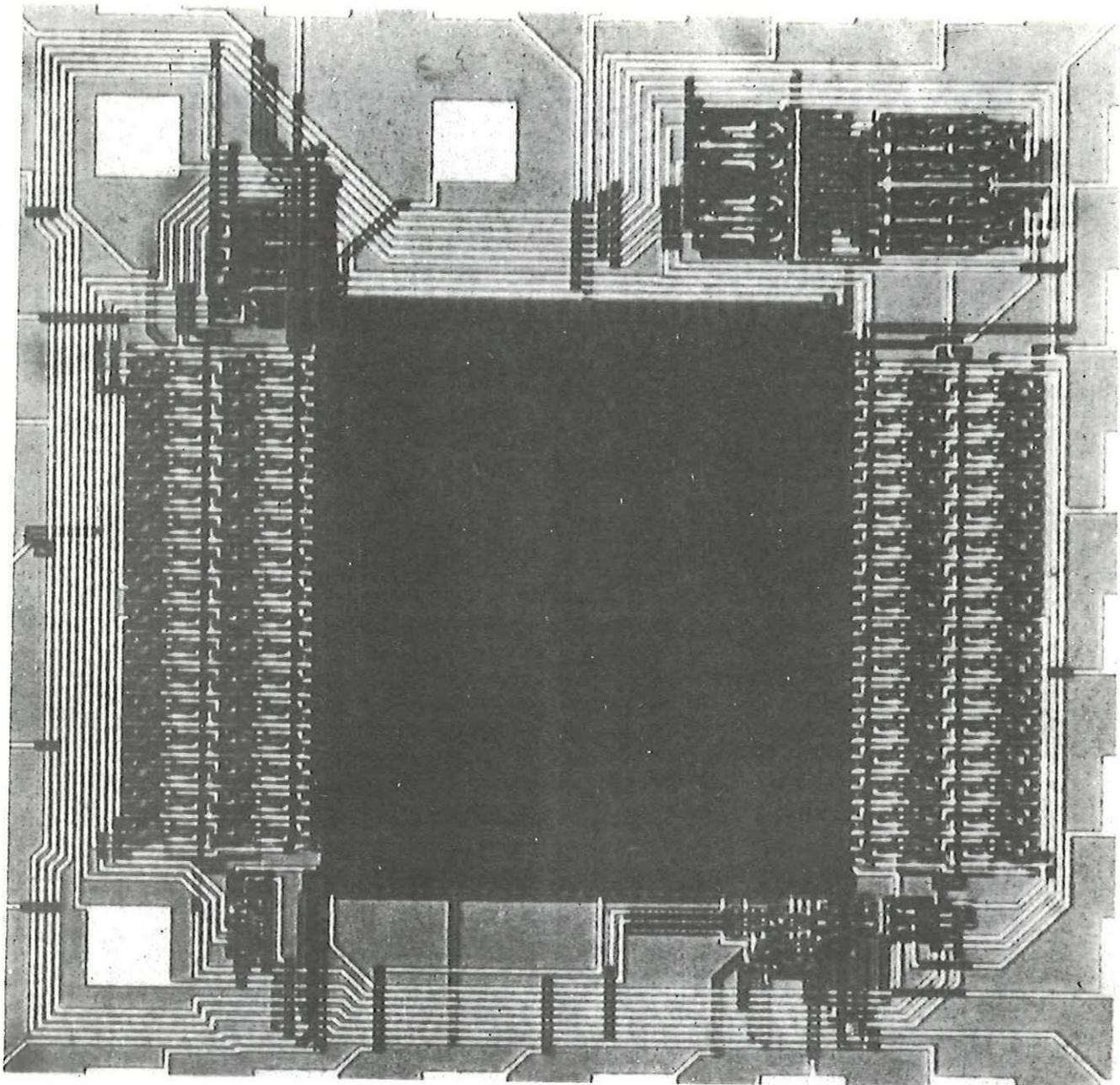


Figure 5. Photomicrograph of 4 kbit test chip

The next step in the design process was the construction of a complete memory chip with all peripheral circuitry (input buffers, predecoders, output amplifier), yet with reduced capacity of 65 kbit. It was built as four quadrants, each consisting of a block of 2 x 2 memory arrays arranged central-symmetrically. Except for the absence of address buffers ABO and AB5, the block diagram of this memory chip is similar to fig. 1.

From this design a prototype memory chip of 262 kbit could be derived simply by an expansion by a factor of two in each dimension; the peripheral circuitry, especially all the internal clock generators, remained essentially unchanged. Fig. 6 is a drawing of the complete chip showing the overall arrangement of 8 x 8 memory arrays (4 x 4 central-symmetrical blocks). In contrast to the test chip with a single memory array (fig. 5), on the prototype memory chip the parallel channel clock drivers along the left and the right edge contribute only relatively little to the total area.

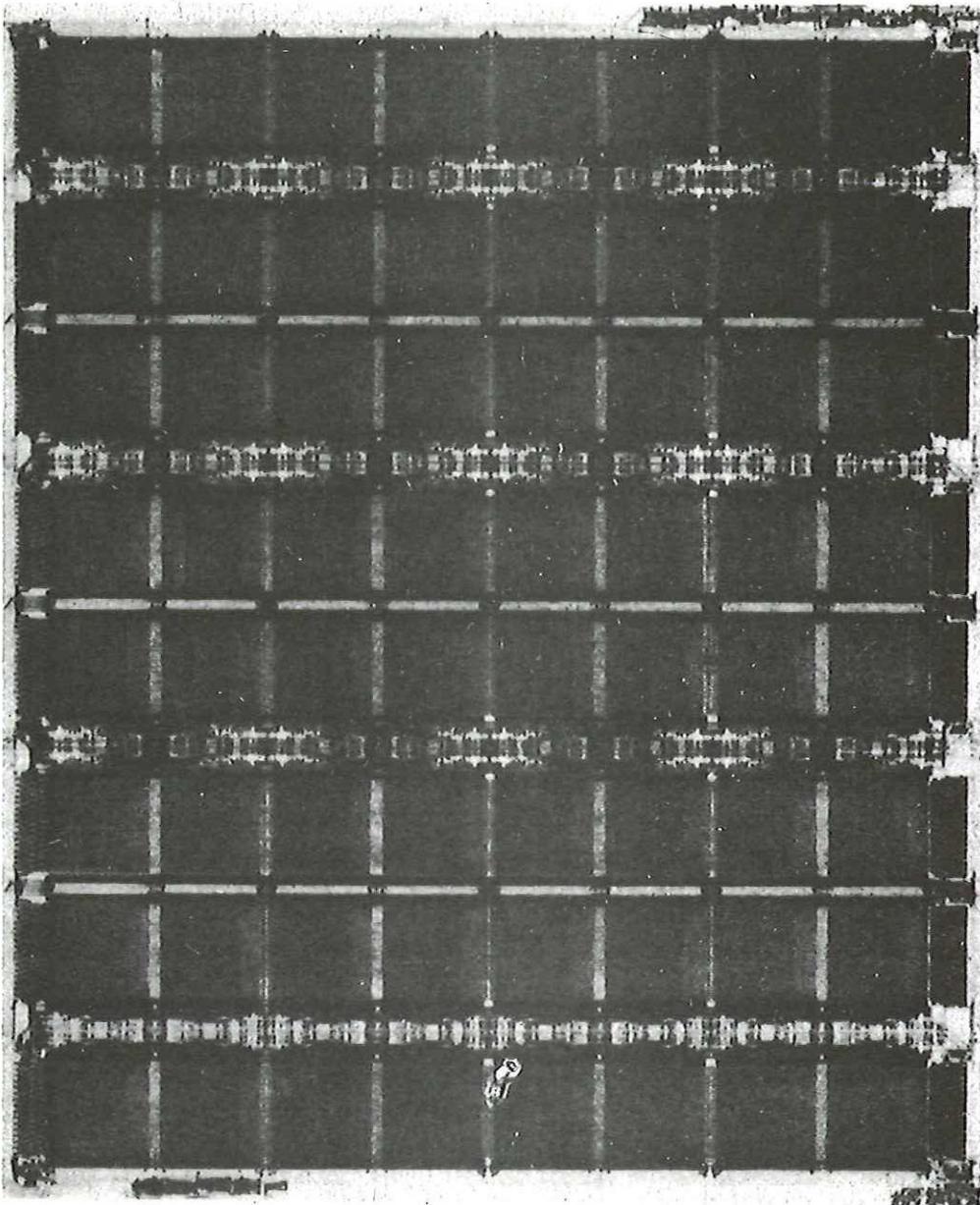


Figure 6. Drawing of 262 kbit chip

#### References.

1. Schneider, P.: CPU-utilization and secondary-storage performance - The demand for a new secondary-storage technology. AFIPS Conf. Proc. 46 (1977) pp. 819-825
2. Göttler, E.; Grüter, O.; Schneider, P.: CCD Memory Circuits of High Bit Density. IEE Conf. Publication No. 130, First European Solid State Circuits Conference, Canterbury (1975) pp. 76-77
3. Doering, E.; Göttler, E.; Grüter, O.; Schneider, P.: CCD Memory Circuits of Highest Packing Density - Technological and Electrical Improvements. Microelectronics and Reliability 16 (1977) pp. 419-425