

AN ALL-IMPLANTED CCD/CMOS PROCESS

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ABSTRACT

A process has been developed that combines double polysilicon, surface type, n-channel CCD's with silicon gate CMOS circuits on the same substrate. The process is all ion-implanted (including the getter step), and requires only one more masking step than a full high voltage CMOS flow. Two CCD shift registers with internal CMOS peripheral circuits, and a CMOS op-amp have been designed and characterized to demonstrate the design flexibility afforded by the availability of both p and n channel transistors.

I. Advantages of CCD/CMOS

CMOS has several circuit performance advantages over NMOS that outweigh its additional processing complexity. In digital circuits, CMOS has lower static power, higher speed, and higher drive capability; while in linear circuits, it has higher gain per stage, and wider input and output voltage swing. This paper describes a process that combines the superior performance of CMOS with double polysilicon surface type n-channel CCD's. The process makes it possible to have CCD with high speed CMOS clock drivers and peripheral circuits. Alternatively, it makes possible a digital CMOS chip with CCD's as circuit functions.

II. Device Cross-Section

A cross section of the resultant structure is shown in fig. 1. The n-channel CCD is located in the P-tub region, as is commonly done with n-channel transistors in CMOS. This contrasts with processes which start with an on-going CCD/NMOS flow, and locate the p-channel transistors in an N-tub.¹ The P-tub method, it turns out, has several useful circuit design advantages, as will be shown later.

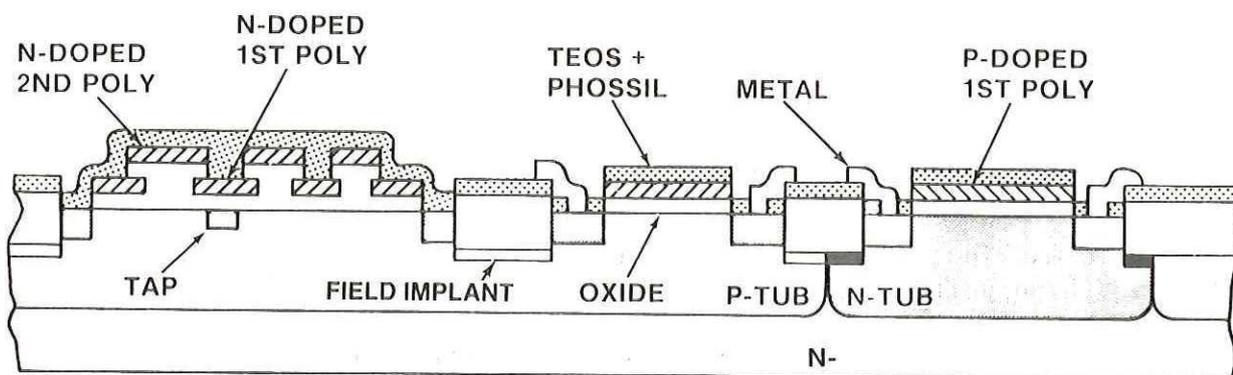


Fig. 1 - Cross section of the CCD/CMOS structure.

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The CCD/CMOS process is fully compatible with the 5 μm silicon gate Planox (localized oxidation of silicon) CMOS flow. In fact, all process specifications are identical except where obviously different, e.g., second gate oxide/poly. Similarities visible in fig. 1 are the field implants under the field oxide, and the so called "double flavor" poly, i.e. p-doped poly over p-channel transistors and n-doped poly over n-channel transistors. Double flavor poly reduces the magnitude of threshold voltages; however, a metal strap is necessary for connecting the two poly types.

The CCD uses double poly to permit two phase operation. The first and second gate oxide thicknesses are 900 \AA and 3200 \AA respectively. The P-tub doping concentration is $5 \times 10^{15}/\text{cm}^3$. An approximately 2 to 1 ratio in surface potentials is obtained when +15V with respect to CCD substrate (P-tub) is applied to both electrodes. The 15 volts are divided into 0 to +10V clock voltages and a -5V CCD substrate reverse bias.

While fig. 1 shows the n-channel transistor and CCD to be in the same P-tub, in general that is not necessary. For example, the NMOS transistors of a CMOS clock driver circuit can be in a P-tub separate from that of the CCD it drives. And by providing a negative bias to the CCD P-tub, the usual positive translation of all clocking wave form is conveniently obtained. A second benefit of the separate P-tub concept is that the NMOS transistors now operate with less substrate bias, giving lower threshold drops across such circuits as the ubiquitous output source follower.

III. Process

The masking sequence is given in Table I below:

Table I - Masking Sequence for CCD/CMOS

Substrate adjust (opposite of P-tub)
 Active area
 p-field
 n-field
 Tap (optional)
 1st poly
 2nd poly
 p+ source/drain
 n+ source/drain
 Preohmic
 Metal
 Passivation

Total number of masks: 11 + 1 optional

The basic masking sequence uses one more step (the 2nd poly) than the full 18V high voltage CMOS flow.

There are significant departures from the conventional silicon gate CMOS process, all slanted towards keeping the total number of masking steps down. The usual procedure is to start with a blanket phosphorus implant for substrate adjust. This is then followed by a heavier boron implant to create the P-tub regions.

For the CCD/CMOS process, it was decided to exclude the substrate adjust implant from the P-tub region in an attempt to increase its minority

carrier lifetime. This was accomplished without an extra mask by means of a nitride/oxide sequence identical to the Planox process. A nitride pattern protects the P-tub during substrate adjust implant and the subsequent 10,000Å oxide growth. The nitride is then stripped, leaving a thin layer in the oxide for the boron to penetrate and form the tub.

A second departure from the conventional silicon gate CMOS is in the doping of the first poly. If the doping takes place after both poly are patterned, the overlap region between the two poly would not get doped. So, after the first poly deposition, a $2 \times 10^{15}/\text{cm}^2$ 100 KeV phosphorus implant is performed, producing a sheet resistance of $1\text{K}\Omega/\text{sq.}$ after anneal (see Fig. 2). Later, during the source/drain implant, the exposed first poly over the n-channel is doped to $35\Omega/\text{sq.}$ and poly over p-channel is doped to $107\Omega/\text{sq.}$ This process sequence also saves a masking step.

The first gate oxide is grown at 1050°C , with dry $\text{O}_2/6\% \text{HCl}$. When the second gate oxide repeated the same cycle with a longer O_2/HCl time for the thicker oxide, severe "blistering" of the underlying poly 1 occurs.² A combination wet O_2 followed by dry O_2/HCl with a drying time in between eliminated the problem.

Device parameters averaged over several lots are presented in Table II.

Table II - Average CCD/CMOS Parameters

substrate N_D	$6.5 \times 10^{15}/\text{cm}^3$
P-tub N_A	$5.2 \times 10^{15}/\text{cm}^3$
tox_1	910Å
tox_2	3180Å
V_{tn} poly 1	0.62V
V_{tn} poly 2	1.86V
V_{tp} poly 1	-0.60V
n+ ρ_S	13 Ω/square
n+ poly 1 ρ_S	35 Ω/square
n+ poly 2 ρ_S	42 Ω/square
p+ ρ_S	54 Ω/square
p+ poly 1 ρ_S	107 Ω/square
tap ρ_S	84 Ω/square
n+ V_B	26V
p+ V_B	24V
field V_T over P-tub	24V

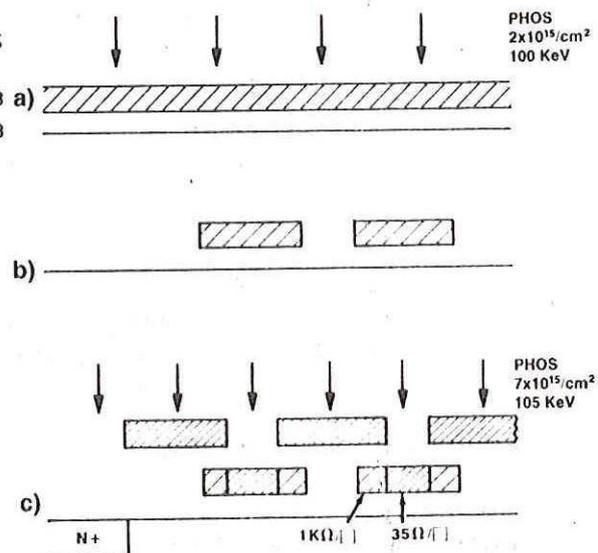


Fig. 2 - Implant sequence for double poly CCD structure.

IV. Getter

The CCD/CMOS process is all ion-implanted for better control and reproducibility. It also minimizes the number of high temperature steps. This carries over into gettering as well. Damage gettering³ is accomplished by implanting argon at 100 KeV and a dose of $3 \times 10^{15}/\text{cm}^2$ to the back of the wafer. This getter is done as the very first step in processing, and again just after P-tub drive-in. This contrasts with the phosphorus gettering commonly used for NMOS, which is generally done as the last high temperature step (since it is competing with the heavily doped source/drain regions for the metallic impurities.) As a result, capacitance-time (C-T) response times in the 60 to 140 sec. range have been obtained when a first gate oxide capacitor is pulsed from -7.0V to +7.0V. This represents an average minority carrier lifetime of 18 μs .⁴ Additionally, it was found that the electron carrier lifetime inside the

P-tub correlates well with the hole lifetime outside of it. This would indicate that the minority carrier lifetime is a function of the starting material and the processing it sees, and that the P-tub doping is not heavy enough to create a difference.

On actual CCD shift registers, chip delays of 1.35 seconds have been measured at room temperature. In addition, good uniformity of $< \pm 15\%$ (see fig. 3) in generation rate across a 64-bit shift register has also been obtained. The good uniformity is attributed, for the most part, to incorporation of HCl during gate oxidation.⁵ Fig. 3 is obtained using the integration mode of operation⁶ where the clock is stopped for a relatively long integration time before rapidly shifting out. The individual output pulse then corresponds to the generation rate in one bit position.

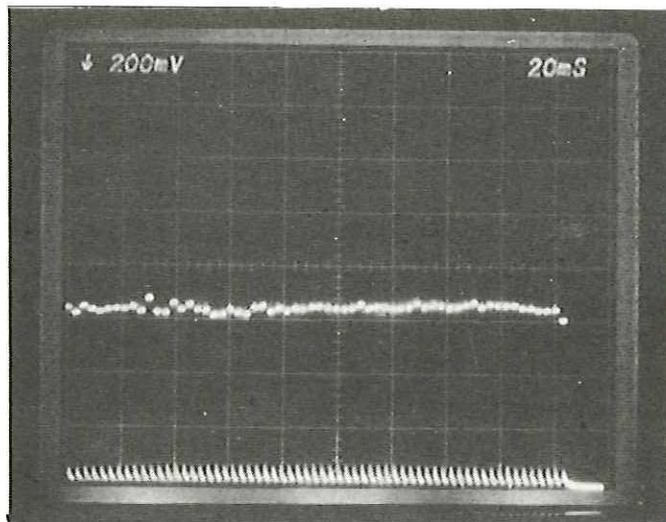
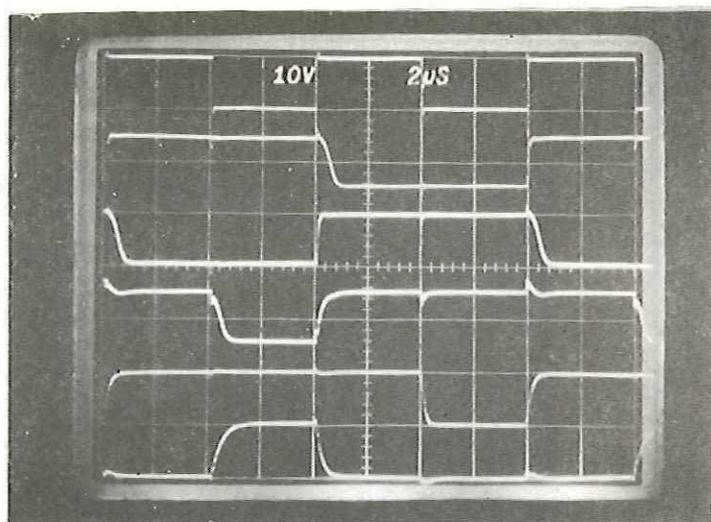
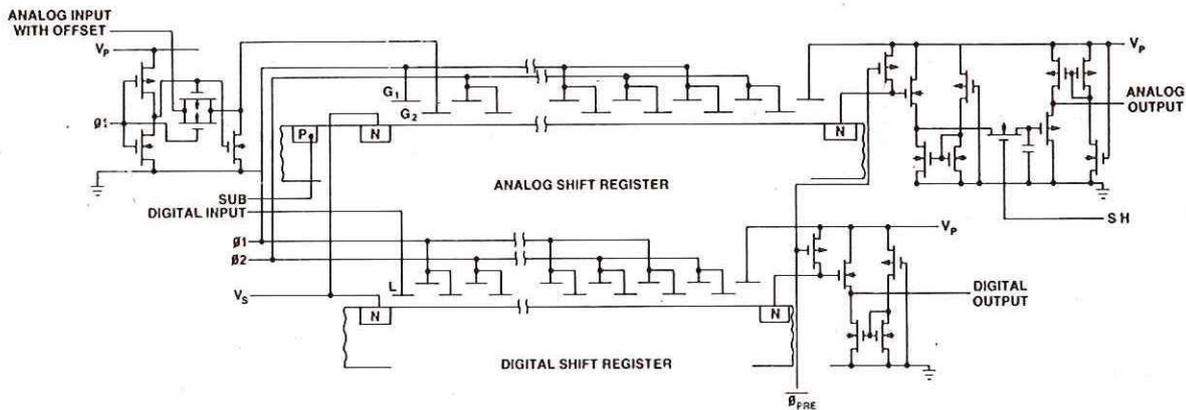


Fig. 3 - Output from a 64 bit shift register after 600 ms of integration time, out of a possible maximum of 1.35 seconds, showing uniformity better than 15%.

V. Device Measurements

Several lots using two mask sets have been processed over a period of time. Among the circuit functions are two 128-bit shift registers (see fig. 4a). One is designed for digital signals and has a $22 \mu\text{m}$ bit length and $10 \mu\text{m}$ channel width. It has an n-channel transistor source follower circuit with a current source for a load. The other is designed for analog inputs and has a $28 \mu\text{m}$ bit length and a wider channel width of $100 \mu\text{m}$ for better signal to noise ratio. It has, in addition to the same output source follower circuit, an output sample and hold circuit with level shift and an input chopping circuit. Note the design flexibility afforded by the availability of both n and p channel transistors. Both registers have been operated with an internal CMOS clock driver (see fig. 4b) at a typical transfer inefficiency, ϵ of 1×10^{-3} at 25.6 KHz. Better devices with $\epsilon < 1.5 \times 10^{-4}$ have also been measured. A 550 mV output swing is available on the digital register versus 6V on the analog one. And, with the +10V/-5V supply, the analog register input voltage range is from 4V to 10V.



Clock in

$\phi 1$

$\phi 2$

V_S

$\bar{\phi}_{pre}$

S/H

Fig. 4 - a) Circuit schematic of a 128-bit digital shift register with output source follower, and of a 128-bit analog shift register with output source follower, sample and hold with level shift, and input chopper circuits.

b) Internally generated clock wave forms with a deliberate 0.3 μs $\phi 2$ to $\phi 1$ overlap and a 0.5 μs ramp fall time.

Several CCD applications require the use of operational amplifiers. It is important then for any CCD process to be able to handle linear MOS circuits. For our purposes, we adapted a metal gate CMOS op-amp design in common use at Motorola into silicon gate. Normally, an MOS op-amp in silicon gate is not practical because the self-aligning feature of the source/drain junctions preclude the use of a bottom plate in making the compensation capacitor out of gate oxide. With the CCD/CMOS process, the tap implant is available for that purpose. The circuit schematic and die photograph is shown in fig. 5, and measurement results are listed in Table III. The die size, excluding bonding pads, is 240 mil² (0.15 mm²). This design compares favorably in size and performance with recently reported NMOS op-amps.⁷

VI. Acknowledgement

The author gratefully acknowledges the contributions of Clarence Lund, Michael Sugino and David Yost to the project.

Table III.

Measured Op-Amp Characteristics
(Lot 19D0 Wafer 5)

Supply voltage	$\pm 5V$
Supply current	0.45 mA
Slew rate +/-	0.4/80V/ μs
A_V open loop	51 dB
Unity gain bandwidth	2.0 MHz
Phase margin	46°
CMRR	44 dB
Common mode range	$\pm 5V$
Input offset	-53 mV
Rise and fall time	200 ns
Overshoot	20%
r_o	240 K Ω

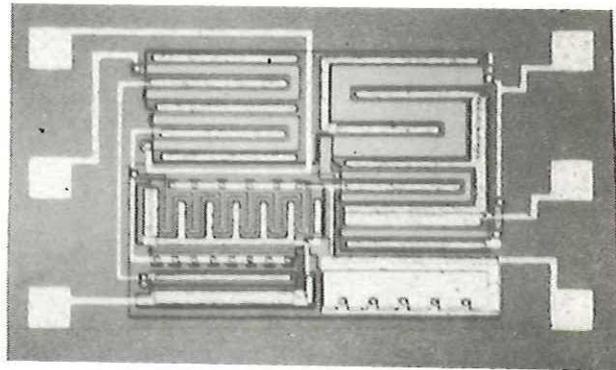
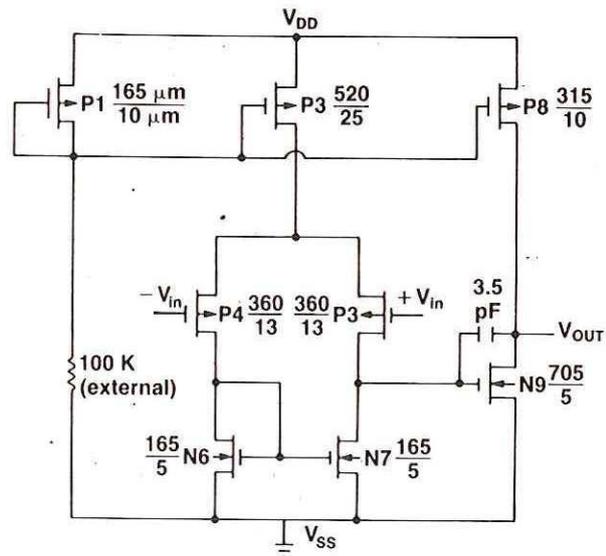


Fig. 5 - Circuit schematic and die photograph of a silicon gate CMOS op-amp using tap implant for bottom plate of compensation capacitor.

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