259 GATE GaAs CCD SHIFT REGISTER FOR HIGH SPEED APPLICATIONS

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ABSTRACT

An ultra high speed GaAs Schottky barrier gate, buried channel CCD operating at clock frequencies up to 500 MHz is described. Implications for signal processing application are discussed.

INTRODUCTION

Development of Charge Coupled Devices (CCD's) in GaAs (as well as other III-V compounds) is attractive, since the higher electron mobility in GaAs, as compared with silicon ($\sim$5:1) makes possible much higher performance in signal processing devices. The higher mobility makes possible shorter (drift-aided) transit time for charges from under one gate to the next, thus increasing the maximum possible clock frequency. More importantly, the higher electron mobility in GaAs results in high speed on-chip FETs for clock-drive and charge detection.

The difficulty in obtaining a stable device quality insulator (such as a native oxide) has prevented development of a conventional M.I.S. (metal-insulator-semiconductor) CCD. Schottky barrier gate buried channel CCD's in GaAs have been realized[1 2] and have been shown to have good transfer efficiency (>0.999 per transfer)[3]. Recent experiments on a second generation device (to be reported here) have been carried out and complete CCD operation (input-transfer-output) at 500 MHz has been achieved.

Apart from the Schottky barrier gate structure, these devices differ from conventional CCD's in yet another significant aspect. Instead of the p-substrate, n-channel arrangement typically used in high speed buried channel technology, the GaAs high speed devices employ a semi-insulating substrate and n-type channel. This arrangement has important implications for high speed applications since stray capacitance is reduced substantially with the consequence that power dissipation in the clock drivers ($P_d = cv^2 f$) is reduced accordingly. Also, the semi-insulating substrate eliminates the need for a separate channel stop.

GaAs CCD PERFORMANCE IMPLICATIONS

The principal advantage of GaAs is its very high electron mobility; typically over 5 times that of correspondingly doped silicon. This high electron mobility (up to 8500 cm^2/vs at 300° K) makes it possible to achieve high electron velocities in n-channel CCD's (and FETs) even with relatively low electric fields (low bias or clock voltages), so that very high speed operation can be achieved with minimum power dissipation. This point is illustrated in Fig. 1 for the case of the GaAs CCD by the calculated worst case electron transit time or corresponding maximum clocking frequency for a 4-phase CCD. Here, 5μm long gates with 1μm gaps are considered. Potential disturbances caused by absence of electrodes in the gap (a serious problem with very thin channels) have been ignored for this calculation. Assuming an essentially empty well, the only driving field

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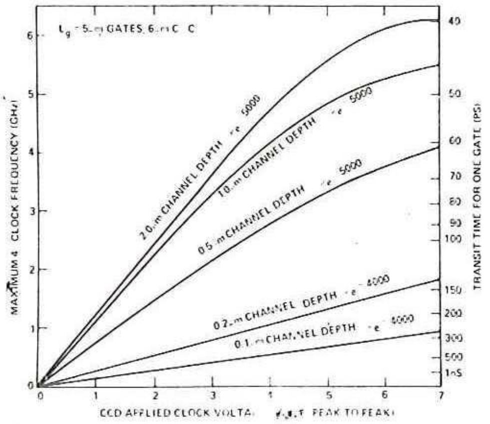

Fig. 1. GaAs BCCCD's drift transit time-limited maximum clock frequencies.

on the electrons is from the fringing fields from the adjacent gate electrodes, whose magnitude is strongly dependent on the depth below the gate electrodes where channel conduction takes place (essentially the thickness of the n-layer). Notice in Fig. 1, that for channel thicknesses of 0.5μm to 2μm, maximum CCD clocking frequencies of 3 to 5 GHz should be obtainable with this 5μm long gate device, even with low levels of clocking voltage (2.5 to 4.5 V_{pp}). Figure 2 illustrates the role of electron mobility in achieving this performance. Here the transit time results calculated for the 1μm channel CCD with the GaAs velocity-field characteristic assuming μ_e = 500 cm /vs (from Fig. 1) is compared with the results assuming μ_e = 750 cm /vs (for Si) in the same CCD structure. We see from Fig. 2 that the GaAs CCD could achieve much higher speed than the equivalent silicon device and (using $p \propto v^2$) could achieve any given speed (e.g., 1 GHz) with only 2% to 4% of the power dissipation.

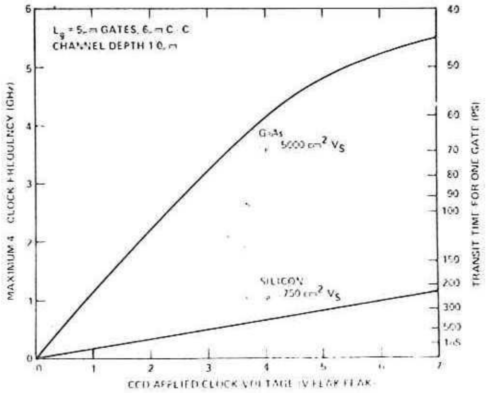

Fig. 2. Drift transit time-limited maximum clocking frequency for buried-channel CCD's.

While CCD's are transit-time limited devices, the switching speed of FETs (such as would be used for on-chip clock drivers and amplifiers) is dominated by load capacitance and transconductance. The transconductance is in turn also a function of the electron velocity-field characteristic at low bias levels.

EXPERIMENTAL RESULTS

As mentioned above a second generation GaAs CCD has been fabricated to investigate the high speed characteristics of CCD's. Figure 3 is a photomicrograph of this device. This is a 64 bit, 4 phase device with a total of 259 gates. A similar device with 32 bits (131 transfers) is

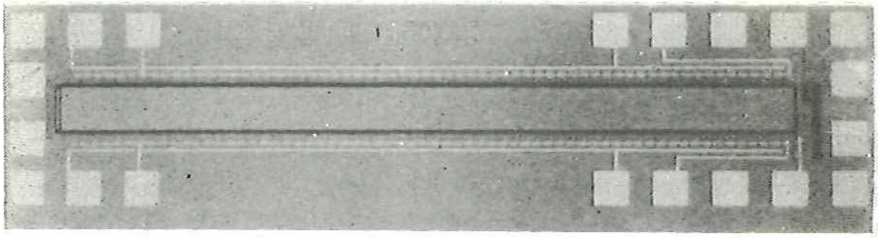

Fig. 3. 259 gate GaAs CCD with on-chip amplifier.

incorporated on the mask set. The gates are 100μm wide x 5μm long and are separated by 1μm gaps. An integral source-follower amplifier with reset FET is employed and can be seen in the right edge of the photo. Two levels of metallization isolated by plasma deposited silicon-nitride are employed to accomplish the interconnection of the gates. The n-GaAs channel is isolated by a mesa-etch. Figure 4 shows the organization of the chip schematically. Signal input is accomplished either by current injection or by potential equilibration.

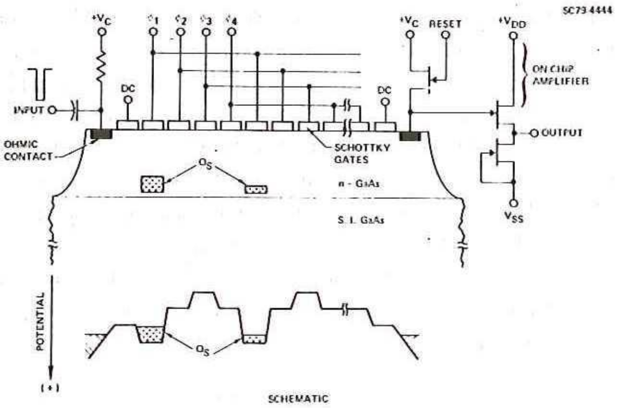

Fig. 4. Schottky barrier gate GaAs CCD schematic.

Charge transfer experiments have recently been carried out on these new devices. The longer device (250 transfers) has been tested at low frequency ($f_d \leqslant 1$ MHz) and shows transfer efficiency well in excess of 0.999 per transfer. The 131 gate device has been tested at high frequency and shows CTE >0.999 per transfer from 100 kHz to beyond 150 MHz. Figure 5 shows the CCD output response at 100 MHz clock frequency to a pulse which is approximately 5 clock cycles long, applied as indicated in Fig. 4. The device has been operated at up to 500 MHz, however CTE is difficult to measure at this frequency due to limitations inthe external clock-drivers and pulse generators currently used in the experiments. Nevertheless, this is to our knowledge, a factor of four higher speed than previously reported for CCD operation.

SIGNAL PROCESSING APPLICATIONS FOR HIGH SPEED CCD'S

Linear signal processing functions such as filtering, correlation, convolution, etc., at high sample rates ($>10^9$ samples/sec) and/or high input resolution (>8 bits) are well suited for the GaAs CCD operating in the analog sampled data mode.

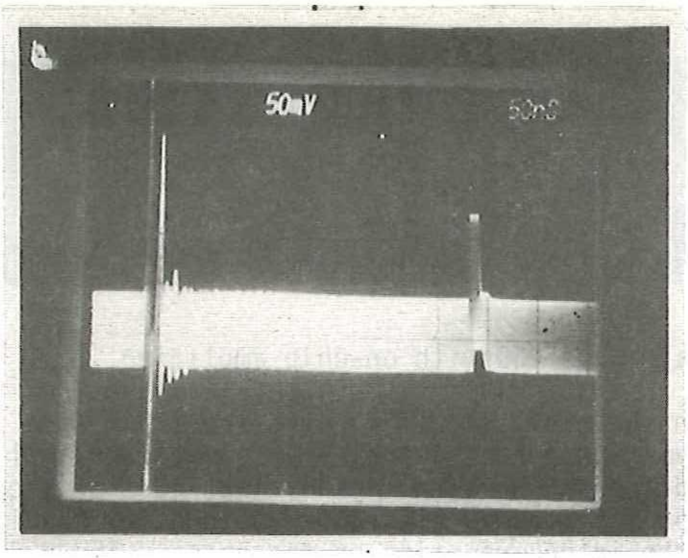

Fig. 5. GaAs CCD Output at $f_{cl.}$ = 100 MHz.

Transversal filter configurations of GaAs CCD's promise attainment of truly prodigious rates in signal processing. For example, a 250 cell CCD transversal filter operating at a 4 GHz clock rate would be performing an incredible 10^{12} shift-multiply-add operations per second (10^7 multiplies/sec is very fast for current silicon digital IC technology). High performance GaAs CCDs in a chip z-transform transversal filter could serve as the basis for a low cost, low power, high performance gigahertz-bandwidth spectrum analyzer or ECM receiver, for example. These devices should also find many applications at even more modest ($<$1 GHz) clock rates as fully self-contained clock drivers, input-output interfaces, etc., are achieved to make the CCDs relatively "user transparent".

CONCLUSION

The superior electronic properties of GaAs together with the extremely rapid progress being made in GaAs integrated circuits technology, promise a class of charge coupled devices capable of $>$1 GHz clock frequency operation.

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