HIGH-SPEED CCD SIGNAL PROCESSING -- A TECHNOLOGY DEVELOPMENT

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ABSTRACT

An integrated CCD analog/binary correlator is described which has been fabricated in a newly developed CMOS/CCD process. The chip contains the CCD clock driver and program register clock driver circuits. The CMOS peripheral circuits have been shown to operate at 30 MHz with 6 μ gate lengths and to 50 MHz with 4 μ gate lengths. This more than doubles the previously obtained speed at which NMOS/CCD peripheral circuits have been operated. Although problems in input and output structures and power budgets must be solved, it is felt that the CMOS/CCD process that has been developed offers an excellent approach to the design of high speed integrated CCD circuits.

INTRODUCTION

Most of the work on CCD devices has been limited to the frequencies below 10 to 20 MHz. One reason for this is that the existing peripheral devices were not capable of operating much above this range and there are several immediate applications for the CCD devices in the region below 20 MHz. However, there are applications for CCDs above the 20 MHz range, e.g. radar systems and it is desirable to push the CCD to these higher frequency levels[1,2]. The CCD has been shown to be capable of operating to at least the 100 MHz range with good transfer efficiency at RCA; so the CCD does not appear to be a limiting factor. However, since it is highly desirable to integrate as many functions as possible onto the CCD chip; the necessary clocking circuitry and the peripheral devices must operate at least up to the desired clocking frequency. The NMOS devices used in most recent integrated CCD chips are not capable of operating at much higher frequency than 15 MHz; but recently developed CMOS circuits have been shown to operate in excess of 30 MHz and to as high as 100 MHz. The development of a compatible CMOS/CCD process would seem then a natural step to take in the development of an integrated CCD.

From the system aspect it is necessary to integrate as much of the CCD support circuitry on the chip as possible; so a major goal of this technology development is to merge the CMOS and CCD technologies. The CMOS process which will be used is a polysilicon gate CMOS process utilizing closed gate n-channel and p-channel FETs. These devices then provide maximum g_m to drive capacitance ratios since the driver output diffusion capacitance can be minimized. This closed-gate complementary logic (C^2L) technology also provides the inherent low power of CMOS logic which helps to reduce the total chip power. The development of an integrated C^2L/CCD process allows:

- C^2L devices for peripheral circuits
- immediate 30 MHz operation
- possible future operation to 100 MHz
- low power capability of CMOS.

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PROCESS DEVELOPMENT

The C^2L and CCD technologies must be combined so that the best characteristics of both are maintained. Since n-channel CCDs provide the highest speed, the lowest dark current generation and highest transfer efficiency when fabricated in a low defect starting material, it is necessary to begin with a p-type starting material. The C^2L process will also be fabricated in the p-type substrate and the p-channel devices are formed in n-wells, which are implanted with phosphorus and driven-in during a long, high temperature cycle. Since the C^2L process does not have field oxide, a major modification must be made to provide the dielectric isolation for the CCD. An isoplanar (recessed) field oxide structure will be used to provide this isolation. This isoplanar oxide can provide CCDs with excellent characteristics and can also be used to provide minimum gate-geometry NMOS FETs. The C^2L/CCD process is then based on a C^2L technology using dielectric isolation (isoplanar oxide) to separate the C^2L portions of the chip from the NMOS/CCD sections, see Fig. 1.

CHIP DESIGN

Fig. 2 shows the test chip which has been designed to evaluate the C^2L/CCD process. The main array (outlined by the white band in the figure) is a 128-stage analog/binary correlator which includes a two-phase CCD clock driver and a binary program register clock driver on the chip[3,4,5]. The rest of the chip is devoted to test circuits which are used to characterize the C^2L/CCD process. All of the logic circuits use 6 μ design rules and have been simulated to 30 MHz. A block diagram of one stage of the correlator is shown in Fig. 3. This shows the location of the NMOS/CCD sections of the chip which are isolated from the C^2L portions of the chip by the isoplanar oxide as shown in Fig. 1. The CCD is a two-phase buried n-channel CCD with two levels of polysilicon and ion implanted transfer regions under the second polysilicon gates. Transistors T71 through T74 are NMOS devices and transistors T75 through T87 are n-channel or p-channel C^2L devices. Transistors T75 to T80 form a set/reset latch which can be isolated from the code program register by T81. This allows the program register to be loaded while correlations are being performed with the previous code which has been latched-up. Clocks ϕ_A and ϕ_B are generated on chip by the program register clock driver circuit shown in Fig. 2. All clock phases required for the CCD are generated in the CCD clock driver circuit except the input strobe phase. The input strobe has not been generated on-chip since the best input technique has not been determined for high speed CCDs. Since there is no conceptual problem in the design of a given input circuit, the open-ended design on the present chip allows the optimum technique to be determined and implemented.

CIRCUIT SIMULATIONS

The circuits have been simulated using a CAD program which uses the Frohmann-Bentchkowsky model as modified by J. E. Meyer. Since no previous data was available for the C^2L model parameters as used in the integrated C^2L/CCD process, they were estimated from previous work on C^2L circuit designs. However, after the first run was made the thresholds for the n-channel devices had to be adjusted, and the second run provided the actual model parameters which were then used to verify the operation of the C^2L/CCD circuits. Figure 4 shows the current voltage characteristics of

several of the FETs which were used in the chip design. Fig. 4a and 4b show p-channel devices and Fig. 4c shows an n-channel device with 6 μ gate lengths. The devices shown in Fig. 4a and 4c were the unit cell devices used in both the CCD clock driver and the program register driver circuits. Although the 6 μ gate length devices were used in the original, Fig. 4d shows a 4 μ gate length p-channel device which was tested in a later version of the clock driver circuits and will be discussed below. The parameters shown in the figures are M: mobility, VT: threshold voltage, SL: slope of the current in the saturation region, C: mobility falloff due to electric field, and N: n-channel or P: p-channel devices. Fig. 5 compares the results of the default values with those obtained using the actual C^2L/CCD model parameters. The figure shows CAD simulations of the CCD clock driver circuit (ϕ_1 and ϕ_2); the default simulation for ϕ_2 is shown by the dashed line and the simulation results obtained from the actual C^2L/CCD model parameters is shown by the solid lines.

POWER CONSIDERATIONS

One of the limiting factors in an integrated high speed CCD device is the power generated by the peripheral circuits in driving the gate capacitance presented by the CCD transfer gates. At frequencies below about 100 MHz this power is reactive power and can be estimated by CV^2f. For the 128-stage CCD in the analog/binary correlator each phase of the CCD has about 40 pF. At 50 MHz the power is around 200 mW with a 10 volt peak to peak clock swing. If the program register is included, the total power at 50 MHz of 100% efficient drivers will be on the order of 750 mW. Although this is not excessive it will degrade the characteristics of the CCD due to the temperature rise in the chip and for longer arrays it will be even worse. An acceptable alternative with bigger arrays or at higher speeds is to take the final driver stages off chip since most of the power is generated in these last stages. This will impose additional design problems of phase delays but these problems should be fairly easy to overcome, and it is much simpler from the system standpoint to add a translater/buffer stage than it is to design all the rest of the logic. The goal in this development is to be able to generate all the logic on chip and as many of the peripherals as possible.

RESULTS

The C^2L peripheral circuits on the chip have operated to as high as 50 MHz as shown in Figure 6. This figure shows a photomicrograph of the program register clock circuit and output waveforms obtained from it at 20 to 50 MHz. The 50 MHz waveform was obtained from a program register which had 4 μ gates and since the limit of the pulse generator used in this test was 50 MHz it is expected that this structure will operate at higher rates. The peak to peak voltage has decreased in this photo because the circuit was originally designed with 6 μ gates to operate at 30 MHz. However, a unit cell approach was used in its design so that the polysilicon gate could be changed easily to 5, 4, or 3 μ gate sizes. In a design for 4 μ at 50 MHz the final output stage would be increased in size to provide the full swing. The CCD clock drivers also have been operated at the designed 30 MHz with 6 μ gates. A test CCD which was included on the chip has been operated at 20 MHz with a transfer inefficiency of about 2×10^{-5}. However, the full analog/binary correlator has not been tested but it is expected that it will operate at 30 MHz with a charge transfer inefficiency on the order of 1×10^{-4}.

ACKNOWLEDGMENTS

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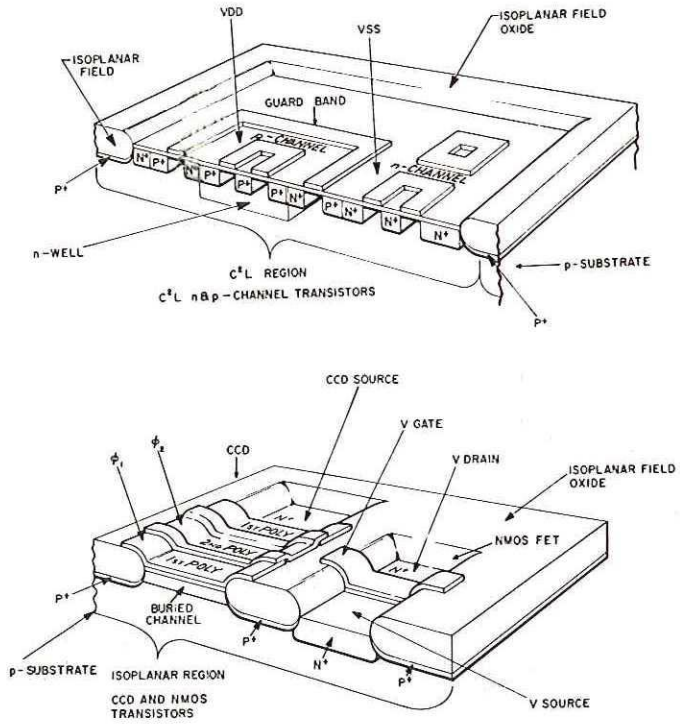


Figure 1

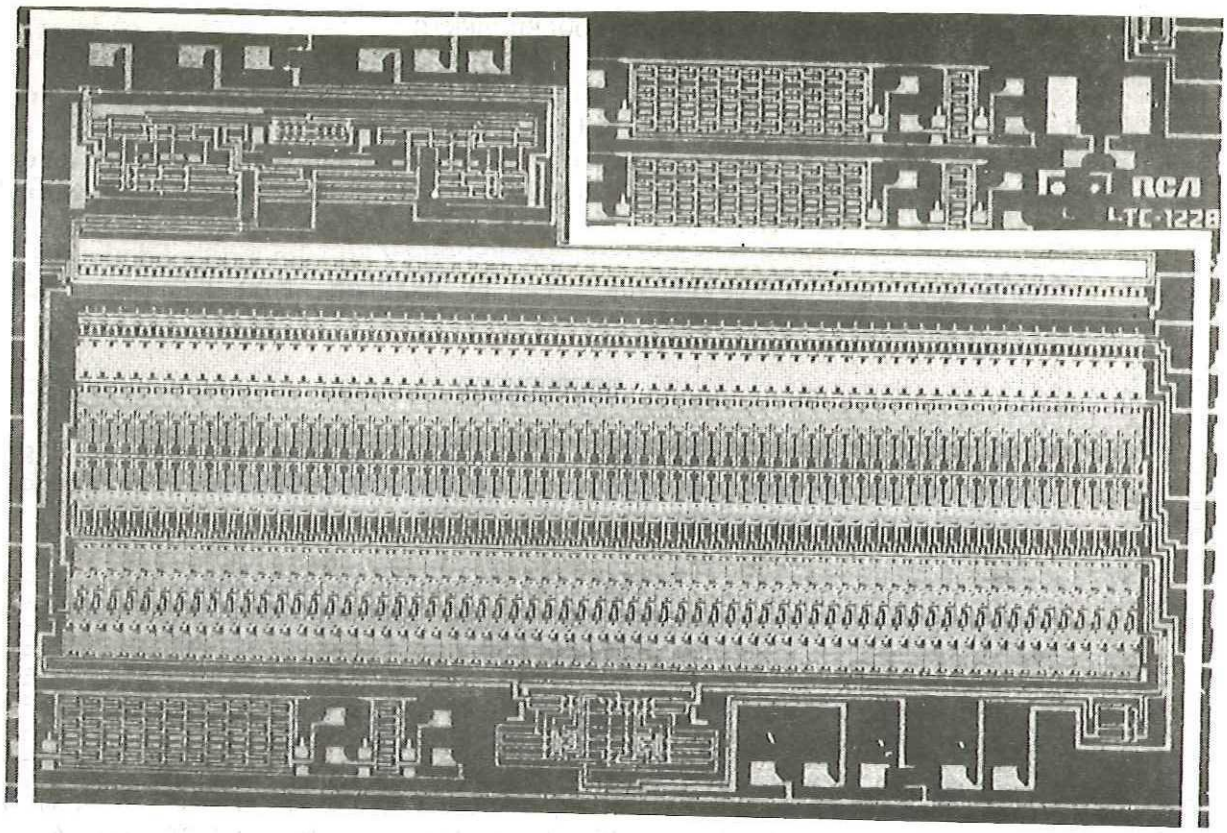
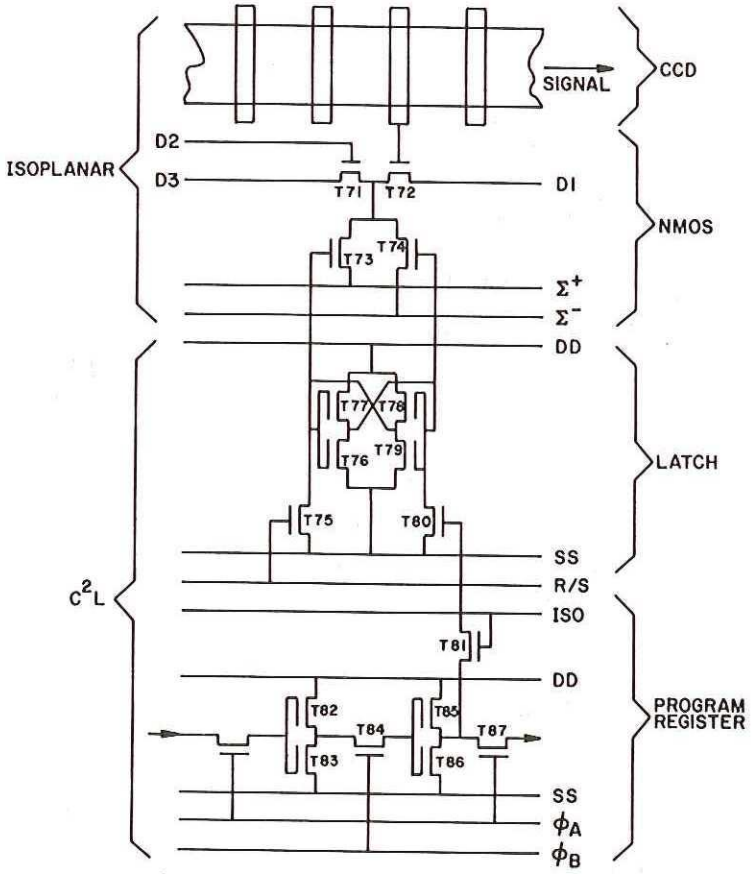


Figure 2



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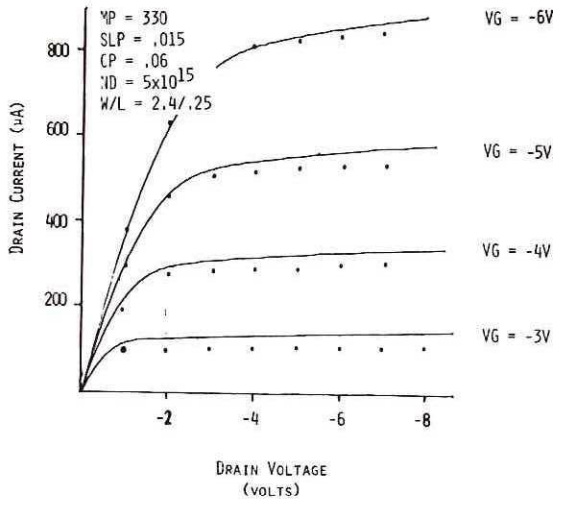
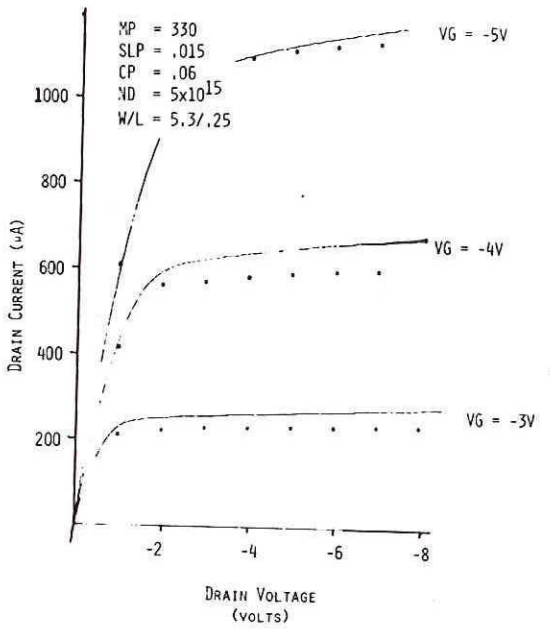
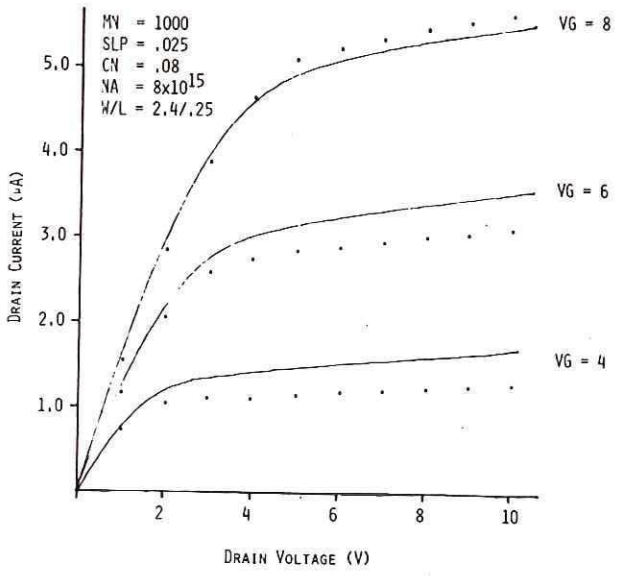


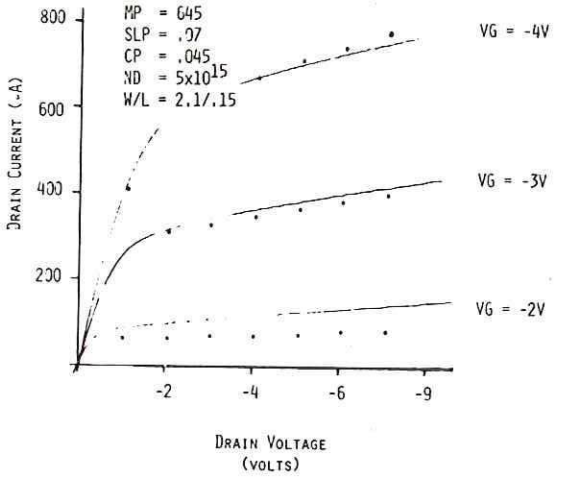
P-channel
L = .25 W = 2.4



P-channel
L = .25 W = 5.3



N-channel
L = .25 W = 2.4



P-channel
L = .15 W = 2.1

Figure 4

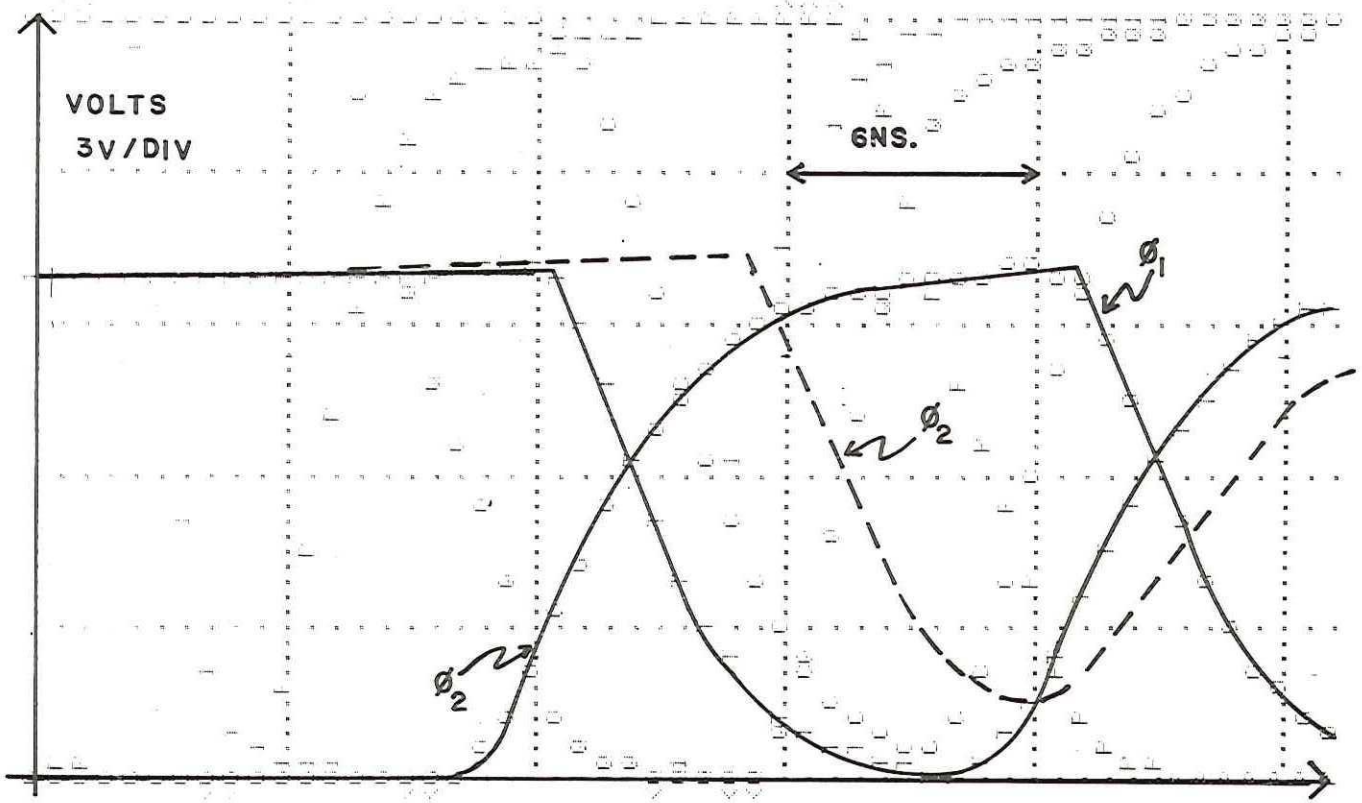
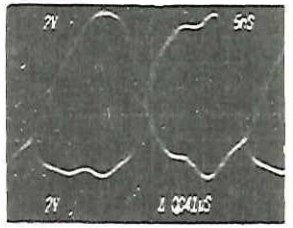
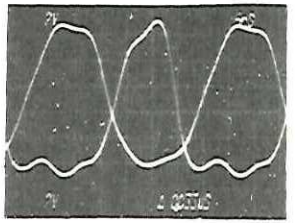


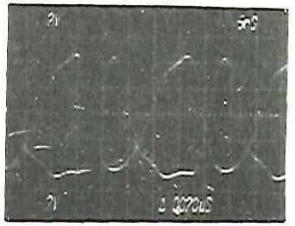
Figure 5



f_c = 24.4 MHz



f_c = 30 MHz



f_c = 50 MHz

Figure 6