APPLICATIONS OF HIGH SPEED CHARGE TRANSFER DEVICES

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ABSTRACT

This paper describes the application of high speed charge transfer device technology to the signal processing areas of spectrum analysis and correlation. The problems associated with operating sampling inputs for CTD's at very high frequencies are addressed. Split gate weight CTD's suitable for high speed CZT operation are described, along with a method for implementing an on-chip premultiplier in the charge domain. The design of a high speed CTD correlator is also described.

INTRODUCTION

The purpose of this paper is to discuss current and recent research on the applications of high speed charge transfer devices. The recent demonstration of GaAs CTD's operating at 500 MHz, complementing silicon CTD operation at 340 MHz, suggest that it is important to examine the feasibility of applying this technology to a variety of higher frequency requirements. Along with simply transferring charge, much interest has been focussed on the input sampling process itself, in order that linear, relatively large dynamic range input signals can be generated at higher speeds.

The primary applications that have arisen are analog delay lines for time expansion of signals, high speed digital CTD delays, spectrum analysis and correlation. In each case, the goal of device research is to improve the obtainable performance in each application area while reducing device complexity, power dissipation and the number of interconnections required.

Charge partition sampling has been described in several recent papers and has a demonstrated ability to generate signal packets at 200 MHz rates.[1] In order to obtain a sample of an input electrical signal which is characterized by a single frequency, it is necessary that the sampling aperture be as small as possible in order that phase variations during the sampling aperture do not average out the signal. Two factors (which are roughly additive) are known to degrade the performance of the charge partition input. The first factor is the time required for the partition gate to actually pinch off the sample. In the buried channel charge partition circuit, this is the time required for the rising partition gate potential to pass through the storage range and above the diffusion bias. This has the effect of greatly reducing the channel conductance in the channel region under the backflow gate.

Since the current flow through a MOSFET is exponentially reduced as gate bias V_g passes into pinchoff, the MOSFET conductance falls a factor of ten for every $2.3nkT/e$ that V_g moves (n is a structural constant $1 < n < 2$). If the response time of the sampler is raised to a value one hundred times greater than the sampling interval, for example, the effect that the input signal can have on the final sample is only one percent. Thus, if one requires ± one percent accuracy of sampled data, this level of pinchoff is all that is required. In order to obtain very high frequency response in a sampling input, it is necessary to drive the gate bias near zero with respect to the device substrate for maximum conduction.

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By then pushing the conductance even a few tenths of a volt past pinch-off, the device cuts off very abruptly, thus "sampling" the signal. Note that as the pinchoff gate voltage rises, no sampling occurs until the RC time is raised to perhaps one percent (1%) of the desired sampling aperture. By the same token, sampling is considered complete when the RC time constant is raised to 100X the desired sampling aperture, indicating that the sample process requires an excursion of conductance of four orders of magnitude or 9.2nkT/e, which is about 0.4 volts at 300°K. Thus, if a leading edge pulse excursion of perhaps 10v/ns is used, the gate induced sampling aperture will be 40 picoseconds.

Prior to sampling by raising the charge partition gate, changes in the signal voltage applied to the storage gate may have a reduced influence on the quantity of charge sampled. If the signal input, see Fig. 1, is incremented or decremented and if the adjacent charge is treated as a source/sink, then the average gate equilibration can be shown to be governed by

$$\Delta Q_s = C_g \Delta V_s \left[f(t, \tau_{th}, \tau_{SD}) \right]$$

For signal processing application, the well is operated nominally half-filled. This means that mutual repulsion or self-induced drift effects dominate the response time of the charge voltage fluctuations. The potential as a function of time is given by:(2)

$$\Delta Q_s = C_g \Delta V_s \frac{t}{t+\tau_{SD}} \qquad \text{where:} \qquad \tau_{SD} = \frac{2e\epsilon_s n_d L^2}{\pi \mu_n C_o^2 V_I^2} = \frac{\tau_{SDO}}{V_I^2}$$

If the input doping level is an implanted region with $n_d = 10^{16}$ cm^{-3} and if $L = px10^{-4}$ cm and $C_o = 10^{-8}$ f cm^{-2} and $\mu = 10^3$, then:

$$\tau_{SD} = 1.08 \times 10^{-10} \frac{p^2}{V_{IO}^2}$$

This data is plotted in Figure 2 . Note that operating out of the linear center range of the CCD buried channel input, particularly toward the nearly empty well region, seriously degrades sampling time. With respect to dynamic range, note that in most CCD designs, charge is stored in the channel up to about 2-3x10^{11} charges per cm^2. A one-micron long gate (L), with a width (Z) of 100 microns therefore can store about 2-3x10^5 charges with a potential SNR of 500. Note that at low temperatures, the value of μ increases for silicon and improves sampling time by a factor of ten at 77°K. Also note that using a 300°K GaAs mobility value of perhaps 6000 will reduce the values of storage time by a factor of six.

Since this sampler depends for its sampling accuracy only on the rising leading edge of the sample gate pulse, it is important that this pulse have the steepest slew rate feasible. Typically, values of a few volts per nanosecond can be obtained experimentally using test equipment pulse generators, and careful attention needs to be paid to this aspect of circuit development for fast sampling input circuits.

UTILIZATION OF HIGH SPEED CTD'S FOR SPECTRUM ANALYSIS

The most compact and simple method for performing spectrum analysis is the chirp-Z transform, since it utilizes essentially one processor to convert n successive time samples into n equally spaced fourier coefficients. But to use the chirp-Z transform at high speeds requires a capability to handle and transform a set of samples at high speeds as well. N-channel processing has been utilized to obtain 295-cell modified double overlapping gate CTD's. These devices have been recently described by G. Szentirmai[3], and were designed with sine-chirp and cosine-chirp weighting. The system that performs the CZT operation is sketched in Figure 3.

A feature of the sliding chirp-Z transform method over the standard one is that it operates continuously, while with the standard chirp-Z system we must wait N time slots with no meaningful output, after which we get N spectral line output and the cycle is repeated. Another difference between the two approaches is that any windowing (weighting w(n)) that is to be done must be done in the "prechirp" stage in the standard chirp-Z, and in the convolution stage (split gate weighting) in the sliding chirp-Z transform methods.

The main elements of this system are the four CTD's which perform the convolution of the prechirp-multiplied input signal with the fixed patterns $\overline{y}_R(n)$ and $\overline{y}_I(n)$. When:

$$\overline{y}_R(n) = w(n) \cos \frac{\pi X^2}{N}$$

$$\overline{y}_I(n) = w(n) \sin \frac{\pi X^2}{N}$$

The weighting factors w(n) are chosen to shape the spectrum in order to suppress unwanted sidelobes. Various families of windowing functions are known and they are well described in the literature.However, nearly all of them suffer from the disadvantage that the more they suppress sidelobes, the wider their main lobe becomes sometimes completely obliterating our ability to distinguish between signals in neighboring bins. The best compromise discovered to date[4] yields a sidelobe about 25 dB below the main lobe without changing the width of the main lobe at all. The corresponding window function is given by:

$$w(n) = A_0 + A_1 \cos X + A_2 \cos 2X + A_3 \cos 3X \quad N=0, 1, \ldots N-1$$

$$X = \frac{(n - \frac{N-1}{2})}{N}$$

where the coefficients were determined by computer optimization and are:

$$A_0 = 0.901326 \qquad A_2 = -0.016178$$

$$A_1 = 0.108034 \qquad A_3 = 0.006818$$

These coefficients were scaled so that the maximum value of w(n) is unity.

The final consideration is that of the value of N. Since our requirement called for a resolution of 256 bins, we need an N = 256. In order to provide a 15 percent guard band, we have increased this to N = 295 and, consequently, N_o = N-1/2 = 147.

Consider now the details of the charge-coupled devices. As mentioned above, the four-phase structure is the preferred one, since two metallization steps are sufficient to provide us with the required, slightly overlapping, set of gates. One of these four gates will be the split gate, and the location of the split will of course determine the gate weight in the standard way.

Although a four-phase gate structure is used, only three of the gates are clock-driven. In order to simplify the charge sensing at high frequencies, the split sensing gate is dc biased about halfway between the extreme voltages of the driven gates. As this reduces the charge handling capability of the sensing gate, the sensing gate width was selected to be twice that of the clock-driven gates.

The selected dimensions are as follows:

295-Cell Device

Channel Width	280 μm
Cell Length	20 μm
Gate Width	4 μm
Sensing Gate Width:	8 μm

For a buried channel device, it is necessary to provide a gap in the implant, then the effect of mask dimension errors upon W_m are straightforward to estimate. If, however, the metal gap and the implant gap are the same size and are misaligned, then two problems arise as shown in Figure 4 (b). First, a portion of the gate overlaps a portion of channel where no implant has been applied, leading to a region with zero mobile charge storage capacity. Second, a portion of the implanted region is not covered by any gate, forming a region which stores uncontrollably. Charge will be poured into this gap and transferred out by every transfer thus providing an unwanted charge sink and signal offset.

To solve this problem, the gate gap should ideally be defined by the ion implantation layer. As shown in Figure 4 (c) and (d), if the metal gap is made smaller than the ion implant gap, and if the metal gap is positioned within the implant gap, the weighting function obtained will be virtually invariant to positional errors of the two mask layers with respect to each other. Alignment of ion implant gaps relies on accuracy of mask positioning alone, and since a photoresist layer is used as the implant mask, the alignment may be extensively checked prior to implant with easy recourse to correction by the device processor until sufficiently accurate placement is achieved.

The location of the splits can be determined with a precision of about a 0.2μm. This yields a theoretical coefficient (quantization) error of less than 0.15 percent (which is more than adequate). Processing inaccuracies will increase this somewhat, but this is still not expected to create any problem.

Figure 5 is a photograph of the sine and cosine chirp split gate weighted CTD's.

Figure 6 shows a representative portion of the CTD cells, defining the cell, active electrodes and sense electrodes. The three active electrodes in each cell all receive properly timed three-phase drive signals whose rising and falling voltages cause moving potential wells

in the N-type silicon under these electrodes. Thus in principle, the chirp-Z transform can be performed to up to perhaps 250 or 300 MHz using existing CTD technology except for two specific problems:

1. Available external differential amplifiers cannot sample sufficiently rapidly to gather an accurate representation of the signal charge present on the CTD gate within the 5 nanoseconds that this signal charge is present on two-phase operation at ∿ 100 MHz. The problem is that of picking off the signal-induced charge from the two large CTD gate capacitances and differentiating the two responses sufficiently rapidly to provide an undegraded large dynamic range output from the device within the few nanosecond time period required. (Other workers have demonstrated buried channel single output charge transfer devices which are split gate weighted and can be used for fixed weight CZT application.[5])

2. Hybrid prechirp multipliers do not function well above 30 MHz.

In order to make the performance of the chirp-Z transform feasible above about 30 MHz, it is necessary to devise a scheme for increasing the speed at which the input chirp function is performed. Present chirp generators use PROM's to store the coefficients, DAC's to convert the digital coefficients to analog values, and fast multipliers to step-by-step obtain the product of the incoming signal and the chirp coefficients emerging from the generator. To circumvent this problem, consider the utilization of a CTD as the coefficient multiplier. CTD coefficient multipliers have previously been designed, built and demonstrated at frequencies up to 2 MHz (surface channel devices). Clearly we could use buried channel CTD's operating at frequencies of several hundred MHz.[6] This is shown in Figure 7.

Operation of the multiplier is as follows:

1. Charge signals propagate into the CTD multiplier device (which is a split-gate weighted CTD) so that as the charge packets pass under a particular gate with a coefficient split, the packets are essentially divided into two portions. Since the multiplier is a four-quadrant analog multiplier, two channels are required for bipolar operation.

2. Once the multiplier CTD is entirely filled with analog charge samples representing some function of time which is to be spectrum analyzed, the CTD multiplier stops.

3. Multiplication proceeds by removing all the charge on one side of the split and storing it in the buffer multiplexer CTD. This is done by lowering a barrier which removes the data on one side of every cell in both CTD's. If, for example, a charge Q_n is present under gate n, then if α_n is the fraction of charge removed (as defined by split), then the final charge signal in the buffer MUX after multiplication is $\alpha_n Q_n$.

4. Charge is now propagated out of the CTD multipliers multiplexer. It is already combined to form the product signal. The use of two CTD's allows this to be bipolar if the multiplier is configured as shown in Figure 7. Note that the input is inverted going into one device, and right side up going in the other. Also note that $W_n = \alpha_n - \beta_n = 2\alpha_n - 1$. Thus for α_n ranging between 0 and 1, the value of W_n ranges from -1 to +1.

Notice that the signal S_{in} is added to background level S_o in one channel but subtracted from S_o in the other channel of the multiplier.

Thus, only two channels and a signal offset are required to obtain a four quadrant multiplication. As shown in Figure 7 , the output in channel 1 is given by

$$S_1 = \alpha_n S_o + \alpha_n S_{in}$$

where: S_1 = signal in channel 1

S_o = offset signal level

S_{in} = signal input

α_n = splitting fraction for device 1

At the same time:

$$S_2 = \beta_n S_o + \beta_n (-S_{in})$$

β_n = splitting fraction for device 2

However, since $\alpha_n + \beta_n = 1$

$$\alpha_n - \beta_n = 2\alpha_n - 1 = W_n$$

$$S_T = S_1 + S_2 = (\alpha_n + \beta_n)S_o + (\alpha_n - \beta_n)S_{in}(nt_o)$$

$$= S_1 + W_n S_{in}$$

which is a valid result for positive and negative W_n or S_{in}. Thus, a method for performing multiplication in a CTD device on the same chip as the chirp convolver exists. One advantage of this method of multiplication is that the device can be used to process any bandpass or bandwidth that can be collected by the input CTD's prior to multiplication. It is not necessary, although desirable, that the fixed weight CTD's used for summing the responses are operated at the same rate. The bandwidth of these processors are therefore given by the operating frequency of the sampling CTD. The CZT is basically an n to k transducer, displaying the successive DFT contributions of a CZT processor. Its DFT is equally correct for samples gathered rapidly or slowly until the processor is full. Its overall bandpass is governed by the clock frequency of the input multiplier. Its time-bandwidth product, however, is a function of the number of cells present in the CZT chirp CTD's. In this continuous mode of operation, input samples will be sampled into the multiplier by a fill-and-spill operating in charge partition mode.

The accuracy required, (or equivalently the fraction of charge left behind in each parallel bucket transfer), must be on the order of 10^{-3} in order to be of interest for high accuracy weight generation. The time required to attain this accuracy in multiplication is primarily governed by thermal diffusion. We shall therefore briefly treat the thermal diffusion case as a means of estimating required transfer times.

In the multiplier application, the most severe case occurs when an α_n or β_n occupies or reaches across the entire channel, i.e. goes to 1.

The maximum value of W then would be the entire channel width. The fraction of charge left behind is given by:

$$F = \frac{8}{\pi^2} \sum_{\text{odd } n} \frac{1}{n^2} \exp \left[- \frac{Dn^2\pi^2 t}{4w^2} \right] \approx 0.813 \exp - \frac{t}{t_D}$$

where: w = gate length

t = time

$t_D = 4w^2/D\pi^2$

must be less than 10^{-3}.

This occurs, for D=25, (for electrons in silicon), in a time of:

$$t = 0.107\ w^2$$

where w is the maximum channel width in cm. If, for example, each CTD channel were 5×10^{-3} cm wide, the equilibration time would be 2.5 microseconds. The entire processor cycle time would then be 5.0 microseconds. This could be directly utilized to build 200 MHz sampling rate multipliers with 500 values in each half, for a total of 1000 points, i.e. 200 KHz resolution.

HIGH SPEED ADJUSTABLE WEIGHT CCD CORRELATORS

The basic correlator function, i.e. of processing two input signals in such a way as to obtain the integral in some range of the product of the two functions, can also be done by high speed CTD's.

The product function can be derived in various ways: (1) floating gate sensing using MOSFET multipliers with adjustable coefficients; (2) feed-forward fill-and-spill input structures.

FLOATING GATE SENSORS

Floating gate sensors have already been demonstrated to function well at 10 MHz and above.[7,8,9] Floating gate sensors have been used to fabricate transversal filters, using the high speed n-channel CTD technology. Typically, these devices operate by permitting an image of a charge packet stored under the floating gate sensor to be generated on the gate of a small MOSFET adjacent to the channel. This charge gives rise to a voltage signal on the MOSFET gate. The reference function may be supplied electrically in the form of a set of bias voltage variations applied between the source and drain of each FET.

Filters of this type have been utilized to form very long processors, but these devices utilize the CTD only as a means of achieving the proper delay prior to each multiplication.

One basic difficulty with increasing the operating frequency of this circuitry is the parasitic coupling of floating gate FET's to other CCD gates. To some extent, this can be overcome by a feed-forward structure.[10]

FEED-FORWARD IMPLEMENTATION

From the point of view of optimizing correlation performance at high speeds, the feed-forward implementation shown in Figure 8 has the following features:

1. A parallel set of inputs, weighted ± 1, insert charge into the CCD channel. The CCD only transports the inserted charge. In doing so, it serves both as a delay line and summing buss for the transversal filter.

2. Using the charge partition input, a linear charge vs. voltage response up to high frequencies can be obtained. Input accuracy is the dominating factor for filter weighting accuracy.

3. Since the filter "output" is a charge packet, not a sum of sensed voltages on MOSFET's, the MOSFET nonlinearity and nonuniformity problems are side-stepped.

4. The charge domain "sum of products" can be utilized on-chip to perform further filter functions.

5. This method does cause the stored charge to build up linearly as a function of the number of taps, and therefore, it is only useful with large dynamic range for comparatively short filters. To build-up dynamic range and CTE, four-phase push clock drivers have been selected.

Rockwell is at present fabricating a silicon chip with four correlating CCD's. Each correlator CCD has 64 cells and 16 equally spaced input taps. Each tap is adaptable or readily reprogrammable in the sense that its essentially digital weight is provided by a digital shift register and latch which will be reprogrammable as fast as the chip can be emptied of one signal charge pattern and loaded with another. Thus, if 40 MHz is the CCD speed, then the chirp digital register speed will be 20 MHz. This rate does not seem to be compatible with NMOS shift register structures, and thus the digital register in this chip has been selected to be a floating diffusion output sensor CTD as shown in Figure 9 . For the digital application, output nonuniformity will not be a serious problem. Also the floating diffusion need not function rapidly since the digital register CTD can be halted to set the latches. Latches have been included in this design primarily to meet some requirements imposed by a variety of potential users that the weights, once programmed, be maintainable for long times. Thus, CMOS latches have been included to set every tap. CMOS was selected to reduced on-chip power dissipation in the infrequently reset but numerous latches.

The overall layout of the correlator is shown in Figure 10. Four CTD's are used in feed-forward mode rather than two to provide a separate collection channel for each of the four suboutputs. Another feature of the design is that the selectable BPSK/MSK/PSK chip correlator was not performed prior to correlation but afterward. Mathematically, for this application it provides an equivalent result. In the front location, the switchable filter is difficult to implement on-chip. It requires a four-tap adjustable weight transversal filter with which is awkward to implement because of the necessary charge-to-voltage-to-charge conversions. But located at the end of the correlator, this filter is implemented with a charge domain input and four parallel outputs offset one cell each and gauged together, as shown in Figure 11. Cascading of these filters is achieved by offsetting the filter segments in time. This can be achieved using CTD's or SAW's as delay lines to provide the proper delay to match adjacent segments of the stored reference signals. Because of the fact that only CTD cells and charge partitioning high speed fill-and-spill inputs are utilized, it appears that these devices will operate at very high speeds.

CONCLUSIONS

Although much more effort is required to complete the design and characterizations of the devices described herein , the high speed CTD has already been applied to several problems, and preliminary results appear encouraging. In the areas of spectrum analysis and correlation, methods of improving the performance of existing CTD's have been described to permit the extension of the applications at least into the 100-200 MHz range.

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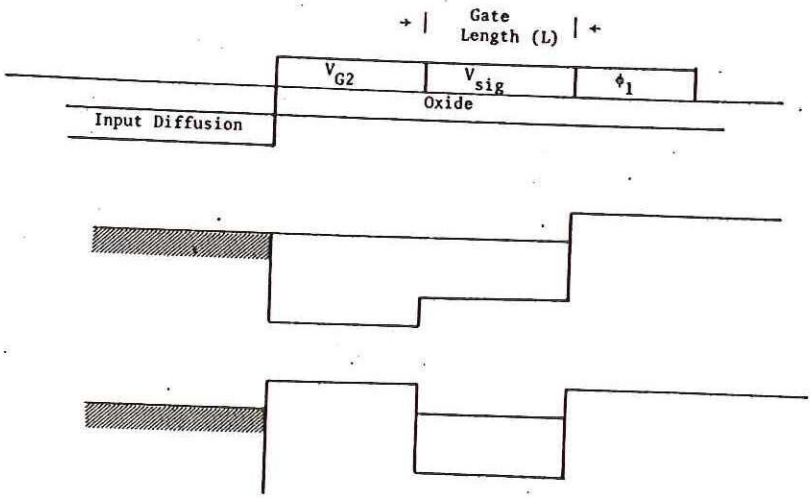


Figure 1. Operation Fill-and-Spill as Charge Partition Input

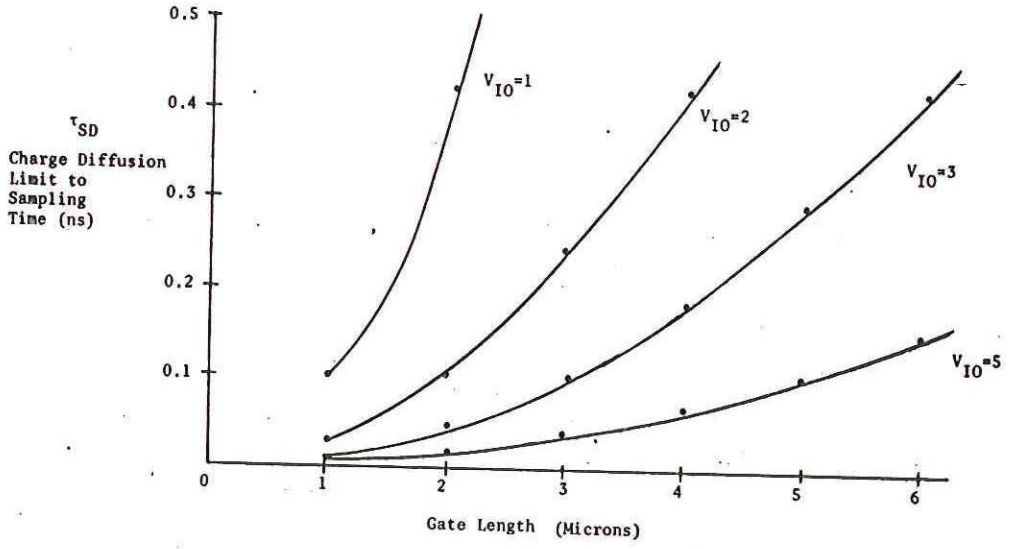


Figure 2. Charge Diffusion Contribution to Sampling Time Plotted as a Function of Gate Width and Well Storage Depth at Reference Level V_{IO}

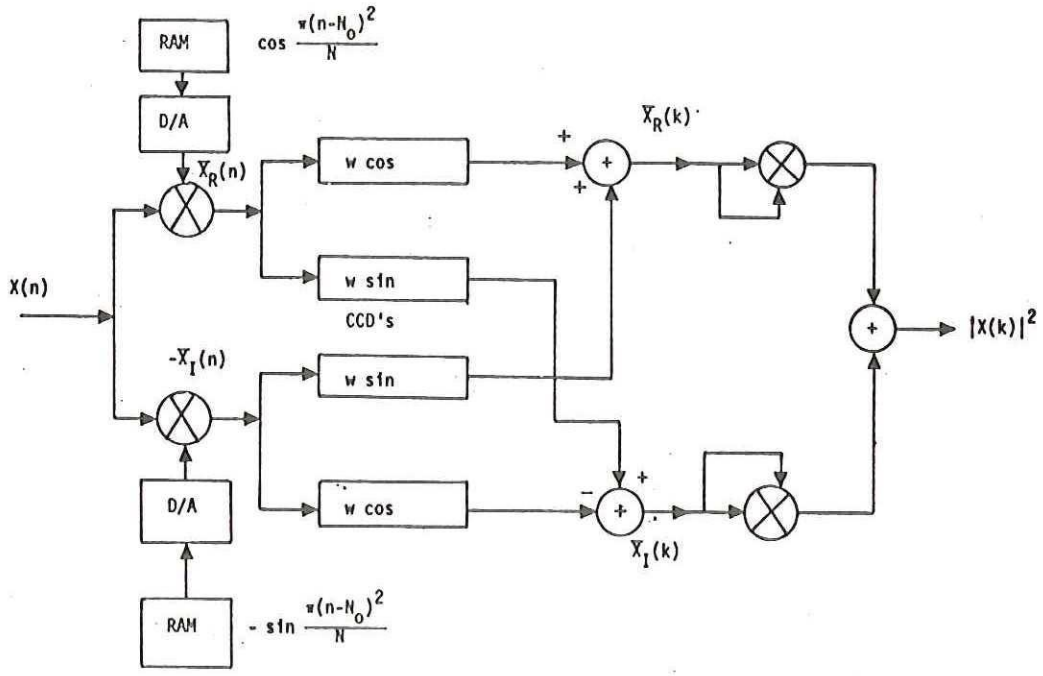
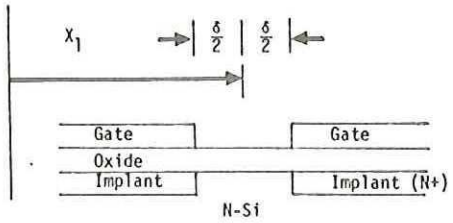
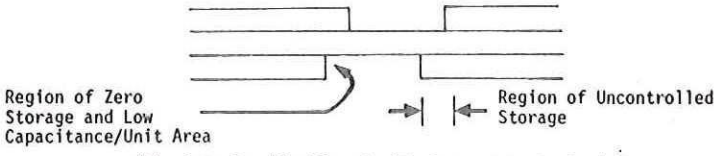


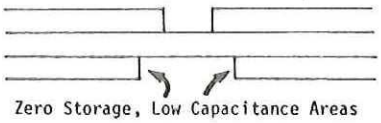
Figure 3. Chirp-Z Transform Block Diagram



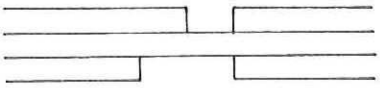
(a) Gate Gap and Implant Gap Properly Aligned



(b) Gate Gap Misaligned with Respect to Implant Gap



(c) Gate Gap Properly Aligned but Much Smaller than Implant Gap



(d) Gate Gap Small and Improperly Aligned, but Containing Negligible Total Inaccuracy

Figure 4. Along Track Cross-Section of Gate Gap of Fixed Gate Weighted PCCD

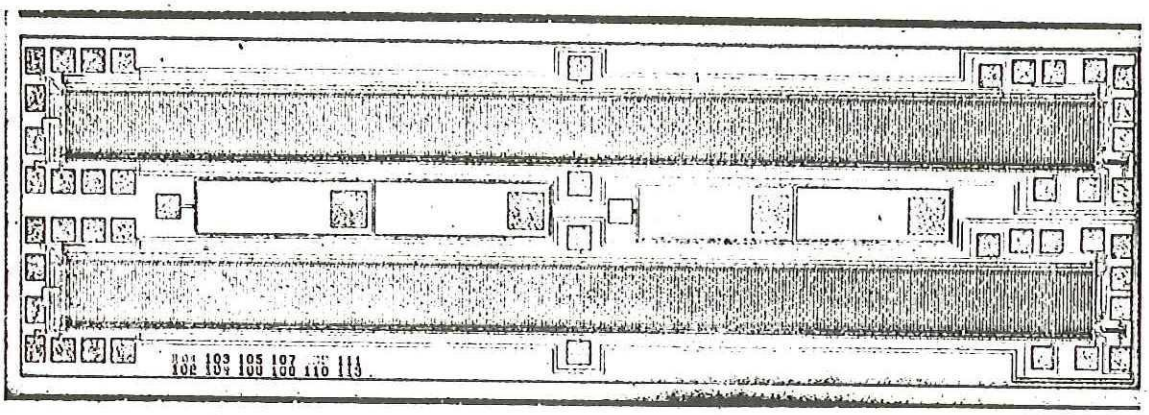
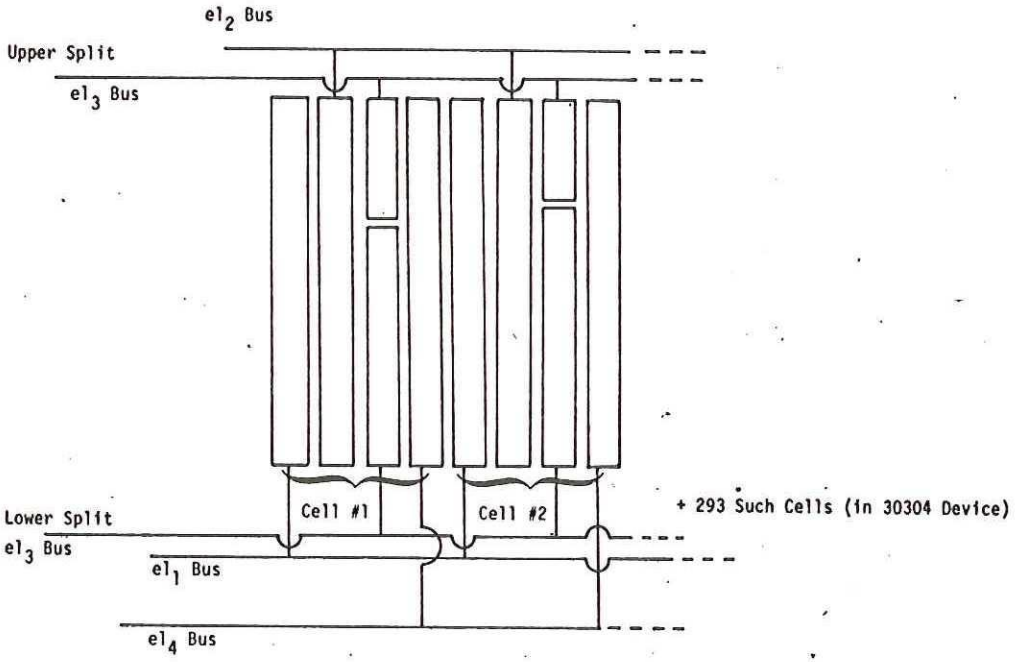


Figure 5. Photograph of Sine and Cosine Chirp Split-Gate Weighted CTD's



There is actually overlap.

Electrodes 1 & 3 are in the lower level.

Electrodes 2 & 4 are in the upper level.

Figure 6. Schematic Layout Showing Relationship Between Active (Driven) and Passive (Sense) Electrodes

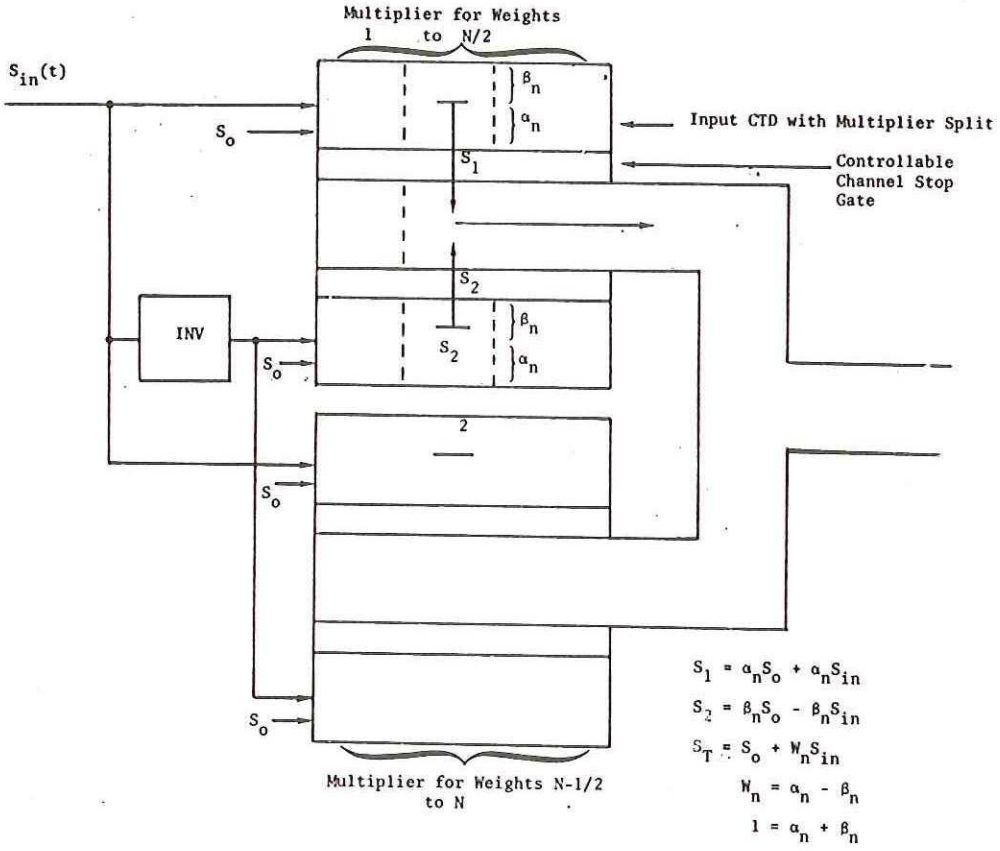


Figure 7 . Block Diagram of CTD for Continuous Operation as Repetitive Fixed Weight Function Four Quadrant Multiplier for N Points

Figure 8. High Speed CTD Feed-Forward Transversal Filter

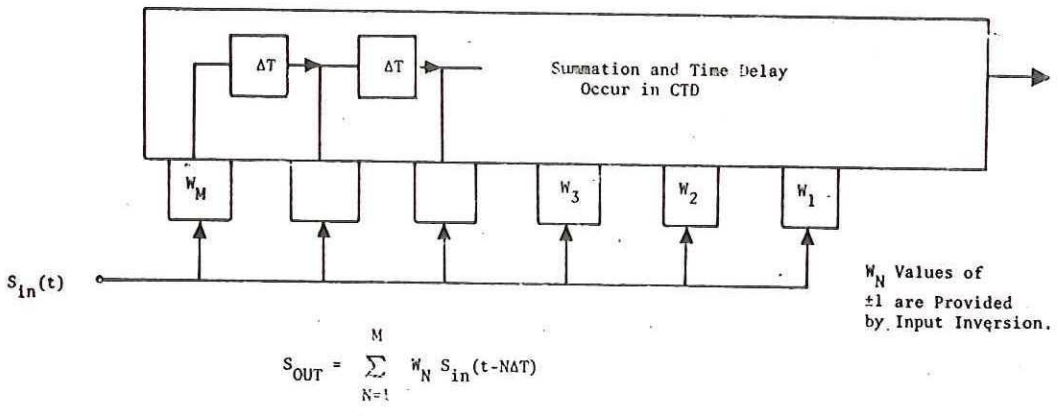


Figure 9 . Block Diagram of Digital Register/Correlator Interface

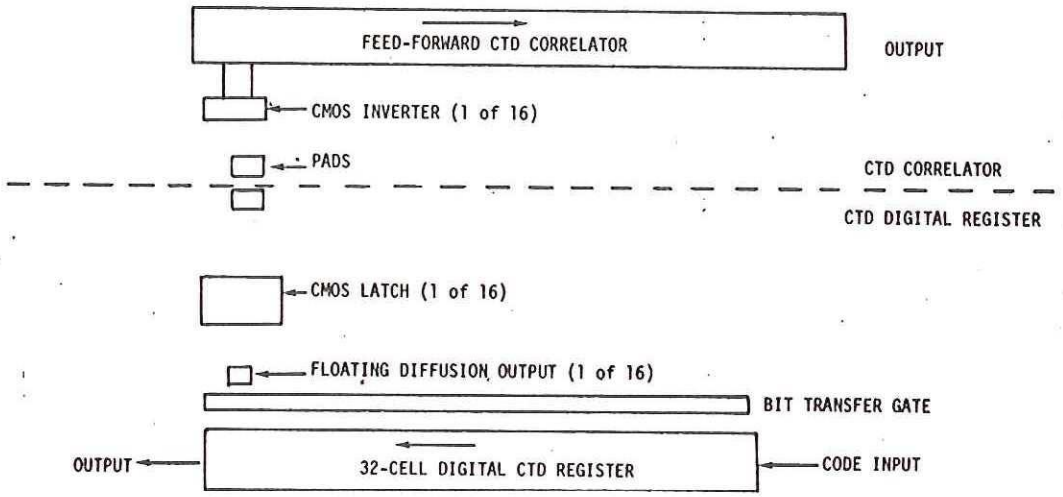
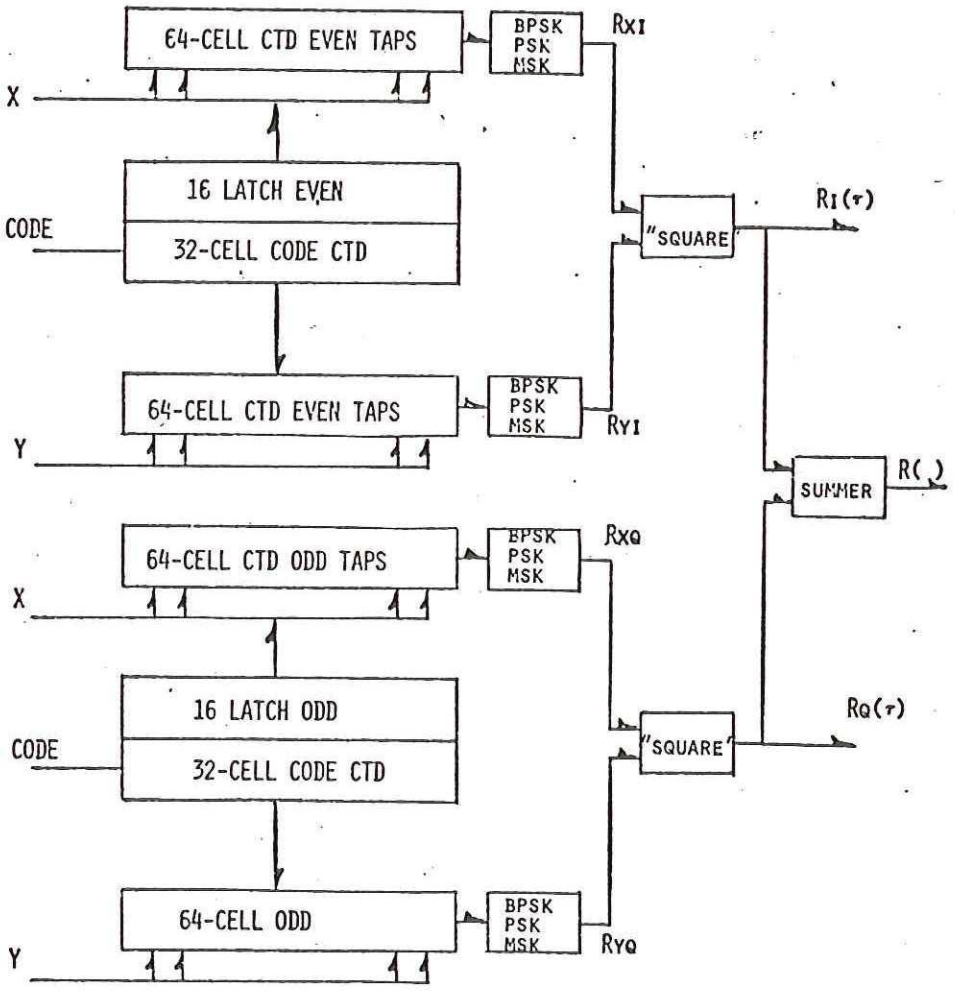


FIGURE 10. CORRELATOR LAYOUT



DELAY LINES FOR X AND Y INPUTS TO CASCADED UNITS NOT SHOWN

Figure 11. BPSK, PSK and MSK Chip Filter Mechanization