COMPARISON OF SWITCHED-CAPACITOR LADDER AND CCD TRANSVERSAL FILTERS

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I. INTRODUCTION

Switched-capacitor ladder filters and CCD transversal filters have developed into two competitive approaches for implementing high performance filters which can be fully integrated using MOS-LSI technology [1,2]. In some respects the two techniques are similar since they are both analog sampled data filters which make use of charge storage on capacitors. However, in most other aspects, they are fundamentally very different since CCD transversal filters use only transfer function zeros to shape the frequency response, whereas the switched capacitor ladders are recursive filters which make use of both poles and zeros. For some applications a transversal, all zero filter must be used, such as when true linear phase is required or in matched filtering. On the other hand, a very narrow bandpass filter can be realized using a simple pair of high Q poles, which is much more efficient than using a CCD transversal filter which would require a large number of zeros and therefore many CCD stages for a narrow passband response.

It is not the intention of this paper to explore the tradeoffs between the use of poles and zeros to implement a given transfer function, but rather to investigate the peak performance to be expected for a frequency response which can be reasonably realized (in terms of silicon area) by either approach. The filter response will be a 3.1 KHz lowpass filter which is similar to that required for anti-aliasing in a PCM telephone system. The switched-capacitor implementation to be investigated will be a 5 pole, 4 zero elliptic filter and the CCD filter will use the split electrode approach with 64 stages. Both filters will be designed to have a passband response of $\pm$ .032 dB with a stop-band rejection of 32 dB. The performance characteristics of thses two filters will be compared after a brief discussion in the next section of the particular high performance implementations which are to be considered.

II. CCD TRANSVERSAL FILTERS

In the last few years researchers have developed new techniques to implement CCD filters which are optimized for differing performance requirements. In almost all cases, however, the basic structure is a transversal filter. The expression which describes the operations of an N stage filter is

$$V_{out}(n) = \sum_{m=0}^{N-1} h_m V_{in}(n-m) \qquad (1)$$

where $V_{out}(n)$ and $V_{in}(n-m)$ are the nth and (n-m)th time sample of the

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output and input signals, respectively. By taking the discrete Fourier transform of this expression the transfer function of the filter can be found

$$H(\omega) = \sum_{n=0}^{N-1} h_n e^{-j\omega n T_c} \tag{2}$$

where T_c is the sampling period. As can be seen from this equation, the frequency response has a periodicity equal to the sample rate, which requires that the input signal be bandlimited (anti-aliased) to avoid spurious responses. The design problem of determining an optimum set of coefficients which provides the closest approximation to a desired frequency response has basically been solved. There are several computer programs that are available which can very efficiently perform this task [3].

An an example of the tradeoffs involved in the design of transversal filters, the design of a simple low pass filter will be discussed. If δ_1 and δ_2 represent the desired magnitude for the passband ripple and stopband rejection and Δf is the frequency width of the transition between the passband and stopband regions, then N the minimum number of weighting coefficients to achieve this response is given by [4]

$$N = \frac{-10 \log_{10}(\delta_1 \delta_2) - 15}{14\ \Delta f / f_c} \tag{3}$$

Therefore, if a very sharp transition band is required (relative to the clock rate), the number of weighting coefficients can be very large. Fortunately, large numbers of tap weights are readily achievable because of the density of the CCD structure.

It is apparent from the above discussion that in order to achieve the sharpest possible transition band it is desirable to have the band-edge as near as possible to the sampling frequency. This, however, increases the sharpness of the bandlimiting prefilter which is required to avoid aliasing of the input signal, when it is sampled at the input to the CCD. A design tradeoff must therefore be made between the length of the CCD filter and the complexity of the anti-aliasing prefilter. For the 3.1 KHz lowpass under consideration a choice of 64 stages implies a clock rate on the order of 32 KHz (using Eq. (3)).

There has been extensive work in various techniques for implementing a transversal filter using charge transfer devices. In many respects the highest performance has been obtained from the split electrode approach shown in Fig. 1. (Additional clocking electrodes for transferring the signal charge are not shown [2,4,5].) The basic structure is a CCD delay line which has one of the electrodes in each stage split into two or three parts [3]. As charge transfers under these sensing gates, which are attached to positive and negative sense lines, the displacement charge is sensed by the charge integrating operational amplifiers connected to each sense line. The value of the weighting coefficient is realized directly as the size of the portion of the sense gate which extends over the channel; except for a small segment which is always left on the other side of the channel to insure that any edge effects due to fringing fields at the sides of the channel will be cancelled out. This cancellation is performed in the third operational amplifier which forms the difference between the two sense lines which

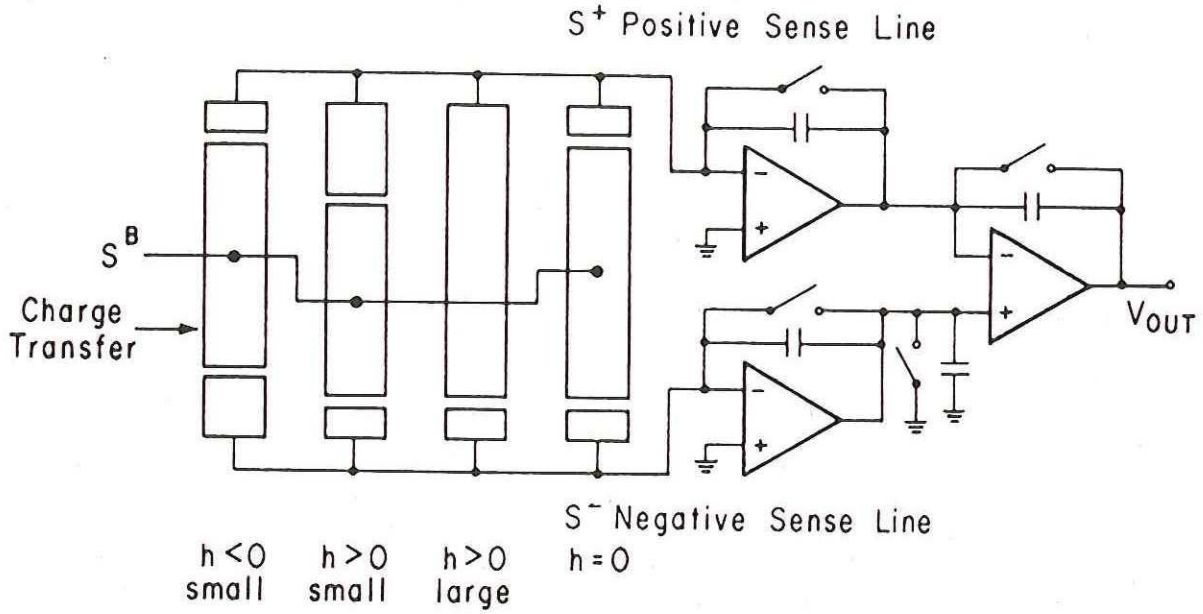

Fig. 1. Double-split-electrode transversal filter.

is required to obtain positive and negative weighting coefficients. An important advantage of this "double split" approach is that small weighting coefficients can be realized without limitations of earlier techniques [5]. The buffer electrode in the center of the double split gates, S^B, keeps the total capacitances of each sense gate constant. Also shown in this figure is a more conventional single split electrode gate which implements a large positive coefficient since the single split technique is more efficient in silicon area.

III. SWITCHED CAPACITOR FILTERS

A possible approach to monolithic filters would be to attempt to integrate in MOS technology conventional RC active circuits. However, this is not possible because of the necessity of accurately defining resistance-capacitance products, which requires that the absolute value of the resistors and capacitors be well controlled. Typical variations in an MOS process yield variations of these parameters on the order of $\pm$ 20%. Also the area required to implement resistors and capacitors which yield RC products that are needed for audio frequencies are prohibitively large.

A circuit that performs the function of a resistor which when used with capacitors that do not have these disadvantages is shown in Fig. 2(a). The operation of this "resistor" is as follows: the switch is initially in the left-hand position so that the capacitor C is charged to the voltage V_1. The switch is then thrown to the right and the capacitor is discharged to the voltage V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C(V_2-V_1)$. If the switch is thrown back and forth every T_c seconds, then the current flow, i_s into V_2 will be

$$i_s = \frac{C(V_2-V_1)}{T_c} \qquad (4)$$

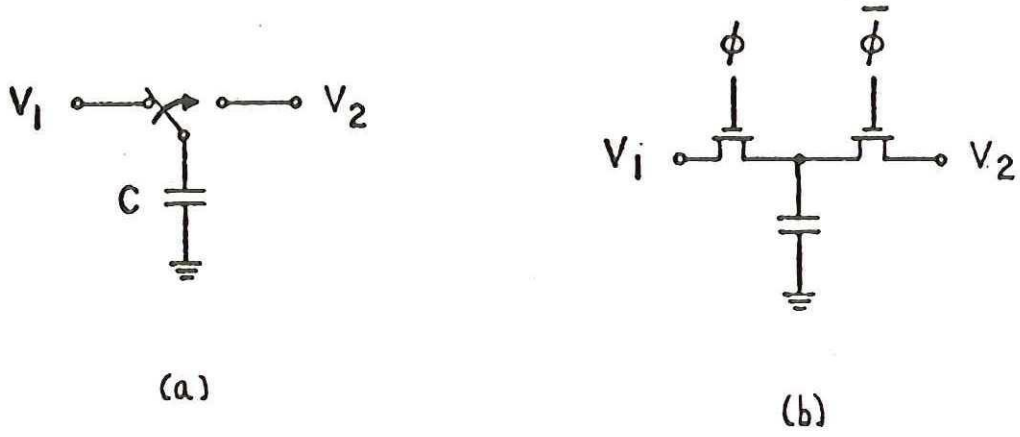

Fig. 2(a). A switched-capacitor resistor.
Fig. 2(b). The MOS implementation.

Thus the size of an equivalent resistor which would perform the same function as this circuit is $R = T_c/C$. The MOS realization of the circuit of Fig. 2(a) is shown in Fig. 2(b). The two MOSFET's are operated as switches which are pulsed with a two phase nonoverlapping clock (ϕ and $\bar{\phi}$) at a frequency f_c. The most important advantage of the switched capacitor resistors is the high accuracy of RC time constants that can be obtained with their use. If a capacitor C_1 which is switched at a clock rate of f_c is connected to a capacitor C_2 the resultant time constant of this RC network τ_{RC} is approximately

$$\tau_{RC} \approx \frac{1}{f_c} \quad \frac{C_2}{C_1} \tag{5}$$

For a given clock rate the value of τ_{RC} is therefore determined by a ratio of capacitor values which makes it insensitive to most processing variations.

The problem of implementing active filters in MOS technology is thus reduced to the question of what kind of active filter should be used. The filter configuration chosen is the analog computer simulation of the equations which describe a passive doubly-terminated RLC ladder. These filters are called "leapfrog" or "active ladder" filters in the active filter circuit literature and are closely related to wave digital filters in the digital signal processing literature.

The basic building block of these filters is a differential integrator and summer which is shown in Fig. 3(a) that is implemented in the conventional way with resistors and capacitors. The equations which describe this circuit are

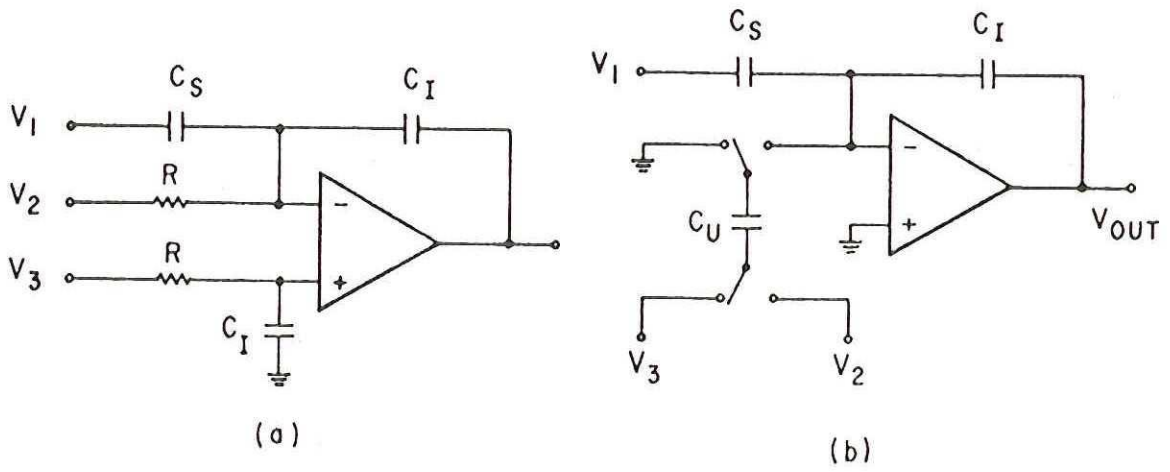

Fig. 3(a). An RC integrator/summer.
Fig. 3(b). The switched-capacitor implementation.

$$V_{OUT}(\omega) = -\frac{C_S}{C_I} V_1 + \frac{1/RC_I}{j\omega}(V_3-V_2) \tag{6}$$

Straightforward substitution of the resistors by the circuit in Fig. 2 would yield a switched capacitor circuit that is sensitive to parasitics, so an alternate method of realizing the resistors which also makes it possible to invert the sign of the signal is used and is shown in Fig. 3(b) [7-9]. The circuit in this figure is described by the following z-transform equation

$$V_{OUT}(z) = -\frac{C_S}{C_I} V_1 + \frac{C_u/C_I}{1-z^{-1}}(z^{-\frac{1}{2}}V_3-V_2) \tag{7}$$

Appropriate interconnection of these sampled data integrators following the RLC prototype yields the parasitic free fifth order switched capacitor ladder shown in Fig. 4. The capacitor ratios which are used to implement this filter are obtained by transforming the L and C values which can be obtained from standard tables [10]. The capacitor ratios for a 3.1 KHz cutoff with a sample rate of 128 KHz are as follows:

$C_2/C_1 = 8.470$ $\quad$ $C_2/C_4 = 2.042$
$C_6/C_5 = 5.043$ $\quad$ $C_{10}/C_7 = 3.546$
$C_{10}/C_9 = 14.707$ $\quad$ $C_{10}/C_8 = 10.445$
$C_{12}/C_{11} = 6.874$ $\quad$ $C_{15}/C_{13} = 3.791$
$C_{15}/C_{14} = 5.338$ $\quad$ $C_2/C_3 = 7.470$
$C_{15}/C_{16} = 5.338$

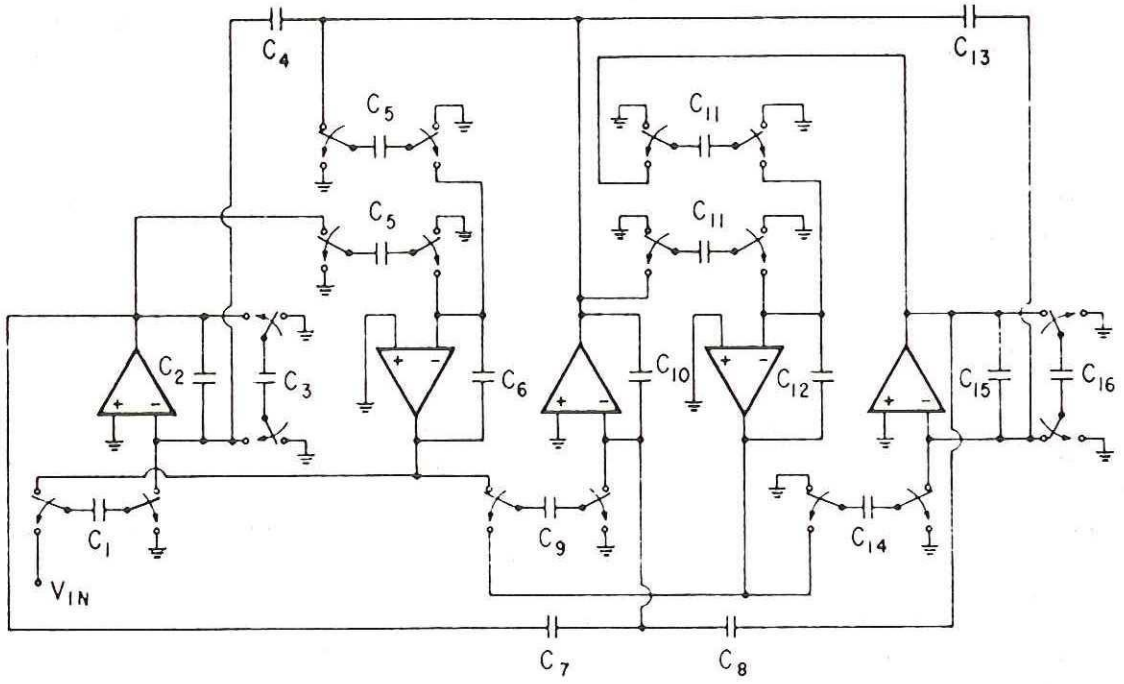

Fig. 4. Switched-capacitor implementation of a fifth order elliptic lowpass.

IV. PERFORMANCE CHARACTERISTICS

A. Response Accuracy

In both the CCD and switched-capacitor approaches the precision coefficients which determine the frequency response are obtained from ratios of capacitance areas. In the case of the CCD's the capacitance area is determined by splits in the sense electrodes as shown in Fig. 1. Since the outputs of the CCD filters are sensed differentially, edge effects associated with the CCD channel sides can be cancelled out. Also the effect of parasitic capacitances on the sensing lines which would degrade accuracy is minimized in the circuit of Fig. 1 by keeping the sense electrodes at virtual grounds.

In switched-capacitor filters the capacitors are not always kept at a virtual ground and since the signal is not sensed differentially, special consideration must be given to insure high accuracy in the response. However, it is possible by taking appropriate care in layout of the capacitors (e.g. constant perimeter to area ratio) as well as proper circuit configurations such as shown in Figs. 3 and 4 to obtain filter responses which are independent of parasitic capacitances and edge effects. Therefore by taking proper precautions in both approaches extremely high accuracy capacitor ratios (and therefore filter coefficients) can be achieved. The limiting accuracy for both techniques is probably then due to photolithographic quantization. This tends to be more damaging to the CCD filters because the transverse filter weighting coefficients vary over a wide range (from .001 to .2 in our example) and thus a fixed quantization interval will result in large percentage errors for the smallest coefficients. The switched-capacitor integrator ratios vary over a much reduced range (in our example from 2 to 15) and since each pair of capacitors can be independently optimized the ratio errors

are fractionally approximately constant, i.e., there is a constant percentage error for all the coefficients.

The effect of tap weight quantization errors on CCD transversal filters can be determined by defining a fixed coefficient error Δ_m where

$$h'_m = h_m + \Delta_m \tag{8}$$

in which h_m is the desired weighting coefficient and h'_m is the actual value including process limitations. From Eqs. (1) and (8) we obtain

$$V_{OUT}(n) = \sum_{m=0}^{N-1} h_m V_{IN}(n-m) + \sum_{m=0}^{N-1} \Delta_m V_{IN}(n-m) \tag{9}$$

which can be interpreted as two parallel transversal filters. One has the ideal response while the other has the values of the errors, Δ_m, as weighting coefficients. Since these errors are in general random the frequency response of the error filters is relatively flat with an amplitude proportional to an rms average of the coefficient errors. Thus these random errors result in a fraction of the input signal in the output which is unfiltered. This signal sets a lower limit on the stop band rejection (typically about -50 dB) as well as add ripple to the passband region.

The analysis of the effect of quantization error on the response of a switched-capacitor ladder is much more complex since these filters are based on RLC prototype circuits which are designed for maximum power transfer between the source and load. For those points where maximum power transfer exists the RLC prototype has zero sensitivity to first order variations in the filter element values. Since there is a one to one correspondence between the capacitor ratios in the switched-capacitor ladder and the RLC parameters the response exhibits very low sensitivity to errors in the capacitor ratios.

In Fig. 5(a)-(d), the designed response and that with a 1% weighting coefficient error for both filters are shown. The CCD transversal filter is quantized with a quantizing interval equal to 1% of the largest coefficient value whereas the switched capacitor ladder is assumed to have a constant 1% error for all the coefficients. In both cases, the filters have a designed passband ripple of 0.064 dB and a stopband rejection of 32 dB, with the lowpass cutoff at 3.1 KHz. With a 1% weighting coefficient error, the CCD filter shows a passband ripple of about 0.14 dB and a stopband rejection of only 25 dB. For the case of the switched-capacitor filter, the passband ripple becomes 0.09 dB and the stopband rejection is virtually unchanged, i.e. 32 dB. In addition, the CCD filter shows a widening of the transition region whereas the switched-capacitor filter has no such tendencies. Thus, the switched-capacitor ladder exhibits a much lower sensitivity to coefficient errors than the CCD filter.

B. Noise

A critical parameter in many filter applications is the noise performance. There are a variety of noise sources in a CCD which include the input voltage to charge conversion (which yields an rms noise of 64 μv for a 1 pf input capacitance); the surface state trapping in the CCD channel on the order of 80 μv for a 64 stage CCD [6]), and the output amplifier noise. The wideband output circuit noise is found by multiplying the equivalent input noise of the op amp sensing signal charge (which for MOS op amps is typically on the order of 50 μv) by the noise

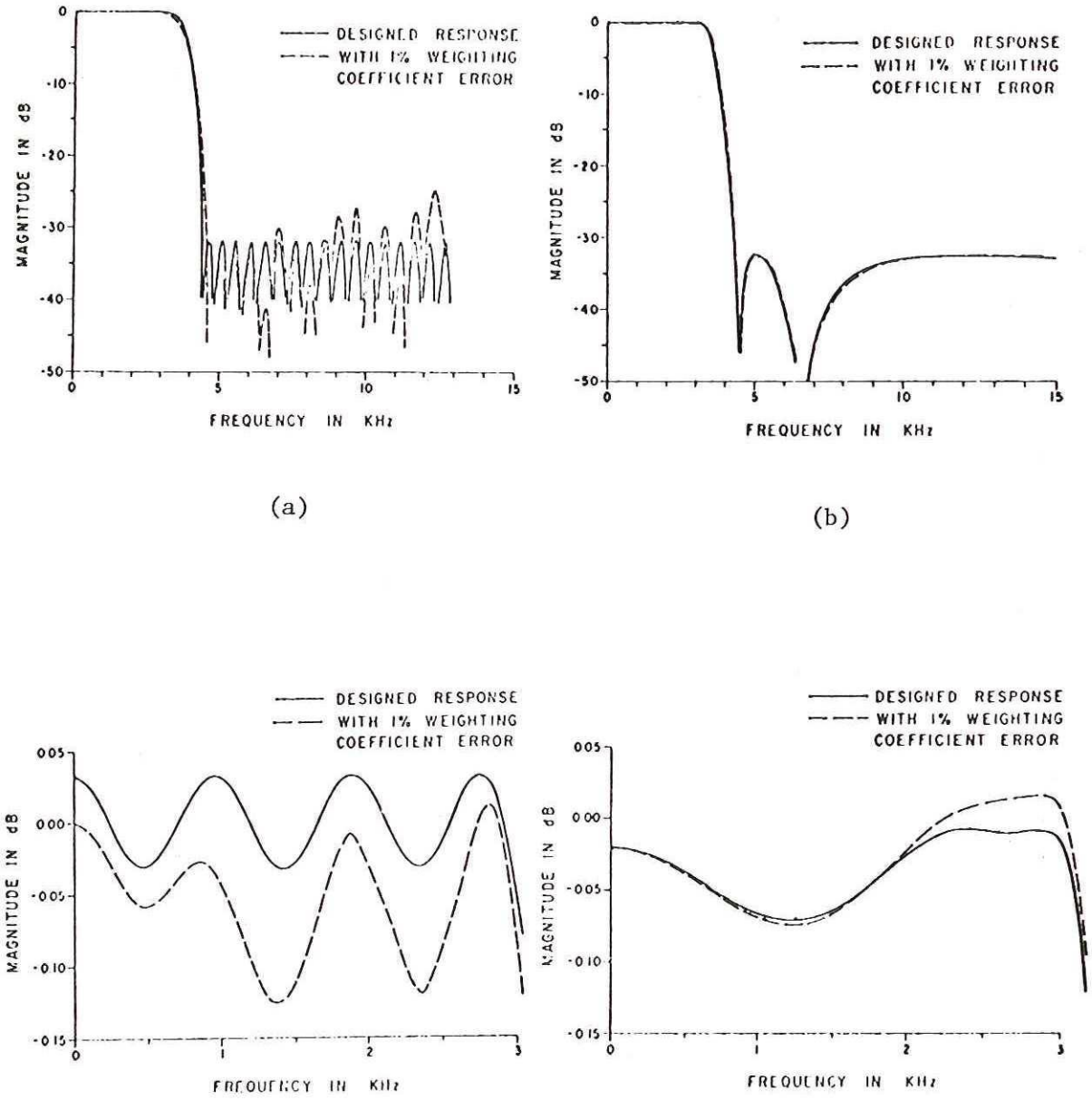

Fig. 5(a). Overall response of CCD filter.
Fig. 5(b). Overall response of switched-capacitor filter.
Fig. 5(c). Passband response of CCD filter.
Fig. 5(d). Passband response of switched-capccitor filter.

gain of the circuit. The noise gain is the total capacitance seen at the op amp input divided by the feedback capacitor which yields a ratio on the order of 5 for a lowpass filter of the type in Fig. 1. Since there are two op amps (one on each sense line) that contribute equally to the noise the total RMS noise, $v_{rms} = 5 \times \sqrt{2} \times 50\ \mu v = 350\ \mu v$. Since this noise is effectively sampled by the resetting switch, the relationship between noise spectral density $u_n(f)$ volts/Hz 1/2 and rms noise is given by

$$v_{rms}^2 = 2 \int_0^{f_c/2} v_n^2(f)df.$$

If it is assumed that the spectral density of the noise is white (independent of frequency) then the relationship between v_{rms} and v_n is

$$v_n(f) = \frac{1}{f_c}^{1/2} v_{rms}$$

For the filter response of Fig. 5(a) the clock rate is 32 KHz which yields a spectral density U_n = 2 μv/$\sqrt{Hz}$. If only the rms noise in the 3.1 KHz passband is considered then the expected noise of the CCD filter is $v_{rms}^{3.1\ KHz} = (3.1 \times 10^3)^{1/2}$ 2 μv = 111 μv. This value is consistent with the data taken on the double split electrode filter described by Ibrahim et al. [5].

A switched-capacitor filter has two primary noise sources; the thermal noise due to the switch resistance as it charges and discharges the switched capacitors; and the operational amplifiers. By making the switched capacitors sufficiently large the thermal noise from the switches can be sufficiently band-limited so that it is negligible compared to the op amp noise. Since the op amps are inside the filter, the op amp noise is filtered by the filter itself, with various transfer functions depending on the placement within the circuit. If we assume, under worse case conditions, that the transfer function to the output from each amplifier is unity, then for the five op amp filter of Fig. 4 the total wideband noise will be $\sqrt{5}$ x 50 μv = 112 μv. The noise in the 3.1 KHz passband if the sample rate is 128 KHz will be $(3.1\ KHz/128\ KHz)^{1/2}$ x 112 μv = 17 μv which is significantly lower than the CCD filter noise. Even though there is definitely a noise advantage with the use of switched-capacitor filters it is not as large as this example would indicate, because of the frequency dependence of the noise in MOS op amps. In the above discussion it was assumed the op amp noise was white when in fact throughout the low frequency range (< 5 KHz) the noise power has a 1/f dependence. This results in a noise increase in the 0 - 3.1 KHz band by a factor of three to four or more depending on the surface state density (which depends on the device processing).

In summary there are two reasons why switched-capacitor filters have lower noise: since the sample rates are higher the spectral density of the sampled noise is lower which results in lower noise in the filter passband; and the noise gain of each amplifier is only unity compared with a value around 5 for the CCD filter (for this example).

C. Op Amp Requirements

The requirements of the operational amplifiers are reduced for the switched capacitor filters in comparison to the requirements of the op amps needed as charge integrators in the CCD filter output in Fig. 1. In Fig. 6(a) the CCD op amp output waveform is shown. This waveform alternates between a reference level when the charge is not under the sense gate and the output signal level when the charge is present. Therefore the op amp must have the capability to slew and be able to settle with full voltage range swings every clock cycle. It is possible to design op amps to do this at 32 KHz clock rates but it requires power as well as complicating the op amp design.

In Fig. 6(b) is shown the switched capacitor output which indicates the first order hold nature of the output. The op amp is only required to follow the maximum frequency signals the filter passes which is 3.1 KHz for our example. The op amp performance is therefore reduced which makes it possible to design it for lower power and reduced area. In the near

PROCESS DEVELOPMENT

The C^2L and CCD technologies must be combined so that the best characteristics of both are maintained. Since n-channel CCDs provide the highest speed, the lowest dark current generation and highest transfer efficiency when fabricated in a low defect starting material, it is necessary to begin with a p-type starting material. The C^2L process will also be fabricated in the p-type substrate and the p-channel devices are formed in n-wells, which are implanted with phosphorus and driven-in during a long, high temperature cycle. Since the C^2L process does not have field oxide, a major modification must be made to provide the dielectric isolation for the CCD. An isoplanar (recessed) field oxide structure will be used to provide this isolation. This isoplanar oxide can provide CCDs with excellent characteristics and can also be used to provide minimum gate-geometry NMOS FETs. The C^2L/CCD process is then based on a C^2L technology using dielectric isolation (isoplanar oxide) to separate the C^2L portions of the chip from the NMOS/CCD sections, see Fig. 1.

CHIP DESIGN

Fig. 2 shows the test chip which has been designed to evaluate the C^2L/CCD process. The main array (outlined by the white band in the figure) is a 128-stage analog/binary correlator which includes a two-phase CCD clock driver and a binary program register clock driver on the chip[3,4,5]. The rest of the chip is devoted to test circuits which are used to characterize the C^2L/CCD process. All of the logic circuits use 6 μ design rules and have been simulated to 30 MHz. A block diagram of one stage of the correlator is shown in Fig. 3. This shows the location of the NMOS/CCD sections of the chip which are isolated from the C^2L portions of the chip by the isoplanar oxide as shown in Fig. 1. The CCD is a two-phase buried n-channel CCD with two levels of polysilicon and ion implanted transfer regions under the second polysilicon gates. Transistors T71 through T74 are NMOS devices and transistors T75 through T87 are n-channel or p-channel C^2L devices. Transistors T75 to T80 form a set/reset latch which can be isolated from the code program register by T81. This allows the program register to be loaded while correlations are being performed with the previous code which has been latched-up. Clocks ϕ_A and ϕ_B are generated on chip by the program register clock driver circuit shown in Fig. 2. All clock phases required for the CCD are generated in the CCD clock driver circuit except the input strobe phase. The input strobe has not been generated on-chip since the best input technique has not been determined for high speed CCDs. Since there is no conceptual problem in the design of a given input circuit, the open-ended design on the present chip allows the optimum technique to be determined and implemented.

CIRCUIT SIMULATIONS

The circuits have been simulated using a CAD program which uses the Frohmann-Bentchkowsky model as modified by J. E. Meyer. Since no previous data was available for the C^2L model parameters as used in the integrated C^2L/CCD process, they were estimated from previous work on C^2L circuit designs. However, after the first run was made the thresholds for the n-channel devices had to be adjusted, and the second run provided the actual model parameters which were then used to verify the operation of the C^2L/CCD circuits. Figure 4 shows the current voltage characteristics of

several of the FETs which were used in the chip design. Fig. 4a and 4b show p-channel devices and Fig. 4c shows an n-channel device with 6 μ gate lengths. The devices shown in Fig. 4a and 4c were the unit cell devices used in both the CCD clock driver and the program register driver circuits. Although the 6 μ gate length devices were used in the original, Fig. 4d shows a 4 μ gate length p-channel device which was tested in a later version of the clock driver circuits and will be discussed below. The parameters shown in the figures are M: mobility, VT: threshold voltage, SL: slope of the current in the saturation region, C: mobility falloff due to electric field, and N: n-channel or P: p-channel devices. Fig. 5 compares the results of the default values with those obtained using the actual C^2L/CCD model parameters. The figure shows CAD simulations of the CCD clock driver circuit (ϕ_1 and ϕ_2); the default simulation for ϕ_2 is shown by the dashed line and the simulation results obtained from the actual C^2L/CCD model parameters is shown by the solid lines.

POWER CONSIDERATIONS

One of the limiting factors in an integrated high speed CCD device is the power generated by the peripheral circuits in driving the gate capacitance presented by the CCD transfer gates. At frequencies below about 100 MHz this power is reactive power and can be estimated by CV^2f. For the 128-stage CCD in the analog/binary correlator each phase of the CCD has about 40 pF. At 50 MHz the power is around 200 mW with a 10 volt peak to peak clock swing. If the program register is included, the total power at 50 MHz of 100% efficient drivers will be on the order of 750 mW. Although this is not excessive it will degrade the characteristics of the CCD due to the temperature rise in the chip and for longer arrays it will be even worse. An acceptable alternative with bigger arrays or at higher speeds is to take the final driver stages off chip since most of the power is generated in these last stages. This will impose additional design problems of phase delays but these problems should be fairly easy to overcome, and it is much simpler from the system standpoint to add a translater/buffer stage than it is to design all the rest of the logic. The goal in this development is to be able to generate all the logic on chip and as many of the peripherals as possible.

RESULTS

The C^2L peripheral circuits on the chip have operated to as high as 50 MHz as shown in Figure 6. This figure shows a photomicrograph of the program register clock circuit and output waveforms obtained from it at 20 to 50 MHz. The 50 MHz waveform was obtained from a program register which had 4 μ gates and since the limit of the pulse generator used in this test was 50 MHz it is expected that this structure will operate at higher rates. The peak to peak voltage has decreased in this photo because the circuit was originally designed with 6 μ gates to operate at 30 MHz. However, a unit cell approach was used in its design so that the polysilicon gate could be changed easily to 5, 4, or 3 μ gate sizes. In a design for 4 μ at 50 MHz the final output stage would be increased in size to provide the full swing. The CCD clock drivers also have been operated at the designed 30 MHz with 6 μ gates. A test CCD which was included on the chip has been operated at 20 MHz with a transfer inefficiency of about 2×10^{-5}. However, the full analog/binary correlator has not been tested but it is expected that it will operate at 30 MHz with a charge transfer inefficiency on the order of 1×10^{-4}.