ADAPTIVE FILTERING IN CCD AND MOS TECHNOLOGIES

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ABSTRACT

This paper looks at developments in the implementation of adaptive filters which use sample analog techniques in CCD and MOS technologies. The emphasis is on the design and fabrication of adaptive structures that can be integrated together with the necessary peripheral circuitry onto a single chip.

Two MOS implementations are considered: structures employing a CCD to shift the signal past stationary tap weights; and circuits in which the signal is sampled-and-held at fixed sites while the filter tap weights are shifted continuously past these sites to perform the convolution.

A description of a simplified adaptive algorithm which is particularly suitable for digital coefficients is given and a transversal filter chip design is outlined which features multipliers and adaptive circuitry located at each tap.

It is concluded that for voice frequency applications a multiplexed multiplier and update circuit in a rotating tap structure will provide the best compromise.

INTRODUCTION

The ease with which charge-coupled devices (CCD's) can be used to implement tapped delay lines and their consequent suitability for the implementation of transversal filter structures has led to the application of CCD's to many signal processing functions and to the consequent growth of interest in the realization of such functions. More recently there has been considerable activity in the design of programmable CCD transversal filters for a number of applications. Of particular importance is the fact that programmable transversal structures can be used as the basic building block for adaptive filtering.

Adaptive filters find application in noise cancelling, speech processing, and in a variety of telephony and telecommunications applications such as echo cancellation and equalization where the characteristics of the network to which the filter is applied are not precisely known.

A number of alternative approaches have been pursued for programmable CCD filtering, differing principally in the means for carrying out the per tap multiplication and coefficient storage. Denyer et al.[1] have described a structure where the tapped CCD delay line interfaces with a single transistor analog multiplier and coefficient storage is realized in analog form using per tap sample and hold sites. White et al.[2] have described structures employing NMOS analog conductances as the reprogrammable coefficients. Haque and Copeland [3] proposed an alternative structure where the CCD itself is

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replaced by an array of sample-and-hold sites, the coefficients are in binary form and multiplication is accomplished with capacitor weighted multiplying digital to analog converters (MDAC's).

The latter approach in particular (often referred to as rotating tap)[4] lends itself to the design of adaptive structures. The operation of a programmable filter of this type in an adaptive mode with an off-chip update algorithm has previously been described.[5] Using a form of the least mean square (LMS) algorithm a programmable filter with 32 taps was shown to adapt to both finite and infinite filter characteristics at voice bandwidths with residual errors of 25 dB below the peak filter response and convergence times of the order of 350 msec.

The approach can be extended to monolithic implementations of adaptive filters where the update circuitry is built onto the chip. The following sections will describe one approach to the design of such a self-contained adaptive filter, suitable for use with sampling frequencies in the voice band range.

THE ROTATING TAP STRUCTURE

The principle of operation of such a structure can be described with the aid of Fig. 1.

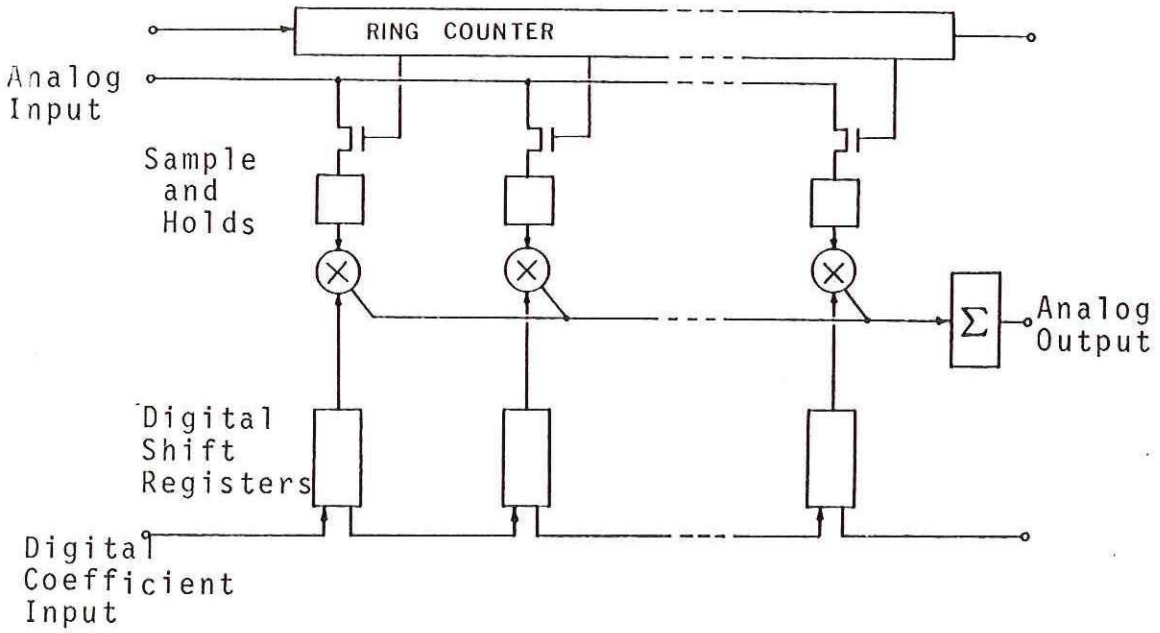

Figure 1. The rotating tap structure

The input signal is sampled-and-held on fixed nodes on the chip, each being refreshed only once every nth sampling period for an n tap filter. The binary tap coefficients shift past these sample-and-hold nodes continuously in order to perform the convolution. The per tap multiplication can now be achieved using an MDAC.

The MDAC and binary coefficients could be combined with a CCD analog delay line but there are several advantages to this newer approach. The generation of the signal at each sample-and-hold node can be accomplished simply with a single op-amp multiplexed in turn in a feedback loop with each node to ensure a linear output.[3] As the analog signal remains stationary there is no transfer inefficiency. In addition, the use of a double polysilicon process allows the design of poly-poly as opposed to MIS capacitors thereby minimizing leakage and dark-current effects.

The dynamic digital shift registers, when recirculated, allow long-term storage of the tap coefficients, a crucial feature for any practical device. This comes at a certain cost; the width of the shift register cells becomes the determining factor in how many taps may be implemented on a chip. Whereas CCD filters with all-analog coefficients have been implemented with 256 taps [1] the rotating tap devices are limited to between 32 and 64 taps per chip. However, such chips can easily be cascaded as there is no requirement for analog signal transfer between devices; they are all connected to a single low impedance signal bus.

In programmable CCD structures the dynamic range is limited principally by linearity and not by noise levels. In contrast, rotating tap structures can attain good linearity (in excess of 55 dB second harmonic distortion) but as a result of their essentially multiplexed nature, gain variations between taps resulting from process variation across the die give rise to fixed pattern noise (FPN) which is significantly higher than the random noise level. Signal to thermal noise ratios for such structures in excess of 85 dB have been measured. Careful design is required to minimize FPN particularly in the multiplier (MDAC) and at the interface between the sample-and-hold and the multiplier where there is a transition from signal representation in terms of voltage (sample-and-hold), to charge (MDAC). This interfacing problem occurs also in CCD transversal filters where a conversion from charge to voltage takes place, causing inaccuracy in the tap output gains.

THE MULTIPLIER

As a result of the need for binary tap coefficients the multiplier must take the form of an MDAC. Previous implementations have reported on the design of m-bit parallel per tap MDACs, where an m-bit digital word switches in the appropriate combination of m binary area ratioed capacitors per tap. Although this approach is attractive from the point of view of speed the capacitors occupy a large area.

The alternative described here is to use a serially loaded MDAC. This occupies less area and fits well with the adaptive update circuitry but requires m clock cycles per sample period and is therefore inherently slower than the parallel approach.

The operation of the serially loaded MDAC with two's complement coding can be described with the aid of Figure 2.

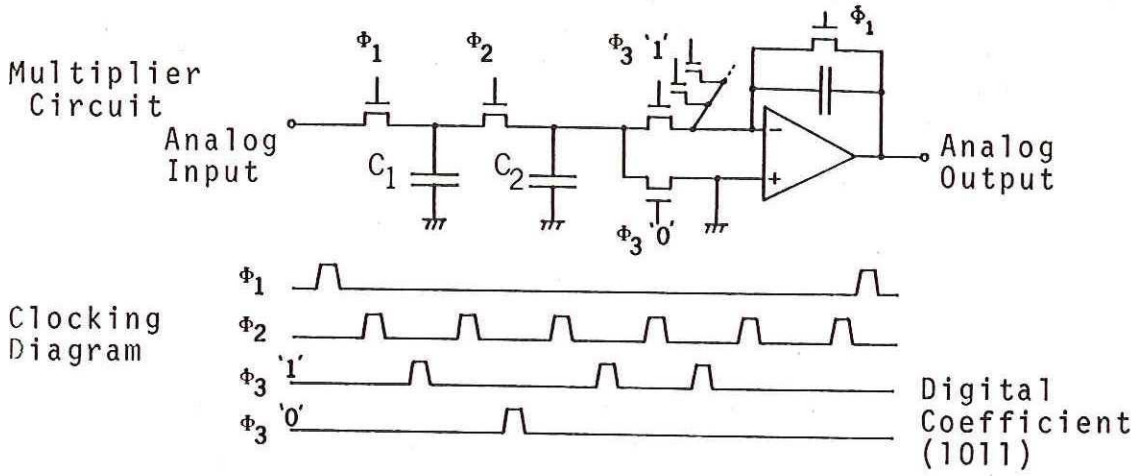

Figure 2. A serial per tap MDAC

Each MDAC consists of a signal inverter/non-inverter, two capacitors, C_1, C_2, of equal value, and an integrating op-amp which is common to all taps. Initially the output of each sample-and-hold and the bias voltage are connected across the input to each multiplier. Inversion or non-inversion takes place according to the sign bit of each coefficient, and the analog samples stored across C_1 in each multiplier. Next, C_1 and C_2 are connected (within each multiplier) transferring half the signal charge to C_2. C_2 is then either connected to the input of the integrating op-amp if the most significant bit (MSB) of the respective coefficient bit is a "1", or it is discharged to ground if the coefficient bit is a "0". This connection scheme is reversed if the sign bit is negative, to account for the two's complement coding.

The charge in each C_1 is then again shared with each C_2 (which reduces the voltage to 1/4 of its original value) and transferred to the integrator according to the magnitude bit. After all m magnitude bits have been processed in this manner the output of the integrating op-amp represents the sum of the products of all n multipliers, and constitutes the output of the transversal filter.

THE UPDATE SCHEME

As each digital tap coefficient moves to the next tap location it must be updated by the adaptive algorithm. The result of the convolution of N tap weights $h_n(k)$ with the corresponding analog signal samples $x(n)$ produces an output $y(n)$.

$$y(n) = \sum_{k=0}^{N-1} h_n(k) \cdot x(n-k).$$

Figure 2. A serial per tap MDAC

If the error between the filter output and the desired response is

$$e(n) = d(n) - y(n),$$

then it can be shown that the following iterative process for tap weight adjustment [6] leads to a minimization of the mean squared error

$$h_{n+1}(k) = h_n(k) + \delta e(n).x(n-k) \quad \text{for } k=0,1, \ldots N-1.$$

This is a simplified form of the least mean square (LMS) algorithm where δ is the convergence factor. This can be further simplified by taking only the sign information of both the error and signal.

Then

$$h_{n+1}(k) = h_n(k) + \delta \ \text{sgn}[e(n)] \ \text{sgn}[x(n-k)].$$

This simplified form of update (the clipped - data LMS error algorithm) coupled with the rotating tap technique gives rise to a very straight forward MOS realization of the algorithm.

It has been shown [7] that this "clipped-data" approach serves to "whiten" or de-correlate the input signal. This is desireable since the LMS algorithm itself has rapid convergence only for uncorrelated signals such as white noise.[7] Voice signals generally do not have this characteristic so they need to be de-correlated to assist rapid convergence of the filter function.

One tap location showing the update scheme is illustrated in Figure 3.

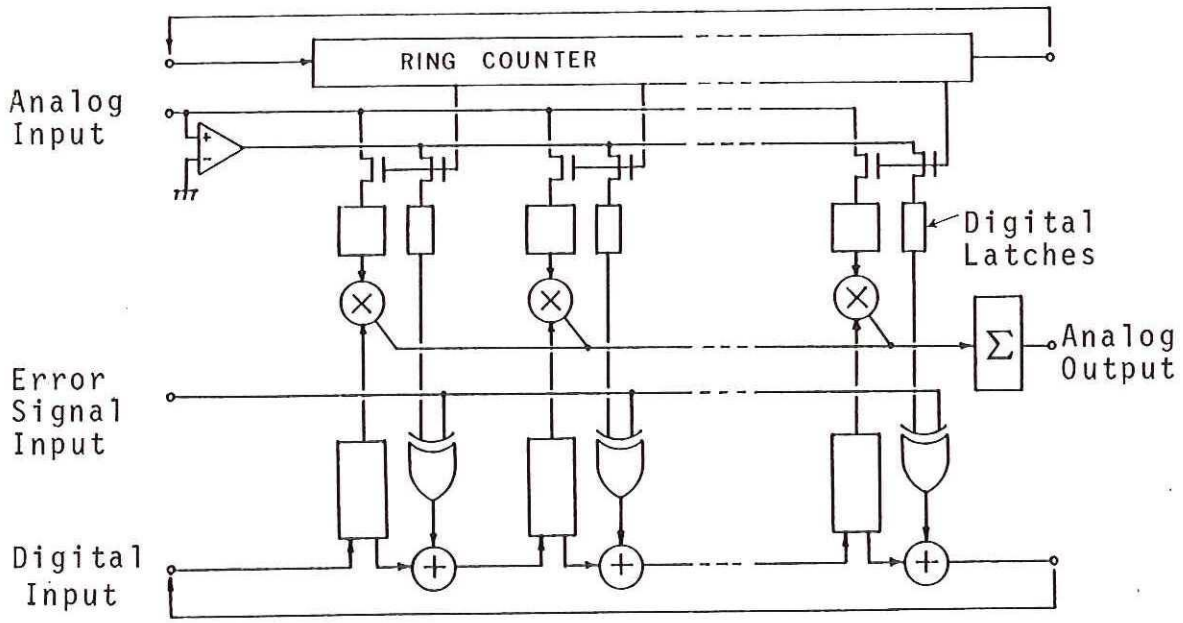

Figure 3. Single tap, showing the update scheme.

The correlation is achieved by multiplying the sign of the error signal (obtained off-chip) by the sign of the analog signal sample at each tap. A positive, zero or negative product, increments, does not change, or decrements respectively the corresponding coefficient. A one bit full adder is used to update each coefficient bit-wise serially.

The convergence factor for this scheme is equal to the value of change in the coefficient ($\pm$ 1), divided by the maximum value of the coefficient (2^m).

Since multiplication must be done MSB first in the serial MDAC, and addition must be done MSB last, the digital shift registers must be bi-directional so that data may be shifted back and forth between sampling instants. Some logic must also be incorporated at each tap to prevent overflow and underflow of the coefficients, which could cause instability.

THE CHIP LAYOUT

A photomicrograph of the chip is shown in Fig. 4. There are 32 taps with 7 bit-magnitude plus sign coefficients. The two capacitors in the serial multiplier can be clearly seen towards the top of the photograph whilst the 8 bit shift registers are evident in the lower portion.

The two op-amps, one for input linearization and the other for the multiplier sensing, are visible in the top right.

The external circuitry consits essentially of clock generation, comparators, and a sample-and-hold for the output.

The 205 x 170 $mils^2$ chip was fabricated using an NMOS double poly process.

SUMMARY

A description of the rotating tap transversal filter has been given, and the structure modified to incorporate the circuitry necessary at each tap to enable adaptivity. The update algorithm was outlined together with reasons for its choice. The use of per tap multipliers and update circuitry permits cascading devices without the need for increased clock frequencies, but at a cost of increased FPN and the need of a small area serially loaded MDAC. The trade-off indicates that for voice frequency applications, a multiplexed multiplier and update circuitry would yield better noise performance in a small area. For this latter approach the rotating tap structure is ideal.

The approach is also worth pursuing because of its ease of implementation in MOS technology and because computer simulations of the simplified algorithm indicate that 35 dB noise cancellation can be achieved with a convergence time of 300 mS.

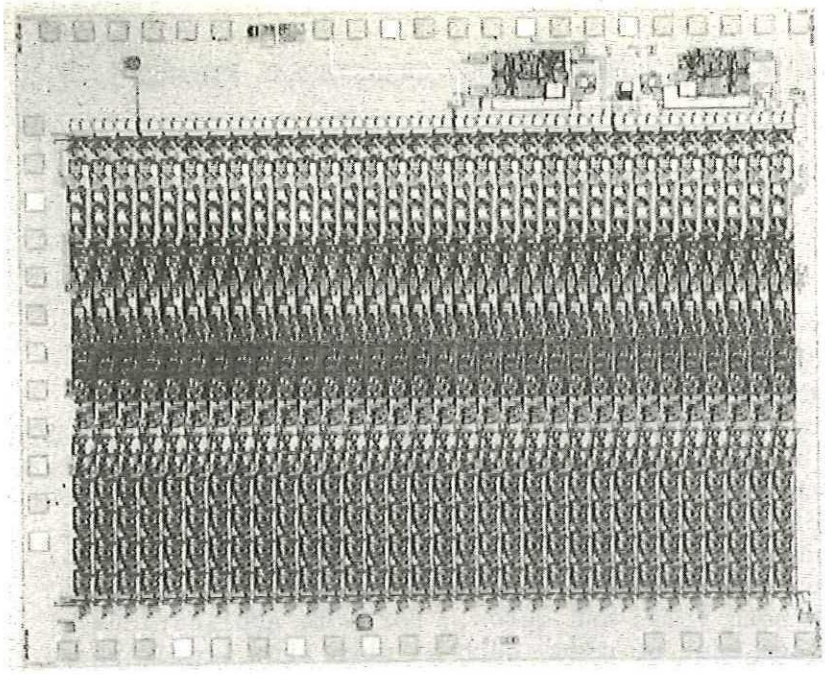

Figure 4. Photomicrograph of Adaptive Filter Chip

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