THE ELECTRICALLY PROGRAMMABLE SPLITTED-ELECTRODE CCD TRANSVERSAL FILTER (EPSEF)

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ABSTRACT

A novel concept for electrically programmable tap weighting in surface charge-coupled device splitted-electrode transversal filters is presented. The analogue-programmable tap weighting is based on the redistribution of the charge packet, prior to the splitted-electrode sense operation. The redistribution takes place underneath a lightly doped polysilicon gate and performs two-quadrant analogue tap-weight multiplication. The performance data of a prototype filter with 8 electrically programmable taps demonstrate the appealing features of this concept for analogue tap weighting.

INTRODUCTION

During the last decade new analogue sampled data circuits have raised a growing interest in integrated-circuit filter implementations. Charge-transfer devices and switched-capacitor circuits have shown to offer an adequate solution to many filtering problems in the fields of communication, instrumentation and other analogue signal processing [1, 2] . Particularly the splitted-electrode CCD concept has been successfully applied in the implementation of transversal filter functions, e.g. the PCM low-pass filter and the chirp-Z transform filter [1].

Besides these mask-programmable filters, there is a demand for electrically programmable filters. These can be applied as adaptive filters, correlators or as fixed filters in small volume applications. Most electrically programmable CCD filters that have been reported [3, 4, 5], use one or more floating-gate tapped delay lines with analogue or binary multipliers.

In this paper a new electrically programmable splitted-electrode filter (EPSEF) is presented, which uses a CCD with splitted-electrode sensing and an in-channel tap-weight multiplication. The in-channel tap-weight multiplication is achieved by the redistribution of the charge sample before it is partitioned, transferred and sensed at the splitted electrodes. The sensing and summing techniques for the partitioned charge packets are the same as in the conventional splitted-electrode CCD's.

The theoretical background of the in-channel tap-weight multiplication principle is explained in the next section. The design of an 8-tap implementation and some technological details are discussed in the third section. Performance data and examples of filter functions, obtained by the EPSEF, are presented in the fourth section. Finally the main conclusions are summarized.

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TAP WEIGHTING BY CHARGE REDISTRIBUTION

In CCD splitted-electrode transversal filters, the charge samples are sensed nondestructively by constant-voltage sensing at the splitted sense electrodes. The tap-weight multiplication is performed by measuring the difference between the charge samples under the two segments of a splitted electrode. In this approach the charge underneath the segments of the sense electrode is uniformly distributed. The tap-weight value is determined by the difference between two segments areas of the splitted electrode.

The novelty of the EPSEF CCD concept is the redistribution and the partitioning of the charge sample before it is transferred towards the splitted sense electrode. Rather than by the geometry of the splitted electrode, the tap-weight value is now determined by the redistribution of the charge sample. The redistribution of the charge sample in the transverse direction is controlled by a potential gradient in a resistive gate on top of a storage well. After the redistribution has settled, the charge packet is partitioned during the next charge transfer, by means of a channel-stopper split in the middle of the CCD channel. This split extends from the resistive gate upto and including the two equally sized sense-electrode segments.

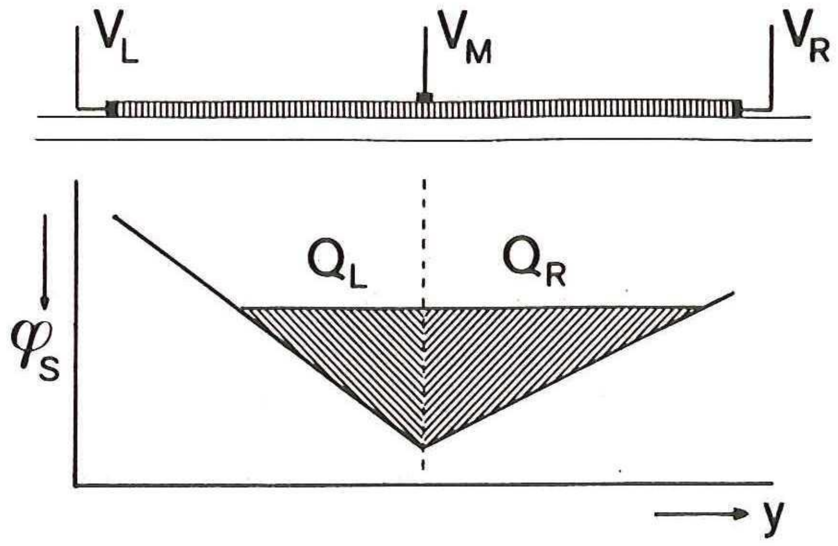

Figure 1. Crosssection through a resistive gate, with surface potential plot.

Figure 1 shows a crosssection of the resistive gate. The resistive gate has 3 contact areas: one in the middle and one at each end. In an n-channel device, the middle contact is connected to the highest potential V_M, which is kept at a constant dc level. The left and right hand voltages V_L and V_R control the charge redistribution process. The wedge-shaped surface potential of an empty well is shown in the lower part of figure 1. Also the potential in the presence of a charge packet is shown. The product of the potential difference and the "well-capacitance" per unit area equals the inversion charge density. The charge portions Q_L and Q_R of the total charge packet Q_S are calculated as:

$$Q_L = \frac{V_M - V_R}{2V_M - V_L - V_R} Q_S \tag{1}$$

$$Q_R = \frac{V_M - V_L}{2V_M - V_L - V_R} Q_S \tag{2}$$

In surface CCD's this result is independent on the function that describes the relationship between the surface potential and the gate potential, if this function is monotonically increasing and not an explicit function of the location. The results (1) and (2) indicate that the redistribution is controlled by the potentials applied to the resistive gate. The relations (1) and (2) are simplified by substitution of:

$$V_L = V_B + V_{TW} \tag{3}$$

$$V_R = V_B - V_{TW} \tag{4}$$

V_B is a bias potential and V_{TW} is the variation around the bias. The differential charge is found as:

$$\Delta Q = Q_L - Q_R = \frac{V_{TW}}{V_M - V_B} Q_S \tag{5}$$

The multiplication factor represents the tap-weight coefficient h_k, hence for the k^{th} tap:

$$h_k = \frac{V_{TW,k}}{V_M - V_B} \tag{6}$$

Obviously an ideal multiplication is obtained if the outer terminals are controlled by a differential voltage V_{TW} superposed on a bias voltage V_B.

This concept of charge partitioning by means of controlled charge redistribution is a novel method for performing a multiplication operation on sampled data, represented by charge packets. Analogue control voltages and the symmetry of the construction provide for an analogue two-quadrant multiplication. If the signal charge is modulated on a background charge packet and alternatively a background charge packet and a background + signal charge packet is sensed, four-quadrant multiplication may be obtained [4]. An additional advantage of the symmetry of the sense electrodes is its decreased sensitivity for clock feedthrough.

THE EPSEF DESIGN

The design of the electrically programmable splitted-electrode filter is for the major part similar to that of a splitted-electrode CCD filter with fixed tap weights. In the input section a fill and spill method is used. A delay section in the CCD design consists of two transfer gates and two storage gates. The EPSEF is clocked in the 1½ phase mode, thus allowing constant voltages at the sense electrodes and the resistive gates. The amplitude of the clockpulses is 10 V_{pp}. The filter is operated with a background charge that fills half a full storage well. The CCD delay line output stage is equiped with a floating diffusion buffered by a MOST source follower. Each tap-weight section in this design requires two delay sections, see figure 2. A tap-weight section starts with a clocked transfer and storage gate ϕ_1 and ϕ_2. Then a transfer gate at dc potential ϕ_3 preceeds the tap-weighting resistive gate. The resistive gate is again followed by a clocked transfer and storage gate. A next transfer gate ϕ_3' at dc potential preceeds the splitted sense electrode.

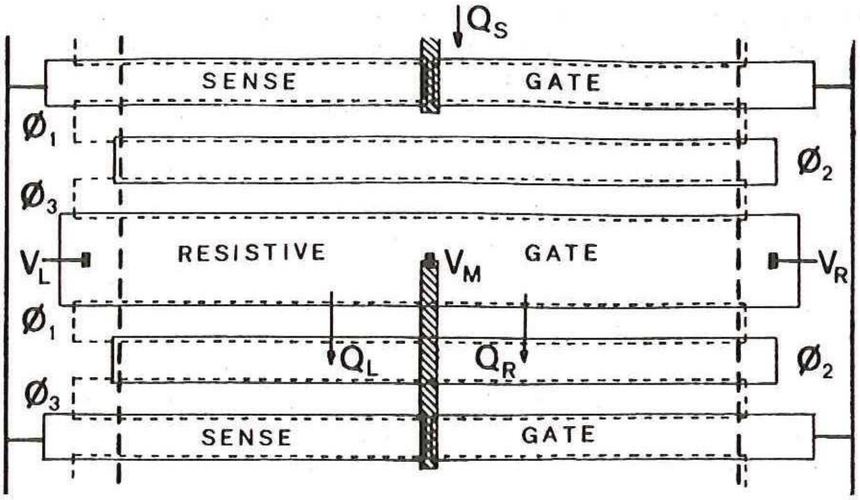

Figure 2. Top view of the EPSEF structure.

A channel stopper diffusion split (width: 15 μm) in the middle of the channel (width: 400 μm) extends from half-way the resistive gate as far as the end of the splitted sense gates. In order to maintain the full charge handling capacity, the resistive gate length has been designed at 30 μm, while the sense and storage gate lengths have been designed at 15 μm.

The prototype design of the EPSEF contains 8 programmable taps, each having two external connections for the tap-weight control voltage. On-chip control circuitry is well conceivable, but has not yet been implemented. The left-hand segments as well as the right-hand segments of the sense electrodes have been interconnected; each group is also connected to an on-chip source follower, thus obtaining low-impedance outputs. Feedback capacitors and MOST-reset switches for the constant voltage sensing are included on the chip, only the operational amplifiers are externally connected. A microphotograph of the EPSEF is shown in figure 4.

The EPSEF has been implemented in a two level CVD polysilicon process on 10 Ωcm p-type material. The resistive-gate material, lightly doped polysilicon [6], has been processed by doping a polysilicon layer from a lightly doped oxide. The resistive gates are integrated in the first polysilicon level; the fabrication process requires one additional mask compared to the conventional splitted-electrode transversal filters. The resistivity of the resistive-gate material has to be in the range of 1 to 10 KΩ/□; the exact value is not important if the power dissipation is low and the variation in resistivity is small. In the contact windows the lightly doped polysilicon is heavily doped in order to provide for a low and linear contact resistance. This local over-diffusion, however, enlarges the equipotential area at the middle contact. Some parameters of the lightly doped polysilicon are:

layer thickness	400 nm
estimated doping concentration	3.10^{18} cm^{-3}
resistivity	6.5 KΩ/□
temperature coefficient	- 0.4%/K
gate dimensions	30 x 400 μm^2
equipotential middle area	19 - 22 μm

The total power dissipation in one resistive gate is 0.7 mW at V_B = 3V and V_M = 7V.

PERFORMANCE DATA

The relation (6) for the tap-weight multiplication factor has been derived in the second section using first order approximations. The influence of second order effects has been elaborated in [7]; it is found that the following effects degrade the performance of the tap-weight multiplication:

- The resistive polysilicon gate in this device has been doped from a chemical vapour deposited lightly phosphorus-doped silicon oxide. A small resistivity gradient in the resistive gate may occur causing an offset in the tap-weight multiplication factor. Doping by ion-implantation may improve the uniformity of the resistivity.
- The influence of the middle contact dimensions has been neglected. Calculations show that an equipotential area in the surface potential underneath the middle contact leads to a harmonic distortion of - 46 dB.
- The redistribution process of the charge requires settling time. Worst case computer simulations indicate a settling time of 3 μs for a 0.1% approximation of the steady state solution.

Measurement series on prototype devices confirm the theoretical expectations.

By means of a small-signal method, the filter output signal V_f has been measured as a function of one tap weight h_k, whereas the other tap weights have been set zero (fig. 3).

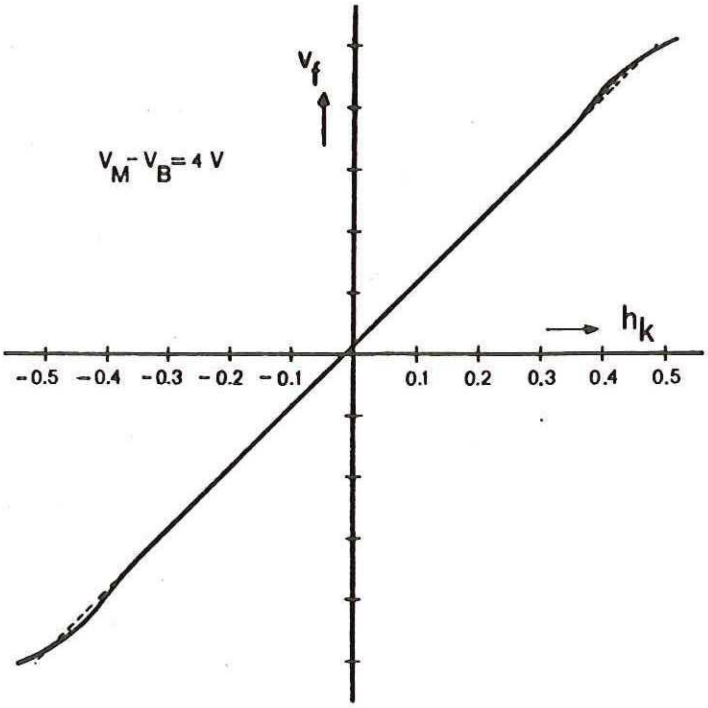

Figure 3. The ac filter output signal v_f versus the tap weight h_k.

A "linear" multiplication is obtained if $-1.4V < V_{TW} < 1.4V$ or $-0.35 < h_k < 0.35$. Outside this range the multiplication operation fails, because the charge has reached the sides of the potential well. Misalignment errors or a resistivity gradient cause a charge offset of approximately 1% of the total charge.

The distortion and the signal to noise ratio have been measured with one tap weight at $h_k = 0.25$ and the other tap weights at $h_k = 0$. In this "delay-line" mode the second harmonic in the output signal is less than - 42 dB and the signal to noise ratio is 35 dB $(0 - \frac{1}{2} f_c)$. The noise is mainly caused by 1/f noise in the source followers of the sense circuitry. The clock frequency of the EPSEF during these experiments has been 100 kHz.

The filter devices have been operated satisfactorily at clock frequencies between 1 kHz and 250 kHz. The charge transfer inefficiency of the CCD delay line is 3.10^{-4} per transfer.

Filter functions that have been implemented, are the Hilbert transformer, the low-pass filter, and a 7 bits p-n Barker code. The low-pass filter transfer function is shown in figure 5. The sideband suppression in the low-pass filter is 40 dB, which is in agreement with the theoretical expectation. The 7 bits Barker code can be used for determining the dynamic range. The Barker-coded filter is operational in a 60 dB input amplitude range. If the dynamic range is defined as the input range, in which less than - 40 dB distortion occurs and in which the output amplitude is more than twice the noise amplitude, approximately 50 dB is reached.

SUMMARY

The charge-redistribution concept for electrically programmable tap weighting in splitted-electrode CCD's has been presented. This concept has been implemented by means of resistive polysilicon gates in an 8-tap electrically programmable CCD filter. The performance of this device confirms the theoretical descriptions and demonstrates the utility of this concept. The features are: analogue tap-weight control, low distortion, small chip area occupation and low power consumption. The linearity of the analogue multiplier concept seems to be promising for analogue correlator implementations.

An important advantage of this novel concept is the application of the sensing, signal-summation and output techniques of the well-known splitted-electrode transversal filters with fixed tap weights. The only additional technological process step is the deposition of a resistive polysilicon gate. Except for the uniformity of the resistivity, there are no strong requirements for this processing step. Deviations of the absolute value of the resistivity do not degrade the filter performance.

The redistribution concept offers the filter designer an electrically programmable filter, which incorporates all advantages of the splitted-electrode CCD fixed filter design.

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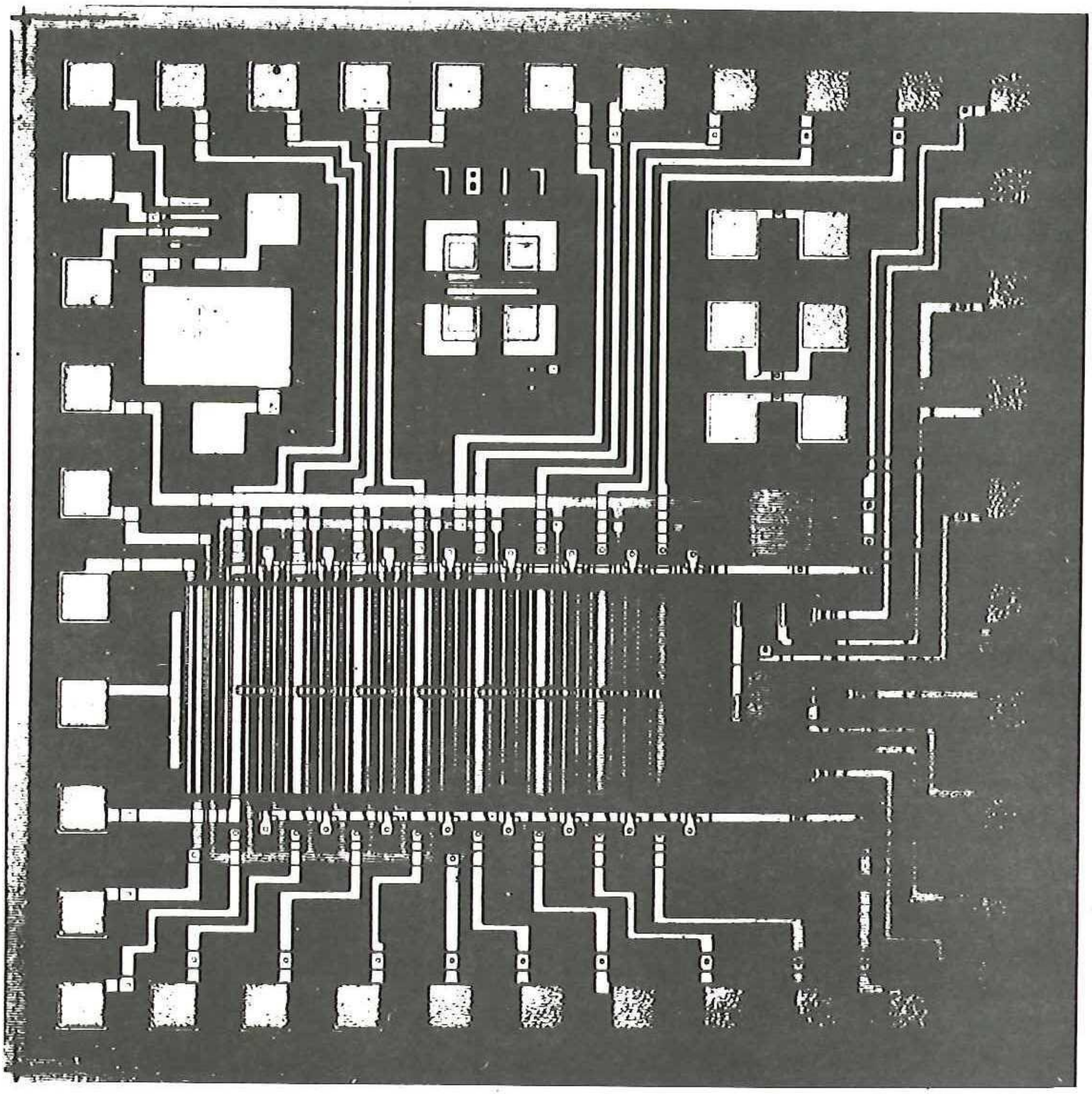

Figure 4. The 8-tap EPSEF chip (2 x 2 mm^2).

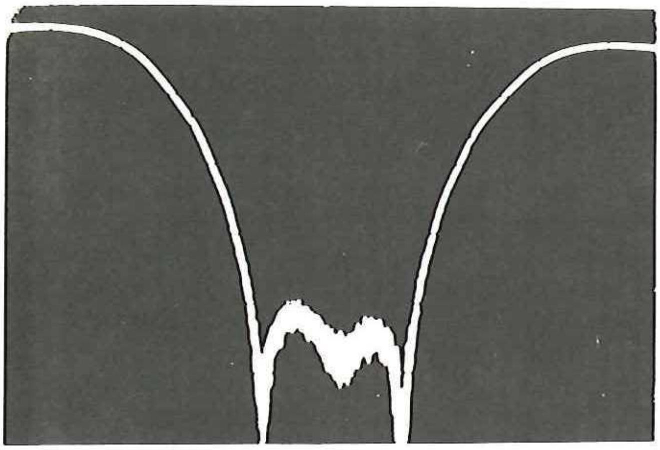

Figure 5. The EPSEF CCD as a low-pass filter. Horizontal: 5 kHz/div. center frequency is 25 kHz. Vertical: 10 dB/div.