256 POINT CCD PROGRAMMABLE TRANSVERSAL FILTER

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ABSTRACT

This paper presents a monolithic implementation of a fully programmable transversal filter containing 256 points and operating up to clock frequencies of 2 MHz. CCD and linear MOS circuitry have been combined to realise a stable, easy-to-use filter within a 16 pin DIL package. Novel operational amplifiers have been developed and are combined on chip with the CCD to automatically achieve a linear, unity gain transfer characteristic which is independent of process variations and is insensitive to parametric drift and supply voltage fluctuations.

The design of the operational amplifiers, and of the CCD and linear MOS circuitry is discussed. The significance of the device is stressed in the practical results which are presented.

INTRODUCTION

Of all CCD structures for signal processing, the transversal filter has been identified as potentially the most powerful[1]. The *programmable* transversal filter then, combines versatility with this power, and thus the production of such a filter is an extremely desirable goal. However, if this device is to prove useful, then it is important that as much of the peripheral circuitry as possible be integrated, so that the filter is easy to use. External adjustment is not desirable and should at least be limited to once-and-for-all settings. Thus internal biasing and chopper-stabilisation techniques must be considered.

For matched filtering applications, it is desirable that as many filter points as possible should be integrated, as well as allowing for devices to be cascaded.

The filter architecture of Fig. 1 is a direct realisation of the classical transversal filter and has been previously reported[2] as offering a most compact circuit by virtue of its simplicity. This architecture has been further developed to produce a 256 point PTF within a 16 pin DIL package. Additionally, a novel general purpose operational amplifier has been developed and is used on the chip to minimise external requirements and thus make the device easy to use.

CCD

The signal register used is a double-polysilicon gate CCD operated essentially in 1½ phase mode with a floating-gate-reset[3] tap at each cell, Fig. 2, on a pitch of 28 μm. To avoid excessive clock breakthrough onto the tap, the clock is split into two phases, ϕ_s and ϕ_s', having the form shown in Fig. 3. The split phase, ϕ_s', is used to isolate the tap within the CCD before ϕ_s floats the tap and then transfers the charge underneath it. A complementary phase $\overline{\phi_s}$ is used to sample and hold the tap output. In this mode, using 15 V clocks, breakthrough onto the taps is limited to 400 mV and a useful linear tap signal range of 2 V is available.

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Charge input is by diode cut-off, although the input gate is made considerably smaller than the rest of the CCD in order to minimise undesirable charge-partitioning effects. The 256 point register consists of two 128 point CCDs combined with a single corner-turning diffusion. Cti is estimated at 10^{-3} per tap for this surface-channel line, and dark current limits total storage time to approximately 250 msec ($f_c \simeq 1$ kHz), at room temperature.

The input is feedback-linearised[4] using one of the on-chip operational amplifiers by including the input diode and first CCD tap within its feedback loop. In this way the through gain from signal input to tap output is automatically linearised and is forced to unity; an extremely useful feature for cascading these devices. For a 1 V p-p signal the through gain is unity to better than 2% and total harmonic distortion is below -40 dB. The operational amplifier automatically compensates for process offsets and gain variations. Clearly this technique is extremely powerful, making the CCD a useful delay element in its own right.

MULTIPLICATION

A single transistor 4-Q MOST multiplier is incorporated at each filter point . The signal is applied to the gate, reference to the source, and the drain is connected to a common current-summing output bus. For signals above 0 Hz:

$$i_{out} = \beta_M V_{sig} V_{ref}$$

where β_M is the transconductance of the multiplier transistor. The output current is current-to-voltage converted off-chip in a single common-base bipolar transistor stage. Signal linearity is limited by field dependent mobility in the multiplying MOSTs to a total harmonic distortion better than -40 dB for signals of 1 V p-p.

REFERENCE STORAGE AND REFRESH

Analogue tap weights are stored in a stationary array on 1 pF capacitors, and are applied to the multiplier transistors through source-follower buffers. Update of the array is achieved in a serial manner by propagating a logic '1' along a dynamic digital shift register. This logic pulse enables a series of transistor switches which sample analogue reference samples off a single reference input bus.

The reference shift register may be clocked up to 5 MHz for fast reference update or, for convenience, synchronously with the CCD.

OPERATIONAL AMPLIFIER

If operational amplifiers are to perform a useful task on-chip then they must be compact, self-biasing and preferrably chopper-stabilised using the available CCD clocks. Such an amplifier has been developed and is used twice on this filter chip.

A diagram of the amplifier structure is shown in Fig. 4. The input stage is formed around a switched capacitor differentiator[5], which uses the complementary CCD clocks. The output of this stage feeds a high gain cascode-connected depletion-load invertor, which in turn is buffered by a simple source follower stage.

In operation the entire amplifier is switched in two phases. During one phase an input is sampled and the amplifier is internally reset. During the complementary phase the feedback loop is completed and the amplifier performs the task of equating its inputs. The advantages of this amplifier are its simplicity (9 MOS transistors, 1 MOS capacitor) and its features of automatic self-bias and chopper-stabilisation via the switch M3. No compensation is necessary because there is a single dominant pole at the output of the invertor stage. The amplifier is thus extremely compact, occupying an area of typically 100 x 200 μm, or about the size of two bond pads.

Because these amplifiers are designed to settle entirely within the duration of each phase, there is no roll-off in frequency response; thus all signals up to and including Nyquist are handled equally well. The amplifiers used on the filter chip feature open loop gains >40 dB and operate successfully up to clock rates of 2 MHz. The clocked nature of the circuitry clearly makes them suitable for general application in switched capacitor circuits.

DEVICE

A photograph of the device is shown in Fig. 5, from which it can be seen that the 256-point filter is formed from two blocks of 128 points which are mirror-imaged. The chip measures 4.5 mm x 3.8 mm (.180" x .150") and thus fits into a standard 16 pin DIL package. To drive the chip little peripheral circuitry is necessary; two standard CMOS logic packages for clocking, two trimpots (one to adjust the signal input and one at the filter output), and a dozen discrete components.

PERFORMANCE

The device has been tested to clock frequencies of 2 MHz. Fig.6 shows a typical output peak obtained by correlating together two full-bandwidth chirp waveforms. Note that this correlation peak is not significantly degraded by cti effects, indeed by cascading these devices useful peaks may be obtained from chirps having time-bandwidth products up to 1000. The dynamic range of the correlation peak shown is in excess of 60 dB.

A further demonstration of device performance is given in Fig. 7 which shows the convolution of two square waveforms to produce a triangular filter output. The quality of this output waveform is again of note; dynamic range here exceeds 70 dB.

CONCLUSIONS

We have demonstrated how a modern CCD/MOS process may be combined with a high degree of design engineering to produce a compact, easily used programmable transversal filter. The device has major applications as a matched filter in lightweight *sonar* equipment and as part of a self-training, or *adaptive* filter using additional feedback circuitry[6]. The concept of employing such a device within an adaptive loop is a powerful one, in that many remaining device errors become automatically cancelled.

It is possible that the reference loading circuitry on this device may be replaced with a multiplier-accumulator structure at

each filter point with no extra penalty in silicon area. This will make feasible a monolithic adaptive filter containing up to 256 points[6].

ACKNOWLEDGEMENTS

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REFERENCES

1. "Charge Coupled Devices and Systems", Chapter 3, Edited by M.J. Howes and D.V. Morgan, Wiley, 1979.

2. P.B. Denyer and J. Mavor, "Miniature Programmable Transversal Filter using CCD/MOS Technology", Proc IEEE Special Issue on Miniature Filters, Jan 1979, pp.42-50.

3. P.B. Denyer and J. Mavor, "Design of CCD Delay Lines with Floating-Gate Taps", SSED, July 1977, pp.121-129.

4. D.J. MacLennan and J. Mavor, "Novel Technique for the Linearisation of Charge-coupled Devices", Electron. Lett., 1975, 11, pp. 222-223.

5. P.B. Denyer and J. Mavor, "Novel MOS Differential Amplifier for Sampled Data Applications", Elect Lett, 1978, Vol 14, No. 1, pp. 1-2.

6. C.F.N. Cowan, J.W. Arthur, J. Mavor and P.B. Denyer, "CCD Based Analogue Adaptive Processing", this conference.

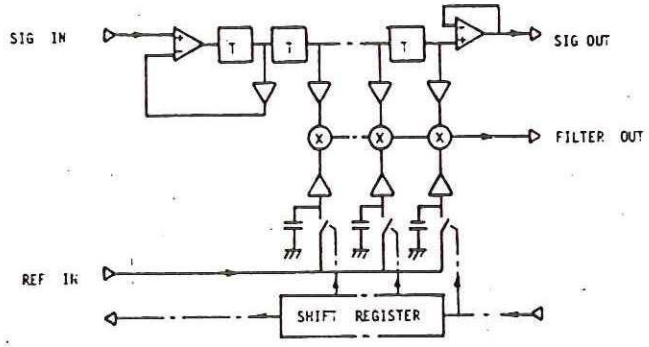

Figure 1: 256-Point Filter Architecture

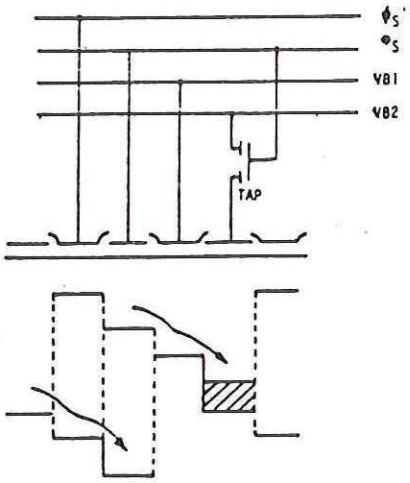

Figure 2: Charge Transfer and Tapping Schemes

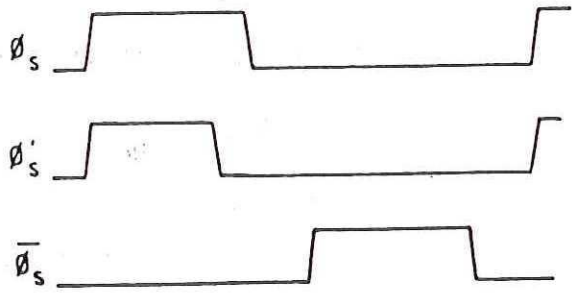

Figure 3: CCD Clock Waveforms

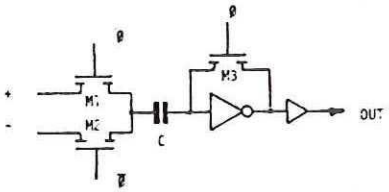

Figure 4: Operational Amplifier Architecture

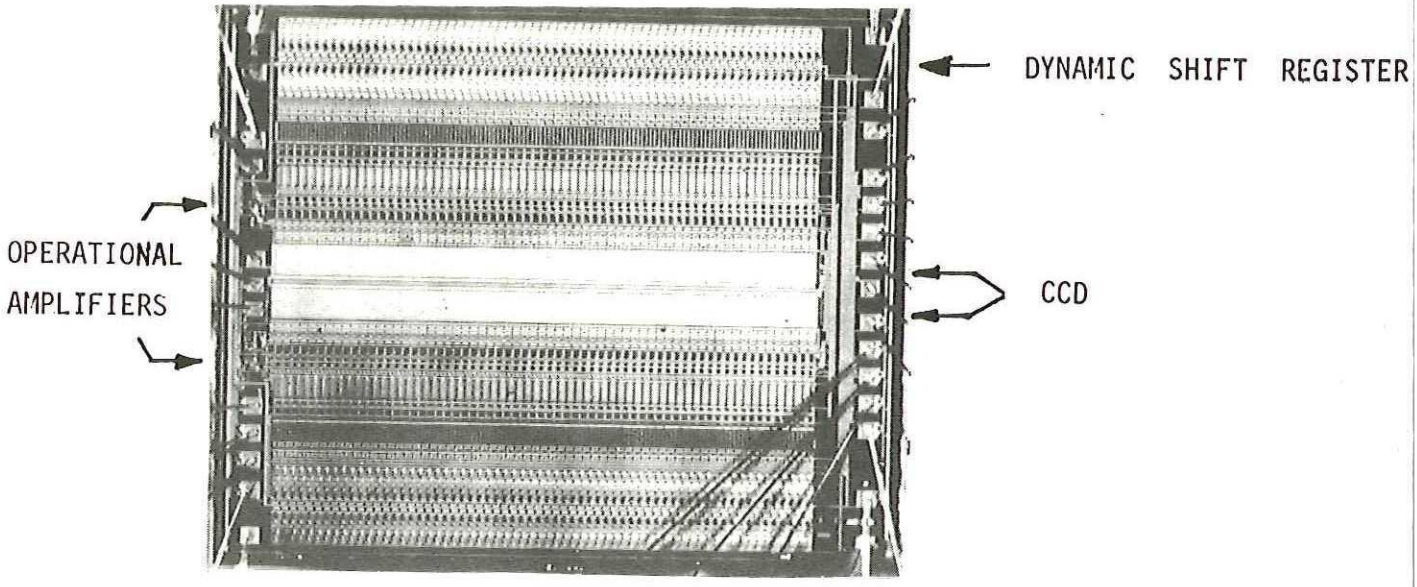

Figure 5: Photograph of the 256 point PTF

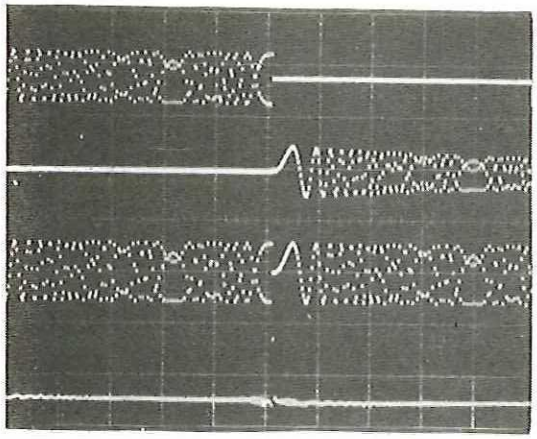

Figure 6:

Correlation of chirp waveforms

$0 - \frac{fc}{2}$ fc = 100 KHz

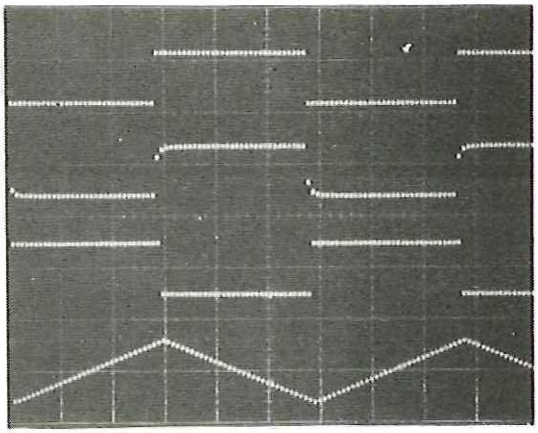

Figure 7:

Correlation of square waveforms

fc = 100 KHz