DESIGN AND APPLICATION OF A CASCADABLE BINARY WEIGHTED ANALOGUE CORRELATOR

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Abstract

A cascadable 127-tap binary weighted analogue correlator is described. The device has been cascaded and operated as a 254-tap correlator for both baseband and bi-phase coded signals at clock frequencies from 1 kHz to 2 MHz. The device has also been operated as a low pass filter and shows good linearity and dynamic range. On-chip power dissipation is 20 mW.

1. Introduction

In spread spectrum communication systems Pseudo Random Noise (PRN) codes are used to trade off bandwidth against signal power. In order to receive the data it is necessary to correlate the received signal, buried in noise, with a reference code. Charge coupled devices offer an efficient approach to the realisation of a binary weighted analogue correlator due to their inherent ability to store and weight analogue samples[1]. The binary-analogue correlator is simply a transversal filter with coefficient values of +1 or -1. The impulse response of the transversal filter is the time inverse of the pseudo random sequence it is designed to detect. Of more general interest is a device whose coefficients can be programmed electrically so that any number of different codes can be used.

This paper describes a 127-tap (64-bit digital) binary weighted analogue correlator chip. It is fabricated on a double poly N-channel process which has surface and buried channel CCD available. The correlator is designed so that up to 16 chips can be cascaded and therefore PRN codes of up to 1024 bits may be used (with 30 dBs of processing gain). Both analogue and digital sections are designed to operate at clock frequencies in the range 1 kHz to 4 MHz. The device is intended to be operated in 2 modes.

(1) As a correlator for baseband signals. Here, each digital bit is used to weight 2 analogue samples (i.e. two samples per digital bit), thereby satisfying the sampling theorem.

(2) As a correlator for bi-phase-coded or phase-shift-keyed (PSK) input signals. In this case each digital bit and its complement are used to weight a pair of taps.

2. General Description of 128-Stage Correlator

The device described is an arrayed structure where both digital and analogue functions are fitted into the CCD pitch of 28μm, resulting in a chip size of 166 x 108 thou. A chip photograph is given in Figure 1. A schematic diagram of the chip is given in Figure 2 which shows that the device can be split into the following sections.

A. 128-Stage Tapped CCD (127 Taps) In order to obtain good linearity a floating gate tapped surface channel CCD with diode cut-off input metering is used. The 128th tap is missed out so that the surface channels can be cascaded if necessary. A 4-electrode per bit structure is used (Figure 3) consisting of two clocked electrodes (ϕ_1 and ϕ_2), a DC phase, and a floating gate tap. This structure is chosen to minimise clock coupling to the tap.

B. Tap Weight Switches and Correlation Busses The taps are weighted by connecting them to either a positive or negative correlation buss by

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means of 127 pairs of tap-switches. A 1-bit (2-tap) section is shown in Figure 4(a). The bi-phase and baseband modes of operation require different tap-switch connection. A universal structure using 4 correlation busses (Figure 4(a)) is used which, by appropriate external connections, can form a bi-phase correlator (Figure 4(b)) or a baseband correlator (Figure 4(c)).

The tap-switch structure also contains the storage capacitors C_H (Figure 4(a)) which are used to store the reference digital code. The storage capacitors are connected between the tap electrode and the tap-switch gate. This minimises the effect of any voltage transients on the tap-switch resistance. The reference code is continually written inot the digital register and transferred onto the hold capacitors once per code period. The structure has been designed so that there is no significant change in the stored logic levels after 20 mS.

C. Digital Reference Shift Register The function of the digital shift register is to accept the reference code serially and present the data at parallel outputs. This data is then transferred onto the hold capacitors at the appropriate time by a set of parallel transfer switches. It is necessary for the digital register to be cascadable so an output buffer stage is included. Since on-chip power dissipation requirements rule out static shift registers, a fully dynamic 2-phase MOS shift register has been developed. This has to meet the parallel output drive requirements over a frequency range of 1 kHz to 4 MHz.

A 1-bit section of the shift register is shown in Figure 5, together with the associated clock and node voltage waveforms. It consists of a basic dynamic inverter stage T1 to T3, driving a self-bootstrapped push-pull stage T4, T5, which has a low output impedance in both logic states. Since the Q (node G) and $\bar{Q}$ (node D) outputs are valid during ϕ_1 and ϕ_2 high periods respectively two parallel transfer clocks ϕ_{TR1} and ϕ_{TR2} are required. The last stage of the digital shift register is modified to reduce its output impedance so that an off-chip capacitance of 10 pFs can be driven.

D. 128-stage Cascading CCD It is intended to cascade up to 16 chips (1024-bit pseudo random code) which results in a maximum of 4096 CCD transfers. To reduce the loss in processing gain to less than 1 dB a transfer inefficiency per stage of $<4 \times 10^{-5}$ is necessary. The tapped delay line uses a surface channel CCD in order to obtain good linearity but surface channel transfer inefficiency is too high for cascading purposes. Therefore, a special 128-bit buried channel CCD is included on the chip (Figure 2). This CCD operates with a single transfer clock (ϕ_1) and uses a 'fill and spill' input for optimum serial linearity. It is designed for a gain of 1.2 and incorporates a low output impedance buffer.

3. Output Sensing Circuit

The output signal is obtained by means of a differential charge amplifier (Figure 6). Switches S1 and S2 reset the two correlation busses to the tap reference voltage V_{REF}, which is normally equal to the DC phase potential. Switches S3 and S4 reset the integrators. When ϕ_1 goes low the signal charge is transferred under the floating gate taps, resulting in an image charge appearing on the feedback capacitors. This is equal to the sum of all the charge packets which lie beneath the tap electrodes connected to each integrator. The difference between these two output voltages is proportional to the correlation coefficient of the reference code and the signal.

4. Experimental Results

A. Tapped CCD The tapped CCD has been operated at clock frequencies in the range 1 kHz to 2 MHz. Linearity from input to tap was measured by operating the device as a low pass filter (all '1's digital refer-

ence code). The harmonic content of the output was measured for a pure sine wave input signal well within the filter passband. For a 3V p-p output signal (∿80% of full range) the 2nd and 3rd harmonics were 40 dB and 48 dB respectively below the fundamental. Figure 7 shows the harmonic performance of the tap and serial outputs as a function of input bias voltage for a tap output of 1V p-p.

Tap weight uniformity was demonstrated by replacing the sine wave with a square wave of period equal to the time length of the correlator. The resulting triangular output is shown in Figure 8 for a two-chip correlator. The two discontinuities are caused by the missing 128th taps.

B. Digital Reference Shift Register The digital shift register has been operated in a 2-chip correlator at clock frequencies from 1 kHz to 5 MHz. A photograph of the shift register output is given in Figure 9 (f_c = 4 MHz).

C. 128-bit Cascading CCD The buried channel cascading CCD has been operated at clock frequencies in the range 1 kHz to 2 MHz (2 MHz is the limit of the test board used) without any discernible degradation due to transfer efficiency. Linearity was measured using a clock frequency of 100 kHz and an input signal frequency of 110 Hz. For an output of 1.5V p-p (≈90% of full scale) the 2nd and 3rd harmonics were 40 dB and 49 dB respectively below the fundamental. A graph of harmonic distortion against input DC bias is shown in Figure 10.

D. Performance as a Binary Weighted Correlator To evaluate the devices the test circuit shown in Figure 11 was used which allows two chips to be cascaded to produce either baseband or bi-phase correlators with 254 taps. A code generator produces a 127-bit pseudo random code. The code is written directly into the digital reference register and a delayed version is used as the analogue input. This allows the auto-correlation peak to be shifted in time with respect to the parallel transfer pulses.

Figure 12 shows the auto-correlation response for a bi-phase correlator at a clock frequency of 200 kHz. Abnormally poor transfer inefficiency ($\sim 10^{-3}$ per transfer) has resulted in 15% reduction in the peak to sidelobe ratio compared with the theoretical value. Further samples are expected before the Conference. The two-chip correlator has been run at clock frequencies down to 500 Hz and up to 2 MHz without visible changes in the auto-correlation function. The peak to sidelobe ratio can also be maintained for an input signal range of 34 dB.

Figure 13 shows a baseband auto-correlation response where the reference code is alternately complimented. This results in alternate positive and negative correlation peaks.

5. Other Applications

The correlator chip can be operated as a transversal filter with tap weights of +1 or -1. An example of this is the low pass filter connection used in Section 4A. However, by using n chips in parallel (as shown in Figure 14 for n = 4) and applying a binary weighting to the input, a 64-tap transversal filter with coefficients of n bit resolution could be obtained.

6. Conclusions

A cascadable binary weighted analogue correlator chip has been designed, fabricated and tested over a clock frequency range of 1 kHz to 2 MHz. The digital reference code can be changed in 80 nS (ϕ_{TR} pulse width). The device has exhibited good linearity and dynamic range. The concept of using a cascadable device to produce longer correlators, than are practical on a single chip, has been proved. The possibility of using this device to realise a high speed programmable transversal filter has been discussed. Such a filter would offer a compact low power alternative approach to digital signal processing.

Acknowledgements

The authors wish to thank M.J. Davis for his assistance in the evaluation. This work has been carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD.

Reference

1. E.P. Herman, D.A. Gandolfo, A. Boornard and D.R. Stepps, "CCD Programmable Correlator" presented at 'CCD 76'.

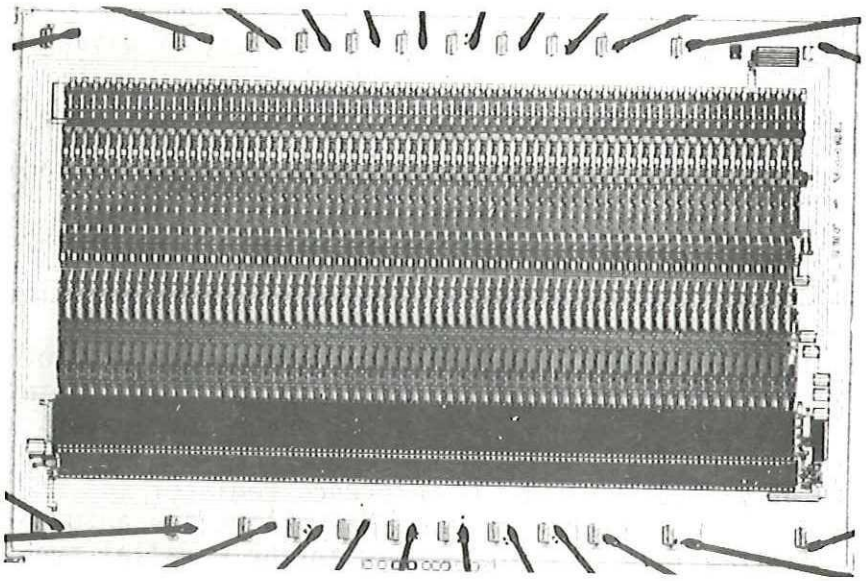


FIG.1. PHOTOGRAPH OF 128 STAGE CORRELATOR CHIP

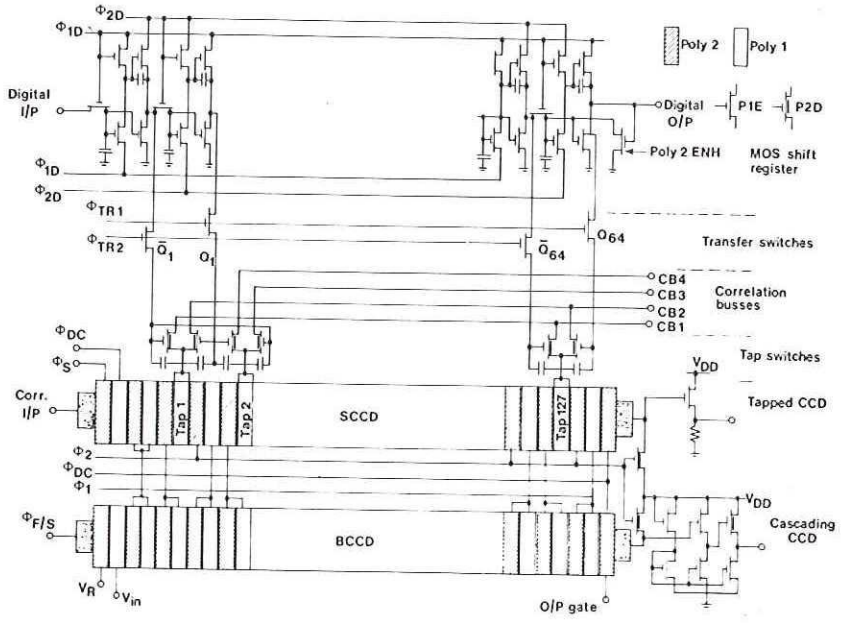


FIG.2. SCHEMATIC DIAGRAM OF THE CORRELATOR

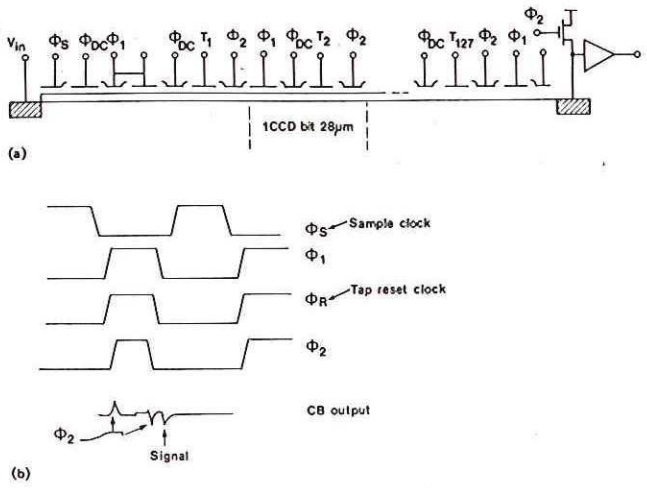


FIG.3. CROSS-SECTION OF SURFACE CHANNEL CCD AND CCD CLOCK WAVEFORMS

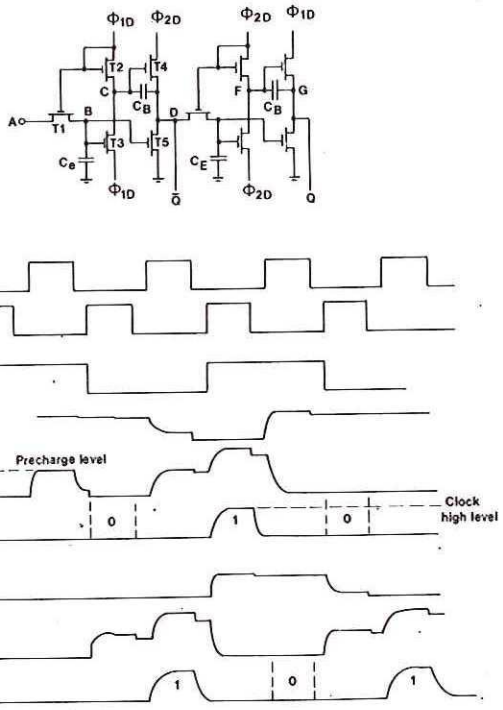


FIG.5. 1-BIT SECTION OF DIGITAL REGISTER

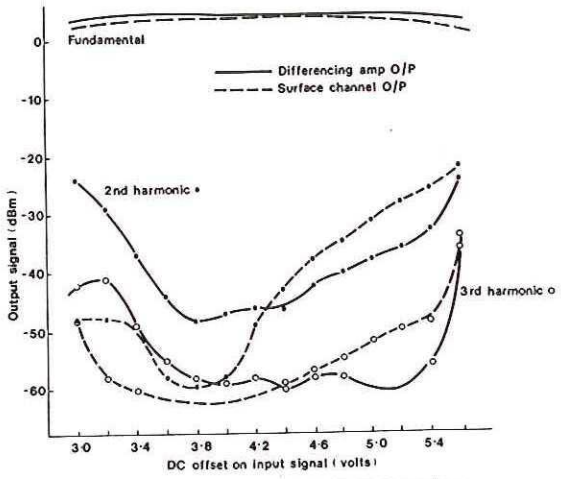


FIG.7. HARMONIC CONTENT AGAINST BIAS VOLTAGE FOR BOTH TAP AND SERIAL OUTPUTS

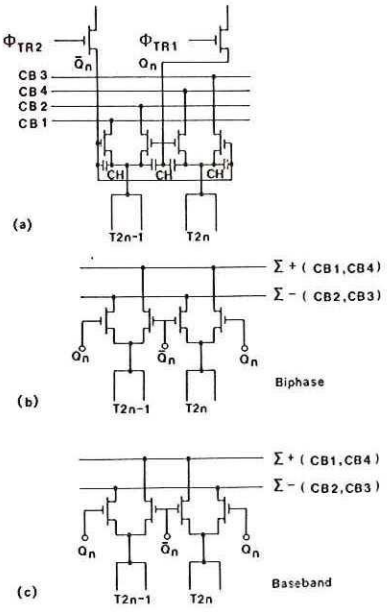
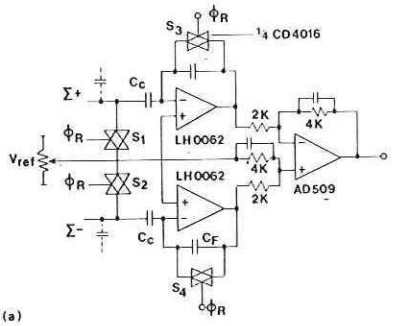


FIG.4. TAP SWITCH CONNECTIONS



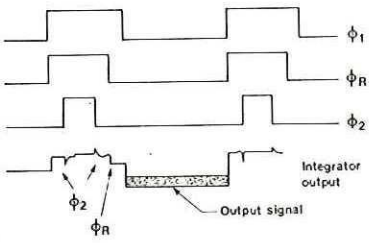


FIG.6. OUTPUT SENSING CIRCUIT

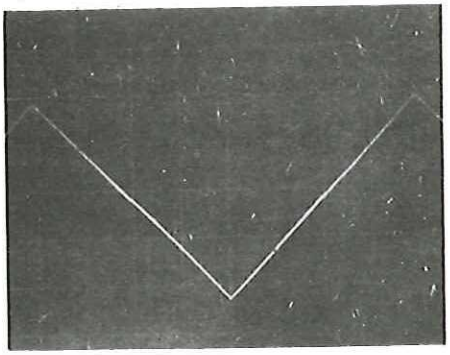


FIG.8. TAP WEIGHT UNIFORMITY FOR A 254 TAP CORRELATOR 0·5V/cm f_c = 200kHz

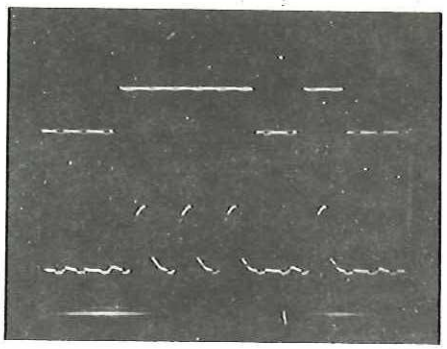


FIG.9 CASCADED DIGITAL REGISTER INPUT AND OUTPUT
5V/cm 0·2μS/cm

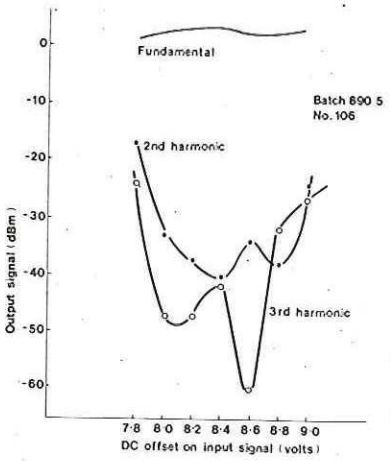


FIG.10. HARMONIC CONTENT AS A FUNCTION OF BIAS VOLTAGE FOR THE BURIED CHANNEL CASCADING CCD

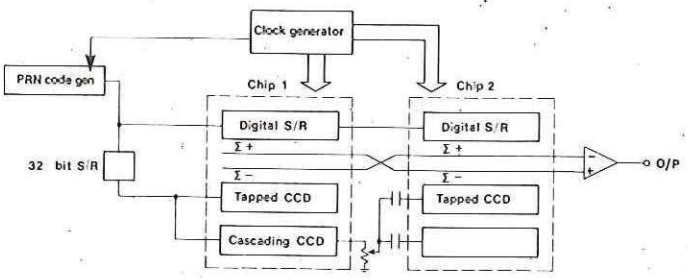


FIG.11. BLOCK DIAGRAM OF CORRELATOR TEST CIRCUIT

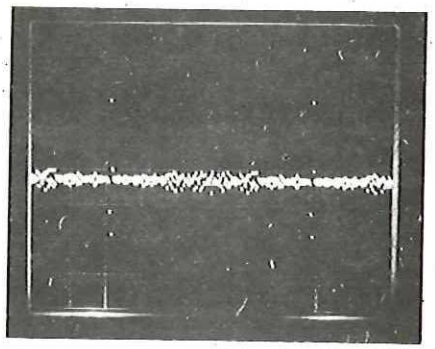


FIG.12. AUTO-CORRELATION PEAK FOR BI-PHASE CORRELATOR
0·5V/div 0·2mS/div, f_c = 200kHz

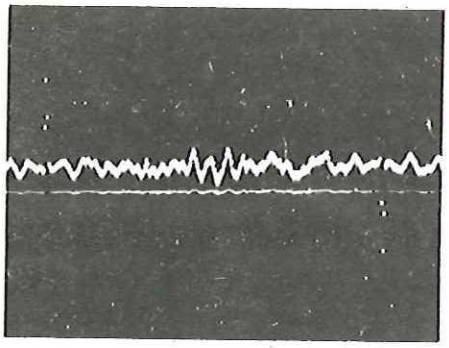


FIG.13. AUTO-CORRELATION PEAK FOR BASEBAND CORRELATOR
0·5V div 0·2mS div, f_c = 200kHz

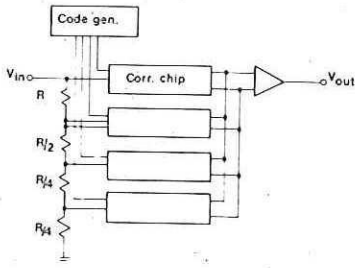


FIG.14. PROGRAMMABLE TRANSVERSAL FILTER