A FAST 32 POINT ANALOGUE CORRELATOR

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ABSTRACT

The design of a novel 32 point Correlator or programmable filter based on a new time delay and integration (TDI) structure is described. This device uses multiplying inputs together with charge summation within the TDI in contrast to more conventional cross correlators which employ tapped CCD delay lines linked with MOST analogue multipliers.

On-chip storage of the correlation coefficients and addressing circuitry for periodic refresh are additional features of this design. A key advantage of this architecture is the speed of multiplication (5-10 ns) inherent to the input technique. This enables high speed buried channel structures to be utilised.

INTRODUCTION

Charge coupled device technology has been widely used to implement various transversal filter designs[1,2,3], due to the simplicity with which delay and tap weighting may be provided. Tap weights may either be mask programmable (using a split electrode filter structure) or externally programmable by means of MOST multipliers on each tap. In addition to the obvious economic advantages of a single programmable design, the flexibility and adaptability of a programmable device, externally and intelligently controlled, provides extra incentive for its development.

A conventional correlator uses two tapped CCD delay lines or, more commonly one tapped CCD and a reference capacitor array. The CCD tapped delay line signal register gives a parallel output from a time sequence of signal samples. The correlation, or weighting coefficients, stored as charge in a bank of MOS capacitors, are then multiplied by the time sequence of signal samples and all the products summed to produce the filter output (Fig. 1a). Multiplications are performed

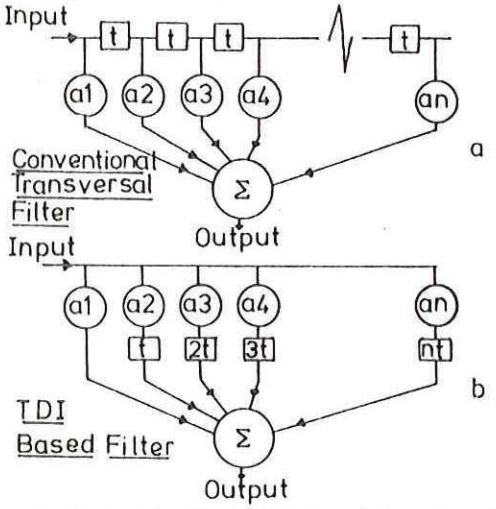

Figure 1 *Conventional and TDI Based Transversal Filter Structures.*

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using a single MOST multiplier at each tap point. Non-destructive signal tapping is usually implemented by a floating gate reset system in which charge packets are sensed capacitively via an isolated or floating CCD electrode, coupled to a high impedance MOST buffer amplifier[2]. These devices have fundamental speed limitations associated with the nature of this technique, though faster operation may be obtained in some structures by utilizing the parallel channel or split charge tapping method[4].

For many filtering applications the reference is stationary or quasi-stationary. This means that the delay elements (suitably modified) and multipliers may be interchanged (Fig. 1b). Implementations designed on this basis have not previously been particularly attractive since a large number of multipliers and delay elements are required. To overcome the problem of the large number of multipliers several separate approaches have been developed. One employs a single multiplier effectively multiplexed between channels[3]. For binary-analogue correlation, another technique uses a digital switch whereby the weighting, 1 or 0, multiplies the data input[5]. Alternatively, in a quasi analogue to digital manner, a number (depending on the weighting coefficient) of signal dependent charge packets are summed together in a common input storage well[6]. Due to the multiplexing nature of both these structures the bandwidth is considerably reduced.

The novel correlator described in this paper uses the configuration of Fig. 1b in a new way. Previous limitations on the number of multipliers and their speed of operation are overcome by utilizing multiplication directly in the input structure of a TDI register to provide fast formation and summation of correlation products. On-chip coefficient storage is provided by capacitors addressed and refreshed via digital registers. Thus high speed and bandwidth with simplicity of design is achieved.

MULTIPLYING INPUT TECHNIQUE

Previous techniques for charge injection into CCDs have been concerned principally with linearising the CCD transfer function[7,8]. The most commonly used methods involve setting the surface potential under an input electrode to equal that under an adjacent electrode at a different voltage by injecting an appropriate amount of charge under it. The value of this charge is then linearly related to the difference in applied potential on the two electrodes, one of which carries the input signal, the other a reference voltage. The multiplying input technique exploits the non linear properties associated with transient dynamic charge injection.

The operation of the multiplying input has been previously reported in the literature[9,10] and a brief explanation is given here. Consider a twin input gate CCD structure as shown in Fig. 2. The voltages V_D and V_C together with the duration of the strobe pulse are arranged so that charge

collected in the storage well, ϕ_1 does not come to equilibrium.

To a first order the input structure may be analysed as a MOS transistor. The charge collected in the storage well will be the integral of the current collected during the strobe pulse, and will contain a charge component representing the product $V_D \times V_C$, plus additional linear and squared terms. The desired multiplication term may be extracted by employing a time division multiplexing technique similar to that used for MOST multipliers.

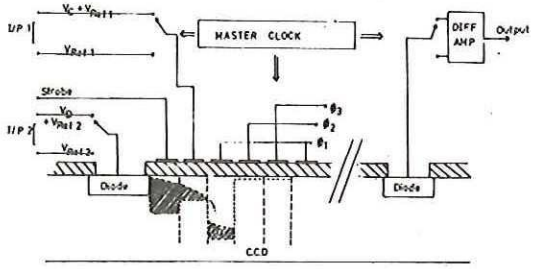

Figure 2 *Schematic Layout of a Multiplying Input CCD*

In this technique a succession of charge packets is produced by switching the input diode and second input gate to the potentials shown in figure 2. The diode may be set to a reference voltage V_{ref2}, or to the reference voltage superimposed on a signal V_D. Similarly the second input gate may be set to V_{ref1}, or to this reference superimposed on a signal voltage V_C. Initially both switches are set as shown in the diagram, with $V_{ref2} + V_D$ on the diode and $V_{ref1} + V_c$ on the gate. This produces, on strobing, a charge packet Q_M, containing a term proportional to $V_C \times V_D$ with others containing V_C or V_D only, and some independent terms. During the next clock pulse, after Q_M has been clocked forward, two charge packets are produced, by strobing twice during the same clock pulse, and summed in the same well to form a correction term, Q_C. The first of these, Q_{C1}, is produced with switch S_1 set at V_{ref1}, and S_2 set at its initial position, and the second, Q_{C2}, with S_2, set at reference level V_{ref2} with S_1 at its initial position. Thus, Q_{C1} and Q_{C2}, when summed, contain all the undesired linear and squared terms of the first charge packet Q_M.

Therefore in a normal linear CCD, pairs of charge packets arrive in sequence at the output. As shown in figure 2, the output may be switched to alternate inputs of a differential amplifier (on or off chip) resulting in subtraction of Q_C from Q_M, giving the desired product output. Figure 3 illustrates input, output and pulse sequences for a linear CCD operated in this mode. A dynamic range of 60dB with undesired harmonics less than 35dB may be easily achieved.

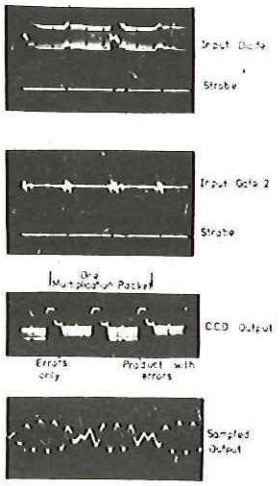

Figure 3 *Strobe, Timing and Input and Output Waveforms for a Multiplying Input CCD*

In our correlator the multiplying inputs to the TDI section operate in a manner identical to this description, followed by sequential addition of the product terms through the TDI.

TECHNOLOGY

The chip has been designed in a 3 phase, 3 level polysilicon technology which permits the fabrication of analogue (CCD and amplifier) components, together with digital registers on the same chip. Minimum dimensions of 3 μm are used, with < 1 μm alignment tolerances. The CCD gate electrodes are 7 μm in the main structure, giving a bit pitch of 21 μm with 5 μm input strobe gates for optimum performance. The shift register transistors are threshold shifted, by appropriate ion implants for optimum operation, and the TDI register is constructed in buried channel technology, but with surface channel inputs. A single self-aligned arsenic implant produces all sources, drains and CCD diodes.

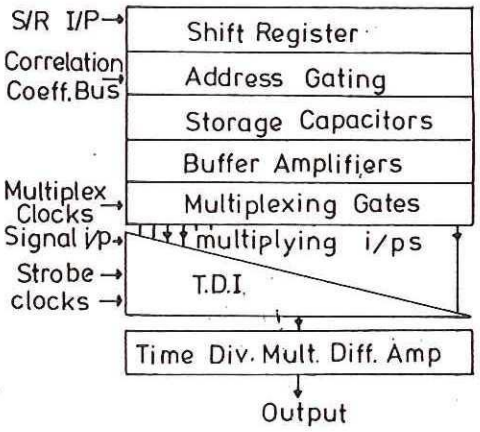

Figure 4 *Block Diagram of Multiplying Input Correlator*

Final metallization over a phosphorus doped flow-glass gives high metallization integrity.

CHIP ARCHITECTURE

A functional diagram of the correlator chip is given in figure 4. Initially the reference signal is fed, on a common metal bus, to a series of polysilicon storage capacitors, which are addressed sequentially by a digital shift register. This register has a design maximum clocking rate of 2 MHz enabling the 32 bits to be filled in 16 μsec. The storage capacitors are constructed in two levels of polysilicon to give maximum time between refresh cycles. The reference signals are fed from these capacitors to the second input gate of each TDI input via buffer amplifiers and multiplexing gates. These latter are required to implement the multiplication corrections described previously. Since the signal is represented by two charge packets, one representing the product plus errors, the other representing the errors alone, the inputs are necessarily spaced at twice the bit pitch of 21 μm.. The running data input is fed to the input diffusions of the individual TDI elements. If 4 quadrant, rather than 2 quadrant, multiplication is desired the diode switching process, discussed earlier, may be performed off-chip.

For elegance of design and economy of space, the TDI section has been divided such that signals fed into opposite halves approach a common output node in the centre. An additional benefit is the concomitant reduction in electrode width over a normal triangular TDI structure, which in turn reduces associated RC time constant effects.

At the output of the TDI, the sum of the correction terms and the sum of the multiplication products will appear in alternate clocking time slots. It is necessary, therefore, to store the values of one and subtract them from the other. This operation is performed using a time divisioned differential amplifier which employs a simple capacitive input differential circuit(11). Thus the output from the chip is the desired sum of products, emerging at half the TDI clock frequency.

Additional to the TDI register is a further 64 bit delay line which may be used for cascading these chips together.

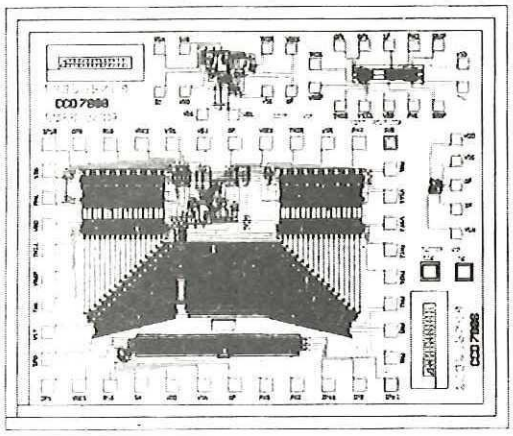

Figure 5 *Device Layout*

Figure 5 gives the chip layout. At A and A' is the shift register and addressing matrix with storage capacitors. These registers are necessarily divided into two sections due to the splitting in half of the TDI structure. The TDI is shown at B, B', and B''. B and B'' are 32 bit, 16 input sections wherein the signals travel from left to right and right to left respectively. B'' is an additional 32 delay section to give the correct total TDI function. Final addition occurs in the central node defined by the boundary between B and B'. The output from the TDI is fed to the differential amplifier C. At D is the 64-bit independently clocked delay line, provided for cascading purposes. Total active chip area is 2.5 mm x 3 mm.

Simulations indicate that the maximum operating speed of the prototype system is limited primarily by the output amplifier, which however should operate at speeds in excess of 20 MHz. In contrast to conventional structures, wherein the speed of the transfer registers is dominated by their floating gate reset tap structures (surface channel) and by the on-chip MOST multipliers, thus device can be fabricated in buried channel technology for rapid, high-efficiency transfer and addition. The multiplying inputs have already been demonstrated at speeds in excess of 100 MHz.

CONCLUSIONS

We have designed a new type of programmable filter or correlator structure, which is inherently capable of very high speed operation. Previous attempts at the design of correlators or programmable filters using floating gate tapped CCD registers with on-chip multipliers, while satisfactory for audio filters are inherently incapable of fast, high efficiency operation. Our structure avoids these limitations through the use of buried channel TDI for the summation, and high speed CCD input multiplication replacing the MOST multipliers. Since the analogue multiplication terms are generated in the CCD inputs. considerable silicon real estate savings and simplicity of design result.

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