

A HIGH SPEED CCD DIGITALLY PROGRAMMABLE TRANSVERSAL FILTER*

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ABSTRACT

A CCD transversal filter with digitally programmable taps is described. By means of on-chip digital circuitry the tap weights can be programmed to "0" or "1". Multiple filters can be constructed on a chip together with circuitry which scales and sums their outputs to produce a device with multi-level tap weights. In order to maximize the operating speed, the device maintains signals in the charge domain, with voltage-to-charge and charge-to-voltage transduction only at the input and output. Two prototype devices, a 32-stage by 1-bit and a 16-stage by 4-bit, have been built and tested at clock rates in excess of 10 MHz. The latter device consists of four 16-stage by 1-bit filters feeding a structure which scales and sums the charge packets to produce the output.

INTRODUCTION

Fixed tap-weight, CCD, finite impulse-response filters have been extensively investigated. Increased attention is now being directed to the more challenging problem of electrically programmable filters. Such filters are needed in applications using matched filtering, cross correlation and adaptive filtering. The goal of the work to be presented is the development of a transversal filter which combines the capabilities of high speed operation (clock frequencies of 10 MHz or more) and tap-weight programmability by means of on-chip digital control circuitry.

Most CCD transversal filters have been implemented in what we shall term the "transversal output" structure (Fig. 1a). The delayed signal is non-destructively sensed, multiplied by the tap weights, h_n , and the products all summed to form the output. In the CCD embodiment of this structure the tap electrodes are gates which are interleaved with the clocked charge-transfer gates. The capacitive coupling between the clocked gates and the tap electrodes is high, and this structure tends to suffer from clock feedthrough when operated at high clock rates. In some devices the tapped signals are sensed as currents which are then converted to voltages. The current-to-voltage circuitry is relatively more complicated and less amenable to high speed operation than the floating diffusion output commonly used in CCD delay lines.

The structure of Fig. 1b, to which we apply the term "transversal input", is functionally equivalent to the transversal output filter, but the delay and multiplication processes are done in reverse order. Fig. 1c is a previously reported structure¹ which falls in this category. It should be noted, however, that the tap weight multiplication can take place either at the inputs (as illustrated) or outputs of the delay lines, and therefore the structure can assume either transversal input or output forms. Note that these structures avoid the requirement of non-destructive sensing, and the output signal emerges from the device as charge. The charge detection can be done with the floating diffusion

*This work was sponsored by the Department of the Air Force.

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or floating gate output, which is structurally simple, can be well isolated from clock pick-up and has low capacitance to give large output voltages. A 32-stage device of the type in Fig. 1c was operated at clock rates up to 20 MHz¹. Other examples of previous work using the structures of Figs. 1b and c can be found in references 2-4.

DIGITALLY PROGRAMMABLE TAP WEIGHTING

Recent integrated CCD correlators have used MOS transistors as analog multipliers. Because of the bandwidth limitations of this type of multiplier, a new method has been devised whereby the tap weights are stored on-chip in digital form, and the multiplication can be performed without compromising the speed of the device. The digital format is particularly attractive in adaptive filtering where the weighting coefficients are obtained from a computational algorithm and are naturally available in a digital form. Fig. 2 illustrates the method by which the analog signal can be multiplied by 0 or 1. The input diode is tied to one stage of a shift register. The first ϕ_1 well draws charge from the diode only when the shift register output is in its low state as shown in the figure. This technique is adapted from a structure first described by Haken⁵ and has the attractive feature of eliminating a clock pulse which is necessary for other input methods.

Fig. 3 illustrates how a filter having multilevel tap weights can be made using the N-stage by 1-bit filters as the building blocks. Each tap weight h_n is expressed as an M-bit word,

$$h_n = -a_{n1} + \sum_{m=2}^M a_{nm} / 2^{m-1} \quad (1)$$

where $a_{nm} = 0$ or 1 and the two's complement representation has been used. Shift registers along the inputs to each section are serially loaded with the data bits a_{nm} . The signals from each of the M sections must be

scaled by the factor $2^{-(m-1)}$ from equation 1 and summed to produce the output signal $V_o(t)$. This weighted summation of signals can be performed in off-chip analog circuitry, but at the expense of additional components and power dissipation. A novel technique for performing this process in the charge domain on-chip is described below.

32-STAGE BY 1-BIT PROGRAMMABLE FILTER

A 32-stage filter with digital control circuitry was built using a CCD process which was compatible with NMOS logic processing. The chip consisted of two 32 by 1-bit filters each with a separate output. As previously described each filter section is capable of performing correlation of an analog input signal with a 32-bit binary sequence. A convenient method of evaluating this device is to subtract the output signals from the two filters, in which case programmable tap weights of "1", "0", and "-1" can be realized. Used in this manner the device functions as a ternary-analog correlator, and was used to demonstrate matched filtering of a 31-bit pseudonoise (PN) sequence. The 31-bits plus a zero bit were serially loaded into one shift register and the complement sequence plus a zero to the other. The output signals were subtracted in an external differential amplifier. The impulse response of the device is shown in

Fig. 4a, and in Fig. 4b the 31-bit sequence representing the time reversed impulse response was applied continuously as the input signal. The output has the characteristic uniform sidelobes and single peak as well as the peak-sidelobe ratio (31:-1) expected of the cyclic autocorrelation function of this sequence. The clock rate was 12 MHz.

16-STAGE BY 4-BIT PROGRAMMABLE FILTER

The structure of a filter having tap weights with M-bits of resolution has been outlined in Fig. 3 and requires the weighted summation of signals from M 1-bit filters. A method of performing this summation on-chip in the charge domain is described in Fig. 5. Each triangular 1-bit section has a long charge collection node along the outputs of the delay lines. This collection node consists of two diode diffusions separated by a gate, called a partition gate, forming transistor Q_p (Fig. 5). The operation of this circuit is in three stages beginning at a time when charge packets in the last storage well of the delay lines are ready to be transferred to the collection diodes and the partition gate is off. Note, the last storage well is controlled by a ϕ_2 clock. When the ϕ_2 clock and transfer gate go low, the charge from the N delay lines is transferred to the two collection diodes. Since each collection diode services a different set of delay lines, the partition gate must go on to allow charge exchange and to equalize the potential on the two diodes. The partition gate then turns off, the transfer gates (Q_{t1} and Q_{t2} in Fig. 5) go on and the separated quantities of charge are transferred, one to an output diode and the other discarded to the supply V_R . The portion Q_s transferred to the output diode is the desired signal, and is related to the total charge Q_T from the triangle section by $Q_s = C_2 Q_T / (C_1 + C_2)$ where C_1 and C_2 are the capacitances of each diode segment. The capacitance ratio $C_2 / (C_1 + C_2)$ is made equal to $2^{-(m-1)}$ to achieve the appropriate charge weighting dictated by equation 1. The charge from the remaining sections is similarly weighted and transferred to the same output diode where it is sensed by a conventional floating diffusion output circuit consisting of output and reset transistors Q_o and Q_r in Fig. 5. Though the additional clocked gates might seem to complicate the operation of the device, in fact the partition and transfer gates were clocked with the ϕ_1 and ϕ_2 CCD waveforms respectively.

The charge transfer through Q_p , Q_{t1} and Q_{t2} is much slower than the high speed transfer occurring in the buried channel CCD, and therefore the charge splitting process could become the limiting speed factor. Fortunately it was possible to design these transistors to have sufficient transconductance so that the device should perform satisfactorily at 20 MHz.

A 4-bit, 16-stage CCD programmable transversal filter has been built and tested to demonstrate the concept. A photomicrograph of this filter is shown in Fig. 6. The chip size is $3.3 \times 2.8 \text{ mm}^2$. Shift registers are located along the inputs to each of the four triangular sections. In addition, a set of latches is added as a buffer store between the shift register and CCD to permit faster updating of the digital weighting coefficients. In the present structure, the analog

signal applied to the section containing the most significant bits is not inverted, and the output of this filter section is brought out separately to be subtracted in an off-chip differential amplifier from the output of the remaining three sections. This inversion could be accomplished on the input analog signal (as depicted in Fig. 3) by the use of the fill and spill input operated in the inverting mode.

To demonstrate programmable matched filtering, the tap weights h_n , of the device have been programmed as a cosine down-chirp, i.e.,

$$h_n = \cos 8 \pi \left(\frac{15 - n}{16} \right)^2 \quad n = 0, \dots, 15$$

where the numbers, h_n , are truncated to 4-bit accuracy. The impulse response of the device is shown in Fig. 7b. When a negative cosine up-chirp

$$v_i(m) = -\cos 8 \pi \left(\frac{m}{16} \right)^2 \quad m = 0, \dots, 15$$

is applied to the CCD signal gate, the output of this filter is the expected correlation spike with sidelobes similar to their theoretical value, as shown in Fig. 7d at 10 MHz clock frequency. From the data of Fig. 8 it can be seen that 1% linearity with 50 dB dynamic range has been realized in this device.

SUMMARY

A CCD programmable transversal filter architecture has been described which, by maintaining the signals in the charge domain, allows relatively simple output circuitry and high speed operation. Two prototype devices have been described which demonstrate programmability of the tap weights by means of digital control circuitry and the weighted summation of charge from multiple 1-bit filters in order to achieve multi-level tap weights. Further work will be directed toward achieving a 32-stage filter with tap weights programmable as 6-bit words.

ACKNOWLEDGEMENT

We wish to thank W. McGonagle for the design of the test circuitry.

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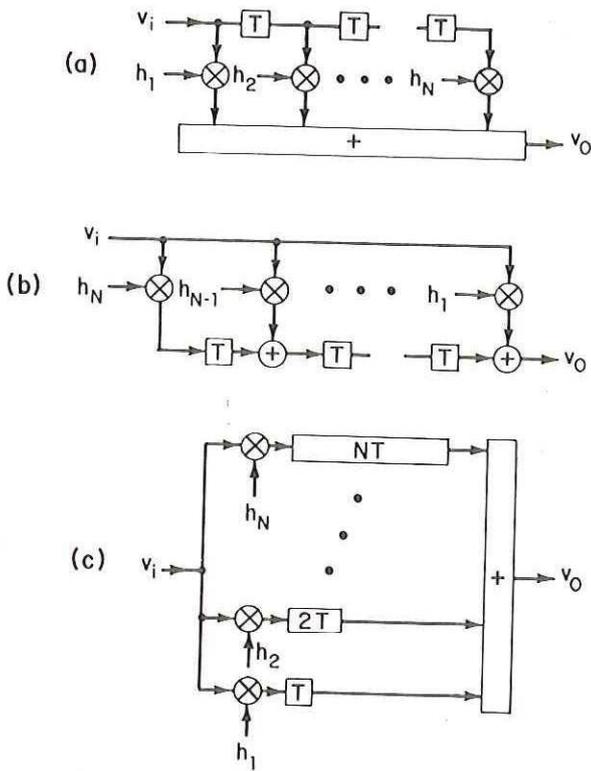


Fig. 1. Transversal filter architectures

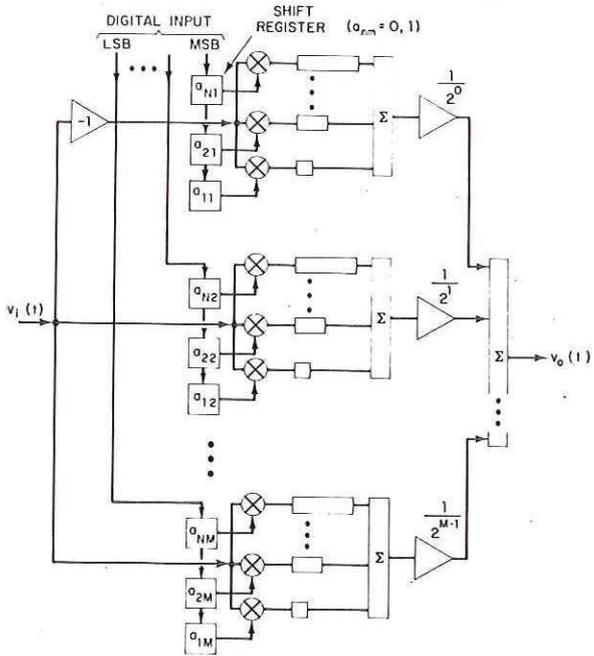


Fig. 3. A digitally programmable CCD transversal filter.

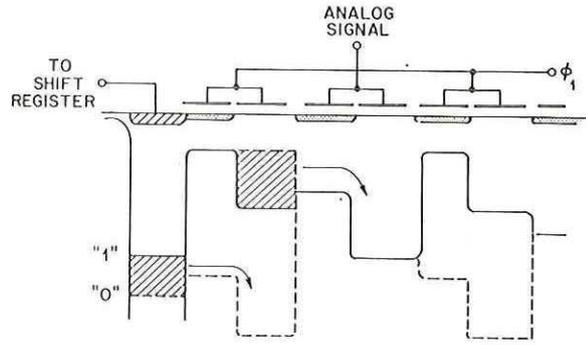
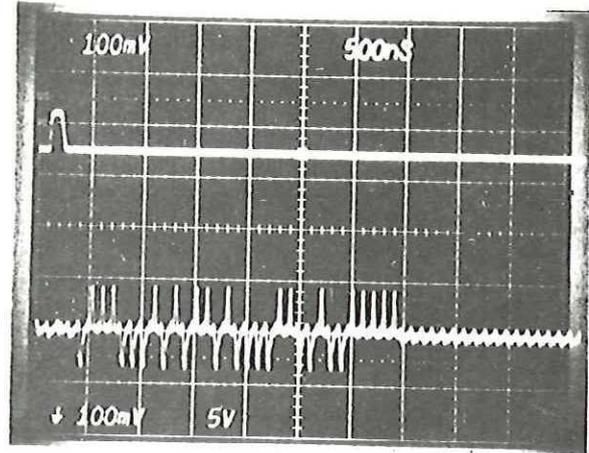
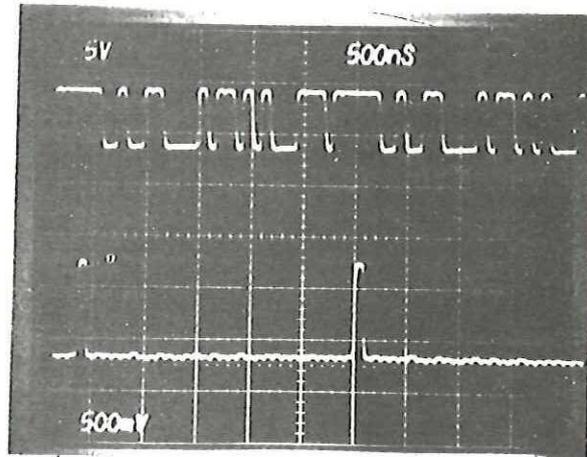


Fig. 2. CCD input method which allows binary multiplication of analog signals by means of a voltage on input diode.



(a)



(b)

Fig. 4. Example of programmable matched filtering using both sections of a 32-stage by 1-bit CCD transversal filter at 12-MHz sampling rate; (a) shows impulse response of device. In (b), analog input to device which is equivalent to time-reversed impulse response, and resulting output gives autocorrelation for this code.

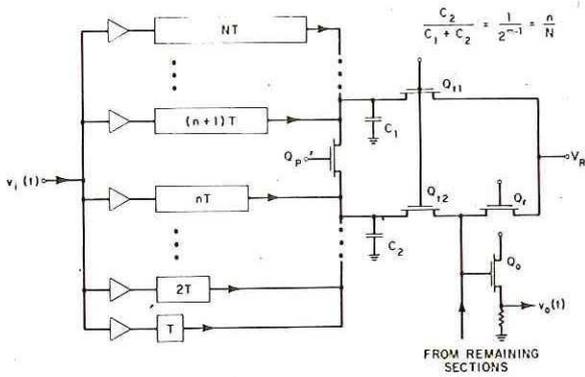


Fig. 5. A schematic of the on-chip, binary-weighted charge summation scheme.

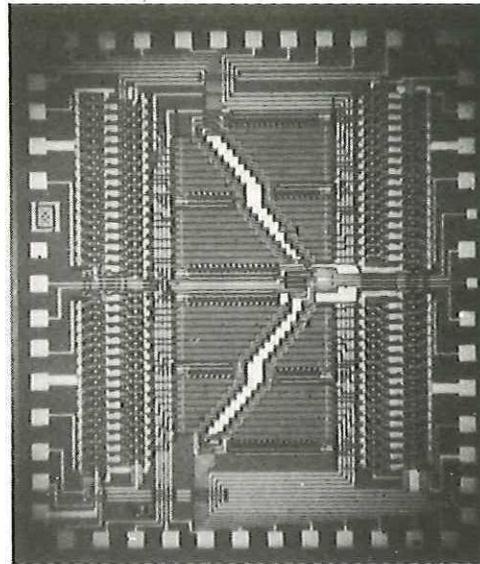


Fig. 6. Photomicrograph of a 4-bit, 16-tap CCD programmable transversal filter.

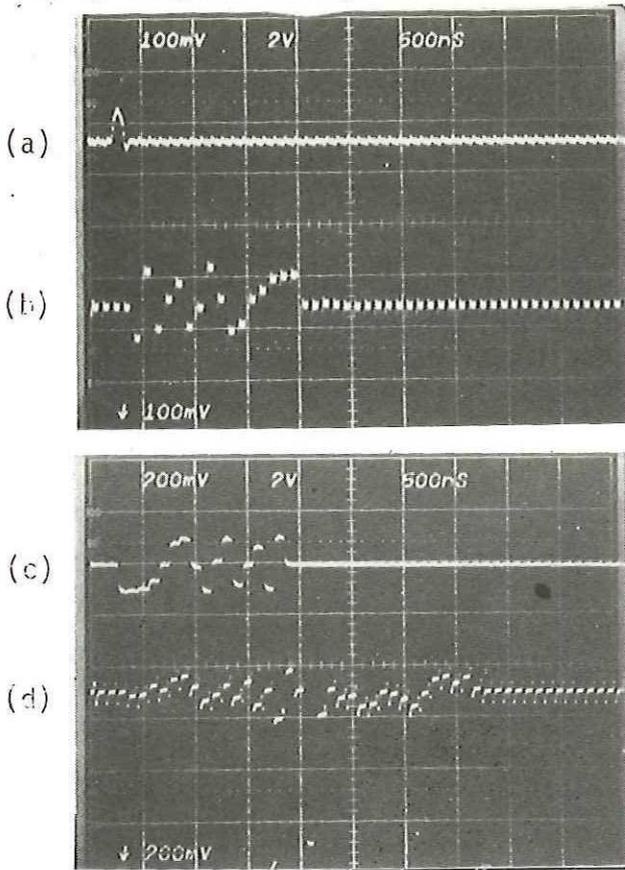


Fig. 7. Example of programmable matched filtering using the 4-bit, 16-tap device. (a) Excitation impulse (b) Impulse response of a cosine down chirp. (c) A negative cosine up-chirp is applied to the CCD input gate. (d) The output of this filter is the expected correlation spike with sidelobes similar to their theoretical values.

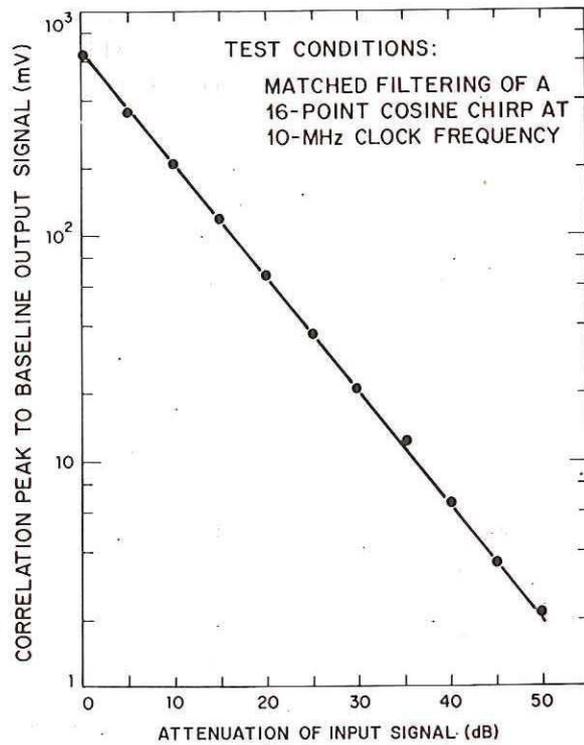


Fig. 8. Input, output linearity of the programmable matched filter.

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