DIGITALLY-CONTROLLED AND ELECTRICALLY-PROGRAMMABLE CCD TRANSVERSAL FILTER LSI

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ABSTRACT

This paper will describe about a 64-stage digitally-controlled and electrically-programmable CCD transversal filter LSI which is applicable for any analog signal processing. The LSI contains a 64-stage CCD transversal filter with quadrantally variable tap-weighting, tap-weight generator composed of 64 x 8-bit D/A converters and 64 x 9-bit static RAM's, clock pulse generator, other timing pulse generator, substrate bias generator, input bias circuit and output amplifier with sample-and-hold. The distinct features of the LSI are (1) compact filter structure using delaying, adding, subtracting and multiplying function of the CCD for quadrantally variable tap-weighting and (2) integration of the tap-weight generator using on-chip D/A converters and static RAM's for sure and stable operation of tap-weight-programming. Evaluation result indicates that the transversal filter LSI is very useful for various classes of the signal processing in video, audio and communication systems.

INTRODUCTION

The electrically-programmable transversal filter (EPTF) is an extremely useful device in various analog signal processing field. General classes of application are; (1) various kinds of frequency filter like low pass, band pass and high pass filter, (2) matched filter in spread-spectrum communication system and (3) automatic equalizer in video, audio and telecommunication systems. In first application, the EPTF can be accurately trimmed into any desired frequency response, compared with conventional LCR-filter. In second application, it is advantageous that the EPTF realizes the matched filter by only one device, compared with conventional filter bank method. The filter in third application must be fully electrically programmable for external control.

Charge-coupled device (CCD) offers an attractive approach to implementation of the EPTF. Since the CCD can directly deal the analog waveform without analog-to-digital converter and can easily integrate any MOS peripheral circuits on the same chip, we can probably obtain the very compact, low-cost and high-reliability filters. However, the CCD-EPTF in previous literature has generally consisted of CCD tapped delay line, MOS multipliers and MOS summing circuits. In this case, the transfer efficiency tends to deteriorate due to tapped CCD's structure using floating diffusion or floating gate. The chip size also tends to become larger due to complexity of on-chip MOS circuits for multiplying and summing. Another problem in the previous literature is to be necessary for many tap-weighting leads, which causes the increase of IC pin outs. One of the solutions to reduce the pin outs is to integrate a tap-weight generator like combination of C-memories and analog switches. By this way, each tap-weight can be programmed through serial analog data, however the analog data are only temporally stored in the C-memories and then they must

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be refreshed in an every short interval. To solve the above problems, a new type of CCD LSI has been developed.

CCD LSI ARCHITECTURE

The CCD LSI contains all peripheral circuits required for the CCD operation. The overall chip dimensions are 4.30 mm by 4.60 mm and about 2/3 of the chip area is occupied by the tap-weight generator to be described later. The CCD LSI configuration and the photomicrograph is shown in Fig. 1. The function of these elements are described below.

(1) The 64-stage CCD-EPTF consists of only a 64-stage CCD delay line with an input port at each stage. The EPTF action is achieved using delaying, adding, subtracting and multiplying function of the CCD. An output signal is sensed by means of a floating diffusion at a final stage. Details are described in next section.

(2) The tap-weight generator consists of 64 by 8-bit D/A converters, 64 by 9-bit static RAM's and two address decoders. The generator originates the control signals according to serial digital data, supplying each CCD stage. Details are also described in later section.

(3) The clock pulse generator originates two separate clock pulses from a sinusoidal clock signal input. One with one-phase is supplied the CCD of about 35pF capacitive load. Another with two-phase is used at the master clock of the other timing pulse.

(4) The other timing pulse generator has two kinds of pulse generator. One is for charge-injection/rejection in the CCD input ports. Another is for sample-and-hold of the output signal sensed at the floating diffusion. All pulses well operate by frequency of 15 MHz.

(5) The substrate bias generator originates a constant voltage of about -5V by means of the clock pulse rectification, supplying the substrate.

(6) The input bias circuit automatically generates optimum input DC bias level for wide dynamic range and high linearity.

(7) The output amplifier with sample-and-hold, receiving the signal sensed by the floating diffusion, increases the signal voltage and current, and reduces the clock pulse component.

The LSI was fabricated using double poly-Si BCCD/NMOS process and one level poly-Si with high resistivity is used for load resistors of the static RAM circuits.

CCD-EPTF OPERATION

The CCD-EPTF operates according to variable charge injection/rejection method in principle, as shown in Fig. 2. Each stage of the CCD-EPTF consists of two identical multipliers modulating an input signal V_{in} by a control signal V_{hk} to produce any weighted charge-packet, a subtractor rejecting the weighted charge-packet from the stage and an adder injecting the weighted signal charge to the stage. In this configuration, an output signal obtained at a final stage is represented by

$$V_{out}(nT_c) = \sum_{k=1}^{M} C_1 \cdot V_{hk}(+) \cdot V_{in}[(n-k)T_c] - \sum_{k=1}^{M} C_2 \cdot V_{hk}(-) \cdot V_{in}[(n-k)T_c]$$

where V_{in} (kT_c) is a sampled input signal and T_c is a unit delay time. This equation shows that the schematic diagram in Fig. 2 is exactly identical with a conventional transversal filter.

Electrode arrangement of the CCD-EPTF is shown in Fig. 3. From first stage to final stage, signal charge-packets are transfered by a clock pulse ϕ_1 and a constant voltage V_2. In any stage, first, a preceding ϕ_1 electrode charge-packet is transfered and stored into a V_2 electrode through an input gate applied an input signal V_{in} and a control gate applied a control signal $V_{hk}(-)$ when the ϕ_1 pulse goes down. A remained charge-packet in the control gate is rejected into a drain through a shift gate when a shift pulse ϕ_{SF} goes up, whose amount equals product of well capacitance of the control gate and channel potential difference between the input gate and the shift gate. Since the well capacitance is approximately proportional to the control signal, the rejected charge-packet is also proportional to product of the input signal V_{in} and the control signal $V_{hk}(-)$. Second, the V_2 electrode charge-packet is transfered and stored into next ϕ_1 electrode when the ϕ_1 pulse goes up. Simultaneously, a stored charge-packet in another control gate is injected into the ϕ_1 electrode through another shift gate when the shift pulse ϕ_{SF} goes up, according to the well-known Fill and Spill method, whose amount is determined by the same way as described above. Therefore, the injected charge-packet is proportional to product of the input signal V_{in} and another control signal $V_{hk}(+)$.

Advantages of the CCD-EPTF are (1) high packing density because of eliminating MOS multiplier and adder, (2) high speed operation due to no floating diffusion or floating gate structure for any tap-lead and (3) complete quadrature-weighting using the variable charge injection/rejection method. An example of the CCD-EPTF operation results is shown Fig. 4 where (a) is positively-weighted output waveform and (b) is negatively-weighted output waveform in first stage input (64-stage delay) at clock frequency of 10 MHz. Gain control characteristics is shown in Fig. 5, where (a) is for positive-weight and (b) is for negative-weight. Although the gain is smoothly changed in a control voltage range between 4V and 12V, the gain characteristics becomes steeper near cut-off and then, second harmonics is increased there.

TAP-WEIGHT PROGRAMMING

The control signals are originated by the on-chip tap-weight generator which basically consists of 64 by 8-bit ladder network D/A converter is schematically shown in Fig. 6. An end of each ladder resistor 2R is connected to V_{dd} or ground by corresponding switch SW_{ik} which can be controlled by corresponding memory M_{ik} data. In this configuration, the ladder network output is represented by

$$V_{hk} = \sum_{i=1}^{8} \frac{V_i}{2^i}$$

where V_i=0 or V_{dd}. Another switch SW_{0k} is used as tap-weight polarity selection, which gives one control gate a V_{hk} and another control gate a ground voltage.

Figure 7 shows more detailed circuit diagram of the tap-weight generator. A X- and a Y-address decoder select any memory which is a conventional static random access memory (SRAM) consisting of four transistors and two resistors, in which the external digital data are written and statically stored. A pair of opposite-sign data stored in the SRAM is given to a pair of transistor switch and a end of the ladder resister is connected to either V_{dd} or ground. A control voltage made by the ladder network is selectively given to either the positive or the negative control gate of the CCD-EPTF and simultaneously, ground voltage is given to another control gate, by means of four transistor switches controlled by another SRAM output. To reduce the power dissipation and the chip area, high-resistive poly-Si was used as the ladder resistors and the SRAM load resistors. The ladder network D/A converter accuracy mainly depends on scattering of the poly-Si resistivity.

Advantages of the digital programming method for the CCD-EPTF are (1) stable and sure operation compared with the analog programming method like combination of C-memories and analog switches and (2) compatibility for other conventional digital system like a micro-processer and a digital memory. The programming function has been experimentally confirmed using a simple data generator which has 11 control outputs with TTL levels, in which one is for polarity selection, 3 for tap-weight selection, 6 for stage selection and one for data input.

CONCLUSION

A 64-stage digitally-controlled and electrically-programmable CCD transversal filter LSI has been developed. Complete quadrature-weighting of the EPTF has been achieved using the variable charge injection/rejection method of the CCD. Digital tap-weight programming of the EPTF has been achieved using on-chip tap-weight generator of 8-bit ladder network D/A converters. Evaluation results show that the transversal filter LSI is extremely useful device in various analog signal processing.

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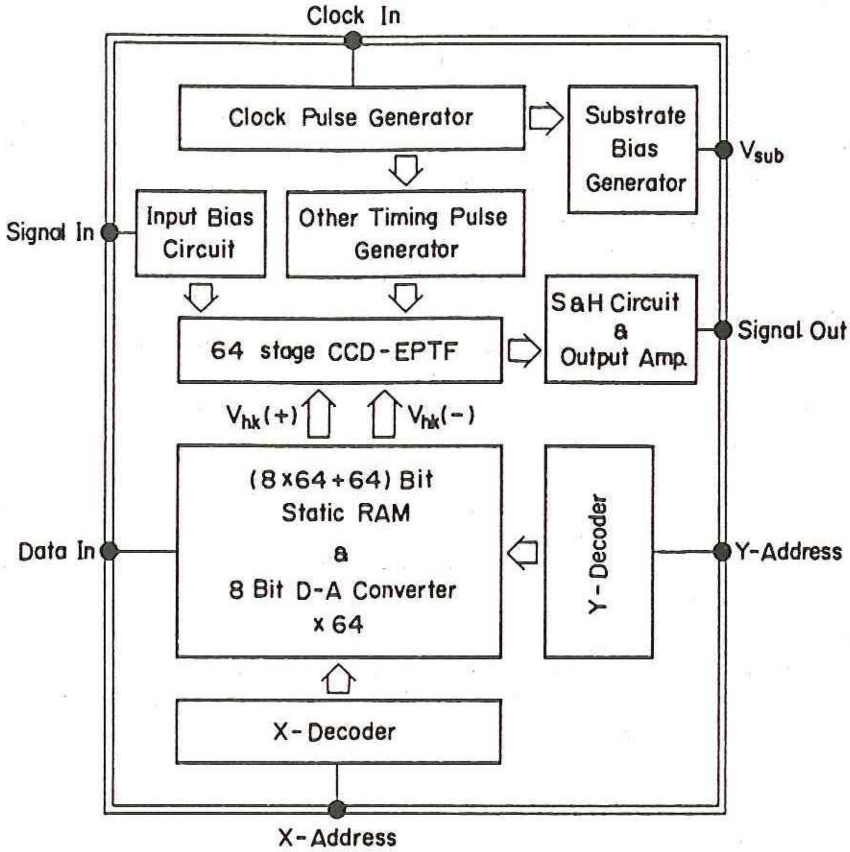
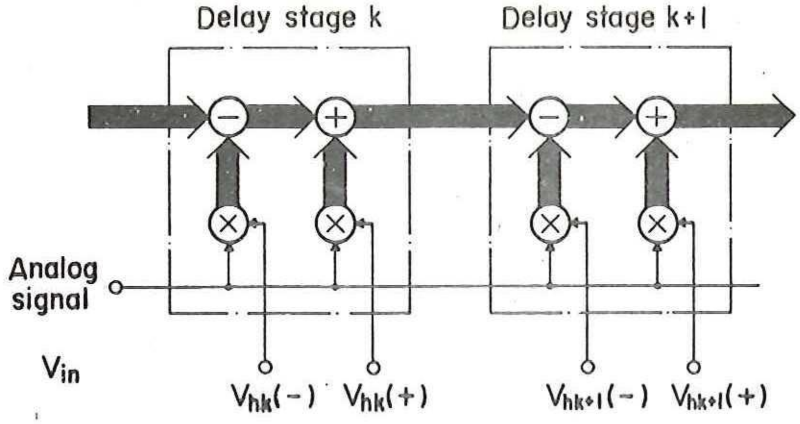


Fig. 1 CCD LSI configuration



$$V_{out}(nT_c) = \sum_{k=1}^{M} V_{hk}(+) \cdot V_{in}[(n-k)T_c] - \sum_{k=1}^{M} V_{hk}(-) \cdot V_{in}[(n-k)T_c]$$

Fig.2 Schematic diagram of the CCD-EPTF

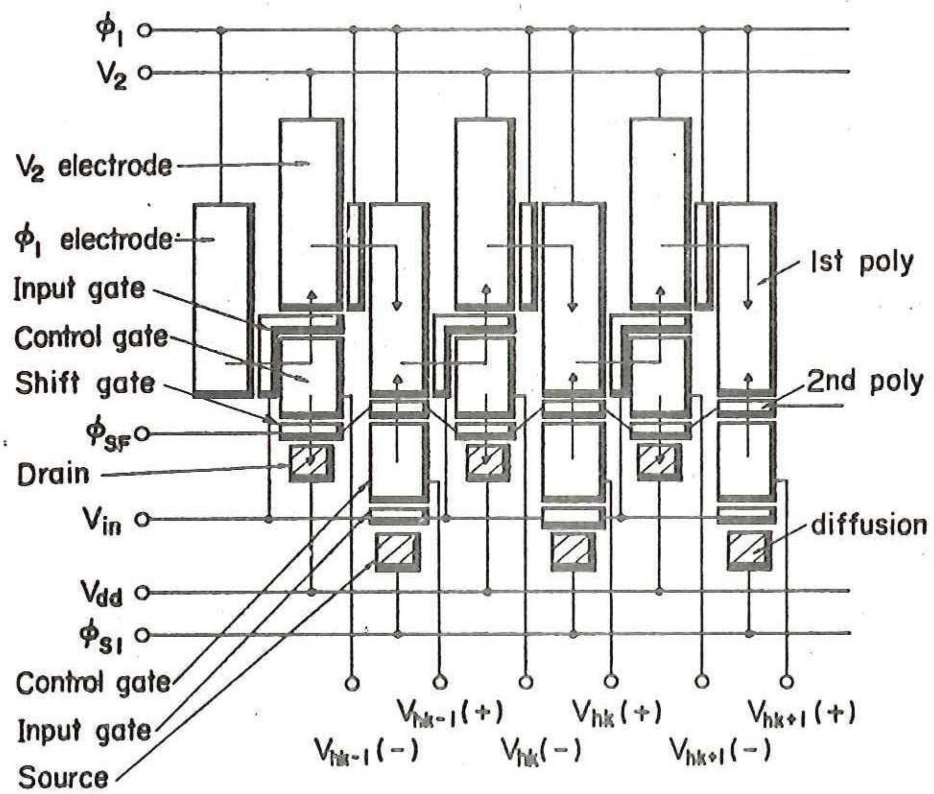


Fig.3 Electrode arrangement of the CCD-EPTF

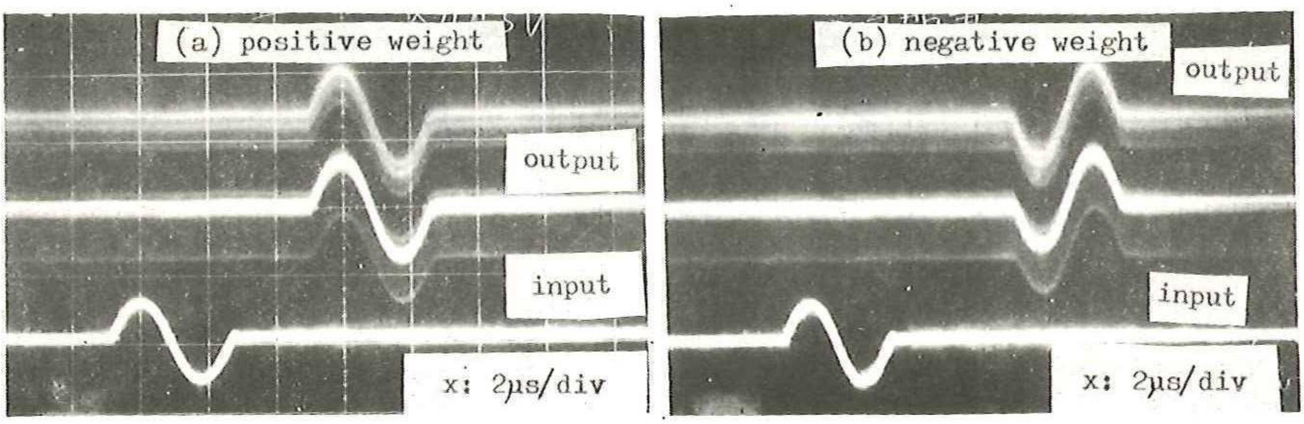


Fig.4 Output waveform of the CCD-EPTF

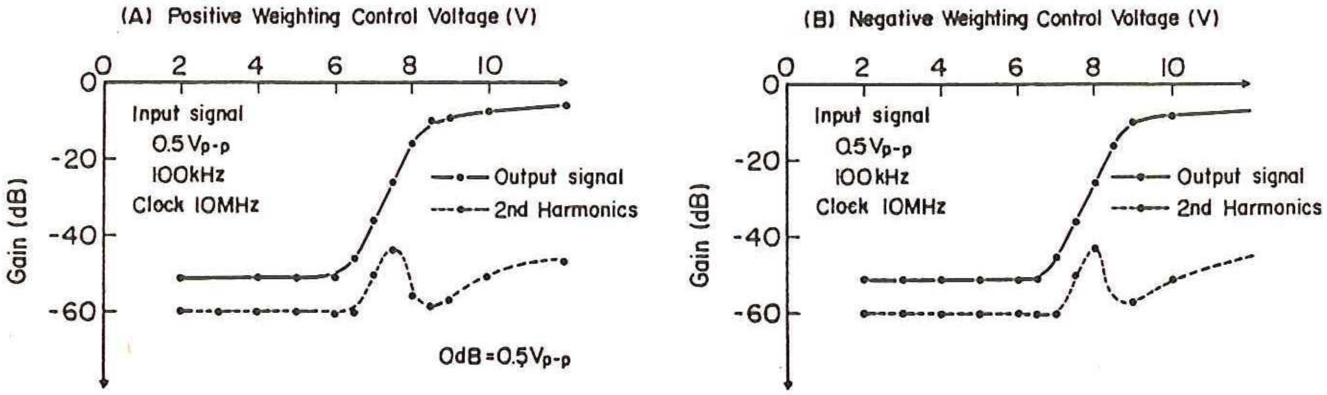


Fig.5 Gain control characteristics of the CCD-EPTF

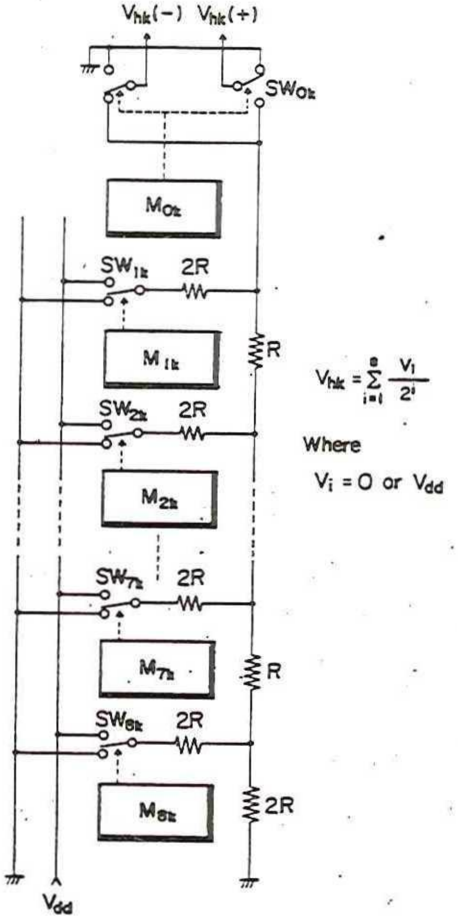


Fig.6 Schematic diagram of the 8-bit ladder network

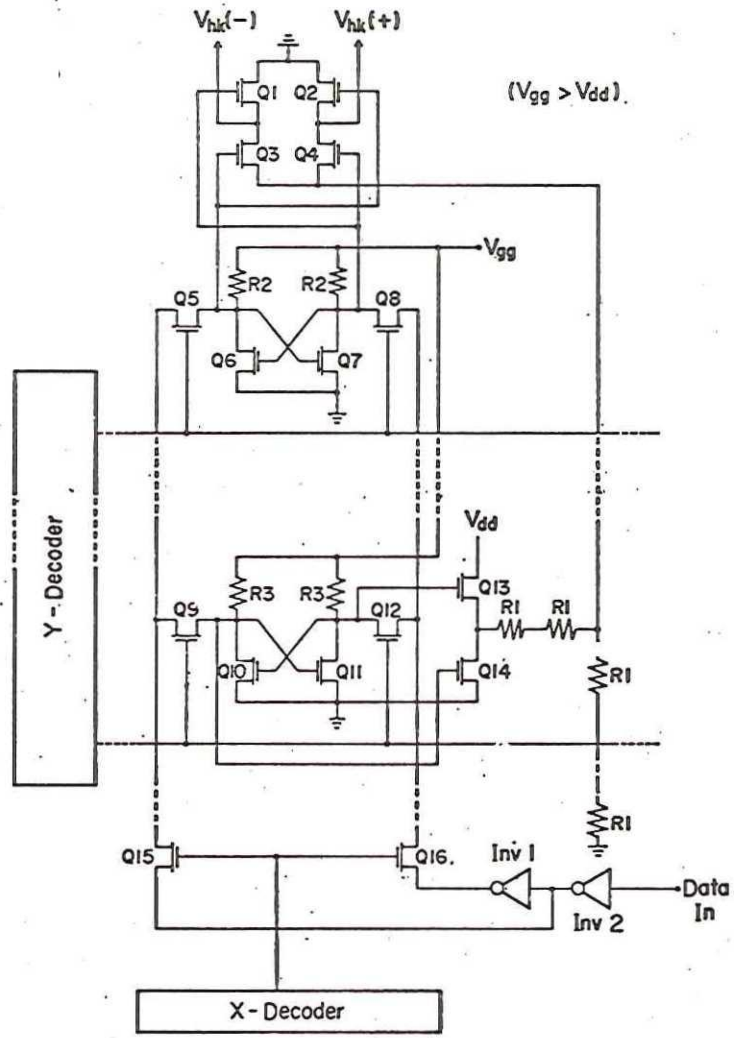


Fig.7 Circuit diagram of the tap-weight generator