PROGRAMMABLE TRANSVERSAL FILTERS: DESIGN TRADEOFFS

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Abstract

Various architectures for realizing transversal filters will be reviewed. Real-time programmability of the tap weights will be of primary interest with several implementations being discussed. Design tradeoffs dictated by the requirements of specific applications will also be presented.

Introduction

The purpose of this paper is to review various approaches which have been proposed for the realization of programmable transversal filters. A variety of architectures will be reviewed with their inherent advantages and/or limitations discussed in light of particular types of applications. The key feature of the devices to be discussed is their programmability. This feature may be divided into three types:

1. Fixed Programmed
2. Field Programmed
3. Real-Time Progammable

The simplest type, of course, is the fixed programmed type. For this case the tap weights are determined during design and are permanently fixed at that time. Figure 1 shows a photograph of a completely integrated, 64-tap, transversal filter which is being used in a wide variety of applications where its unique characteristics are required.

A second fixed programmed transversal filter is shown in Figure 2. This device consists of four transversal filters, each having 512 taps. This device was intended primarily to be used to implement the convolution portion of the Chirp Z Algorithm; a form of the discrete Fourier transform. These four filters, together, perform 2048, 8-bit multiplication and adds each sample-time which demonstrates the power of parallel processing possible with charge transfer devices.

The field programmable structure can be programmed by the user. Although the delay line is already tapped, the tap weights required for a particular application are fixed, i.e., a set of resistors. These tap weights can be changed but require the user to change components, i.e., resistors in the above example and is definitely not real-time programmable.

The most versatile transversal filter is one which possesses the ability to be real-time programmed. This opens an extremely broad range of applications which include adaptive systems, the systems which have the ability to learn from past experiences.

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In this paper we will not discuss the fixed programmed structures; nor will we discuss binary weighted programmable structures. We will mainly concentrate on the real-time programmable structures with analog tap weights.

Basic Architecture For Transversal Filters

The basic operation implemented by the transversal filter is that of parallel multiplication of lagged or delayed samples of an analog signal by an array of predetermined multipliers followed by the summation of these products. This is shown mathematically by an equation:

$$F(k) = \sum_{k=1}^{N} h(n)f(k-n)$$

Figure 3 shows a tapped delay line. The output of each tap is multiplied by a factor h(n), and the individual products are then summed. We can easily see that the equation will result.

Two configurations (See Figs. 4 and 5) may be used to implement the basic function of the tapped delay line. Most often one thinks only of the serial-in-parallel-out, SIPO; however, its dual, the parallel-in-serial-out, PISO, quite often is a more suitable architecture for a particular application.

Although the function is the same, there may be a preferred architecture for realizing the particular configuration. An example is the PISO, which can be implemented using a single delay line with the parallel inputs spaced along the line as depicted in Figure 5, or it can be implemented using a separate delay line for the realization of each lagged product as shown in Figure 6. Such an architecture is for obvious reasons referred to as a 'pipe organ' structure. This structure offers several distinct advantages over either the simple PISO described above or the SIPO.

For instance, in high speed applications, it is often easier to implement the PISO configuration. The implementation of taps along a delay, as in the SIPO configuration, can adversely affect the high speed transfer efficiency of the delay line. Furthermore, the difficulty of signal extraction from a SIPO structure increases rapidly as the sampling ratio increases. This is a result of the high impedance level of the conventional tap structure and complexity of the clocking required to operate the tap structure. The PISO does not suffer these problems, since the output circuit is a simple summing node similar to the output of any high speed delay line. In the PISO, pipe organ configuration, the weighting is at the input which in the normal situation is driven from a variable gain voltage source which presents a much lower impedance to reduce the susceptibility to parasitic pickup of clocking signals.

The simplicity offered by the pipe organ structure is paid for, however, by the increase in silicon real estate necessary for its realization. This may very well be a small price to pay for the simplicity and/or the performance that one realizes.

Real-Time Programmable Transversal Filters

The real-time programmable filter can be realized by a variety of structures. Figure 7 shows block diagram representation of three approaches which have been received considerable attention. The first approach uses two charge transfer devices, each with sequential taps. These taps nondestructively sample the analog signal as it is clocked down the charge transfer device. Each pair of adjacent taps, i.e., the n^{th} tap on each CTD forms the two inputs to the four quadrant analog multiplier. Each multiplier consists of matched MOSFETs operated differentially in the quasi-linear device region. The inputs provided by CTD "A" each have a sample and hold which allows a parallel update of all tap weight values in a fraction of one sample period through a clocked transfer gate. With the sample and hold turned "off", tap weights serially transfer from one end of the finite structure to the other to compute the real-time convolution or correlation of two analog signals. A photograph of a 32-stage analog-analog convolver is shown in Figure 8. Due to uncompensated variations between taps, the performance of this device is limited to about 40dB. More recently, similar devices have been made where the taps are implemented on alternate stages rather than every stage of the CTD; then, by alternately sampling a reference between each sample of the signal, it is possible to compensate at each tap for tap-to-tap variations. More elaborate schemes have been proposed; but, to date, no results have been reported. One such proposal employed a bridge circuit at each tap and two CTDs to supply differential inputs to each bridge circuit.

A much simpler structure has been developed at the University of Edinburgh.[1] A schematic representation is shown in Figure 9. In the structure, the multiplication is performed by a single MOSFET. Tap weights are stored on capacitors where a unique feedback technique is employed which compensates for tap-to-tap variations that affect the actual tap wieght values. These memory capacitors constitute one input to each multiplier. The other input to each multiplier is supplied from a tap on the CTD and is uncompensated. These uncompensated variations appear as tap weight errors in the impulse response and, therefore, limit the performance. A solution to correct these variations uses a stored impulse response to generate an error signal which is used to modify the tap weight values read onto the tap weight capacitors. This technique has been used in the laboratory; however, it is somewhat cumbersome to implement in a real application.

Figure 9 shows the functional block diagram of a recently developed programmable transversal filter which interfaces naturally with a microprocessor. Three configurations are available: 1) 16 tap assymetrical impulse response to realize adaptive equalizers; 2) 32 tap symmetrical impulse response for linear phase transversal filters; and 3) 16 input time-delay-integration function where each input can be independently weighted to perform adaptive beamforming.

The architecture used to implement this function is that of a parallel-in-serial-out delay line; however, a pipe organ implementation was actually used. Each of the 16 inputs is weighted by a multiplying D/A converter (MDAC). The signal or reference input to the MDAC is an analog sample from the delay line. The MDAC output is related to the input by a multiplicative factor which is supplied as a digital word.

This word is stored in a static digital latch and can be updated by use of a tap select control bus. The MDACs are implemented using ratioed capacitors and have an accuracy of 8 bits plus sign for a 9-bit resolution. For 4 quadrant multiplication, offset binary representation of the tap weights is utilized. The tap weight values are stored in an on-chip RAM which can be updated at a 500KHz rate. This device was designed with several applications in mind. At room temperature, its sampling rate ranged from 50 samples per second to 600K samples per second. To realize the low sampling rate without the necessity of external cooling, the use of a bucket-brigade structure for the charge transfer device is needed. A unique feature of BBD allows one to pad each node with additional real capacitance, thus increasing retention time of each node. Figure 10 shows a cross section of the BBD structure showing how this may be accomplished. Since this cannot be accomplished with CCD, there was no choice but BBD. Either structure was possible with the chosen process.

A high sample rate application necessitated the use of an MDAC on each input as in Figure 11. From a cost standpoint, it is desirable to time share or multiplex one or more MDAC, as shown in Figure 12. This would save silicon area and allow the use of higher accuracy MDAC. A restriction on the sample rate of a multiplexed structure to 1MHz/MDAC would not meet the 600KHz sample rate requirement.

A chip photograph of this device is shown in Figure 13. The die, since it has to accommodate 16 MDACs is rather large; however, as is evident, a large part of the chip has only the tap select and tap weight data busses, therefore not significantly affecting the yield.

The chip offers the versatility necessary to implement a wide range of adaptive systems. Its digital interface allows it to be used in conjunction with a microprocessor, thus allowing the optimization of truly "smart" signal processing systems.

Conclusion

A designer's choice of architecture for implementation of programmable transversal filters depends heavily upon the degree of flexibility expected. Each structure discussed has advantages for its particular range of performance. Although a finite limitation on device size is fundamental, functionality need not be restricted to only fixed tap weight structures. Fully programmable capability is limited primarily by analog accuracies and speed in the required parallel multipliers.

Reference

1. J. Mavor and P.B. Denyer, "Design and Development of C.C.D. Programmable Transversal Filters", Electronic Circuits and Systems, Vol. 2, No. 1, pp 1-8, January 1978.

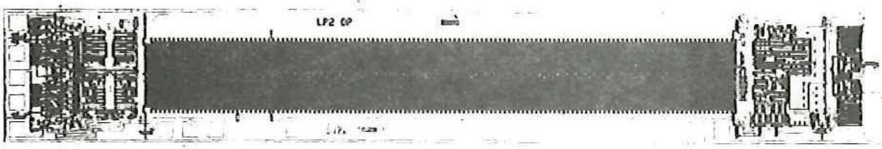


FIG. 1 Fully Integrated 64 Tap Transversal Filter

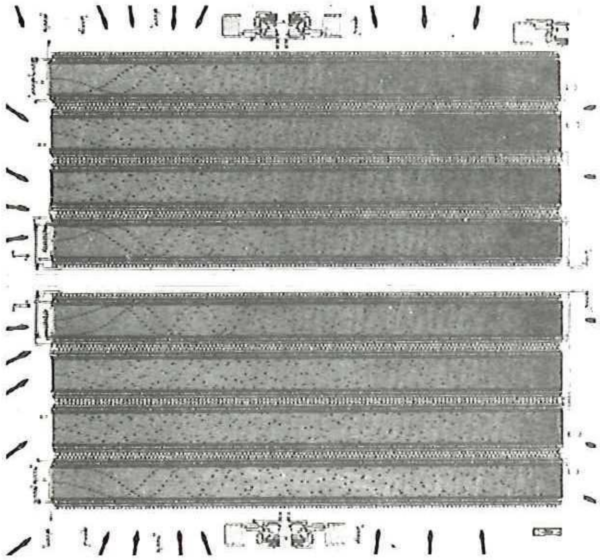


FIG. 2 Quad 512 Tap Transversal Filter

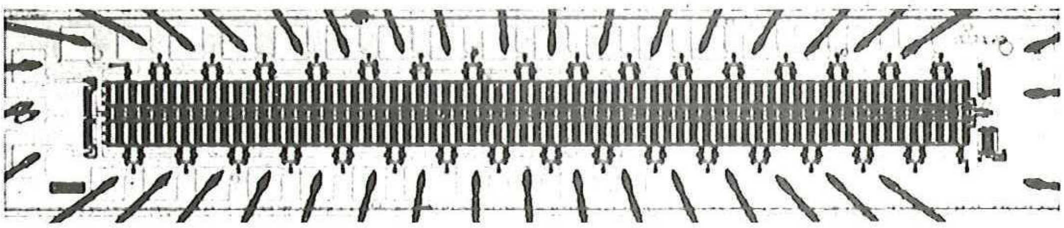


FIG. 3 32 Tap Delay Line

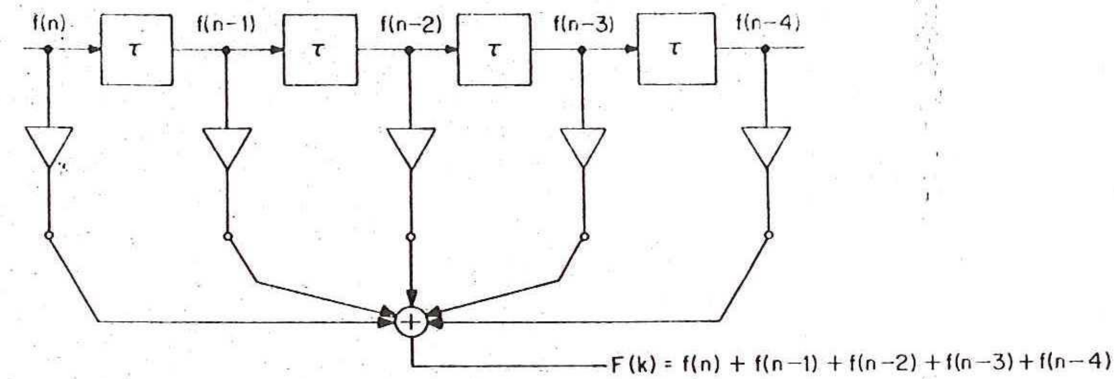


FIG. 4 Serial-In Parallel-Out (SIPO) Tapped Delay Line Structure

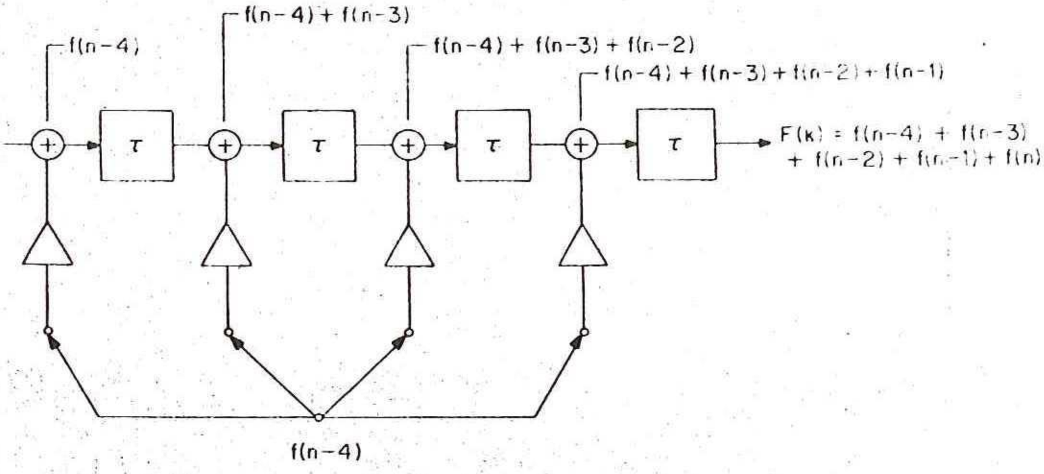


FIG. 5 Parallel-In Serial-Out (PISO) Tapped Delay Line Structure

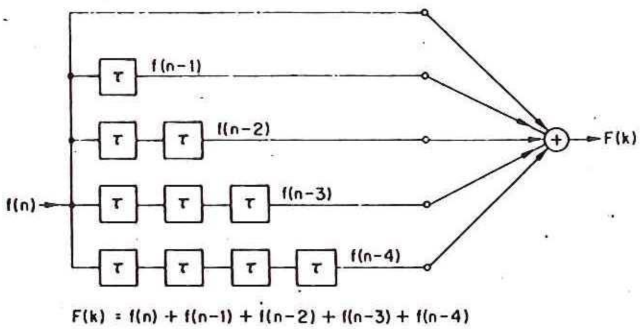


FIG. 6 PISO 'Pipe Organ' Structure

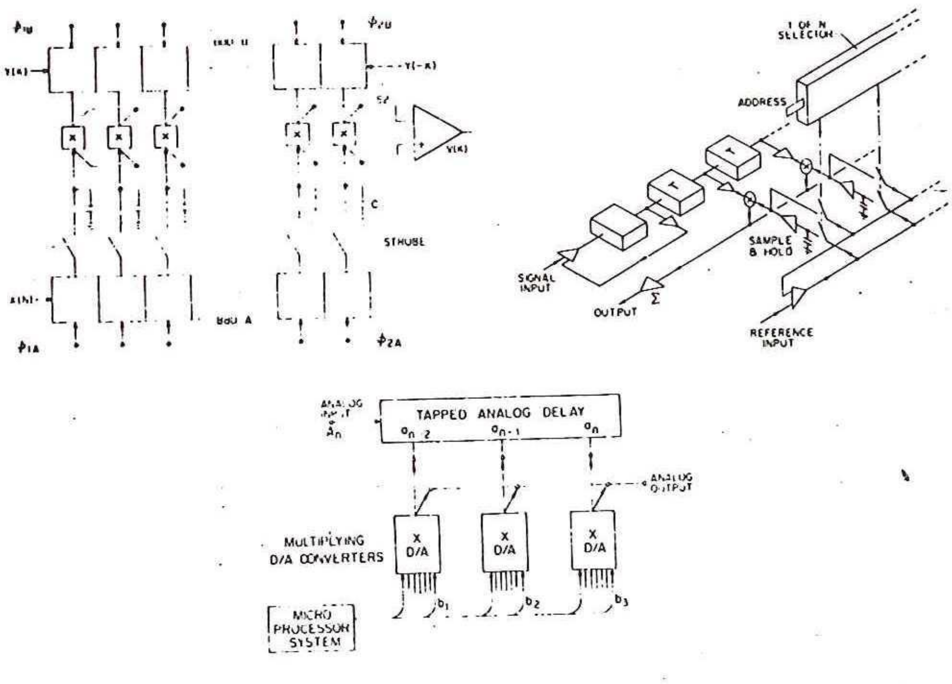


FIG. 7 Three Architectures For Realization Of Programmable Transversal Filters

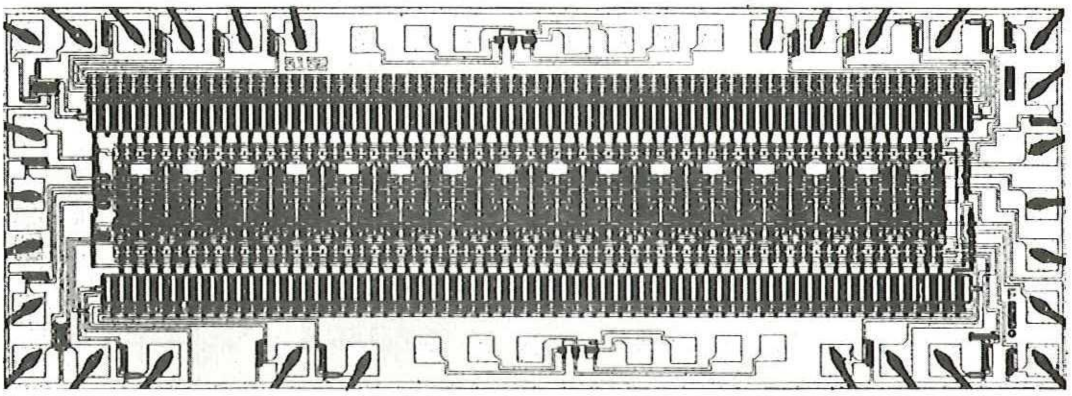


FIG. 8 A 32-Stage Analog-Analog Convolver (AAC)

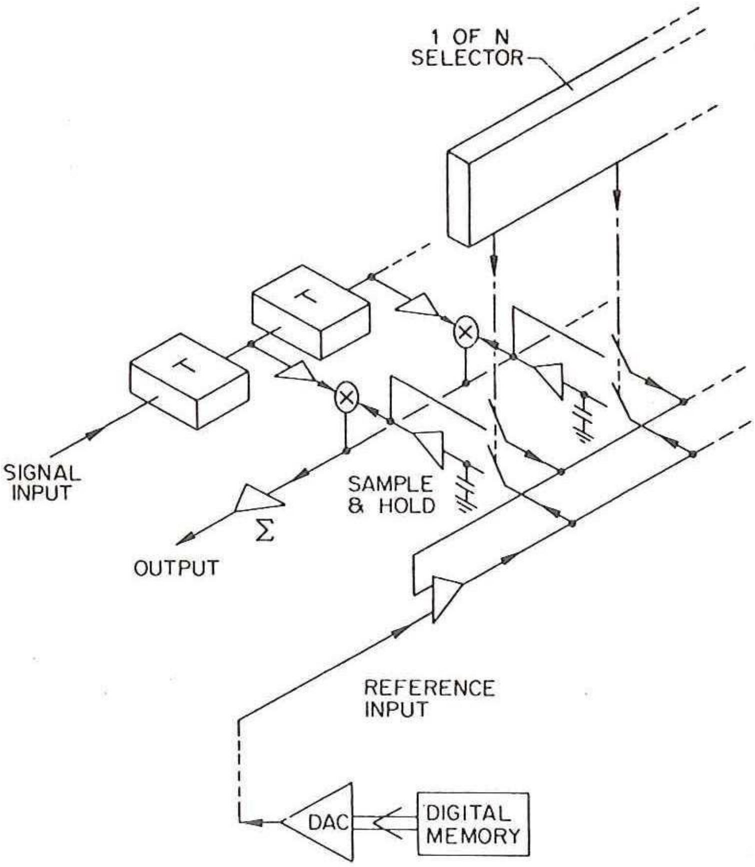


FIG. 9 Block Diagram Of A Programmable Filter Developed At The University of Edinburgh

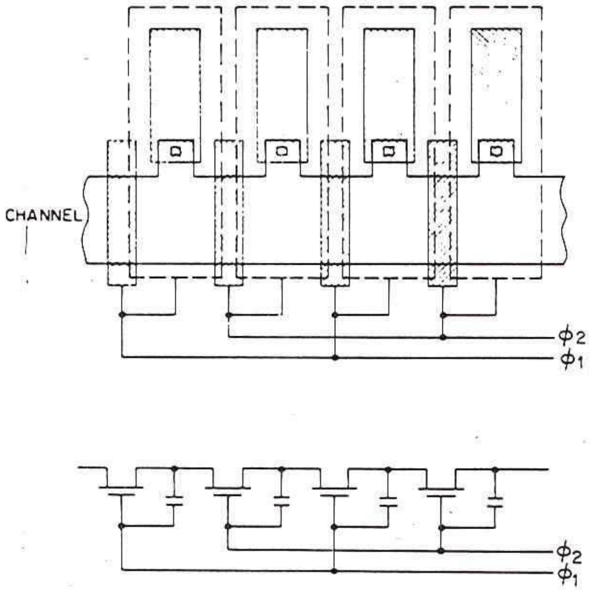


FIG. 10 Topographical Layout And Equivalent Circuit Diagram For A Very Low Frequency BBD.

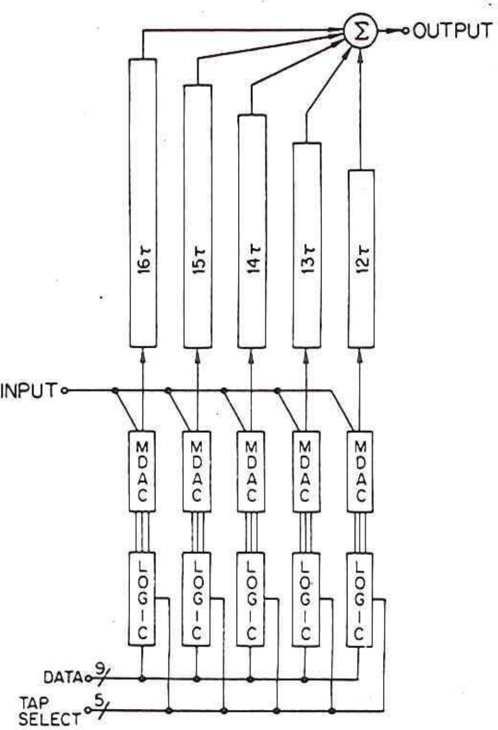


FIG. 11 Programmable Transversal Filter Made With Pipe Organ Delay Line And MDAC Multipliers

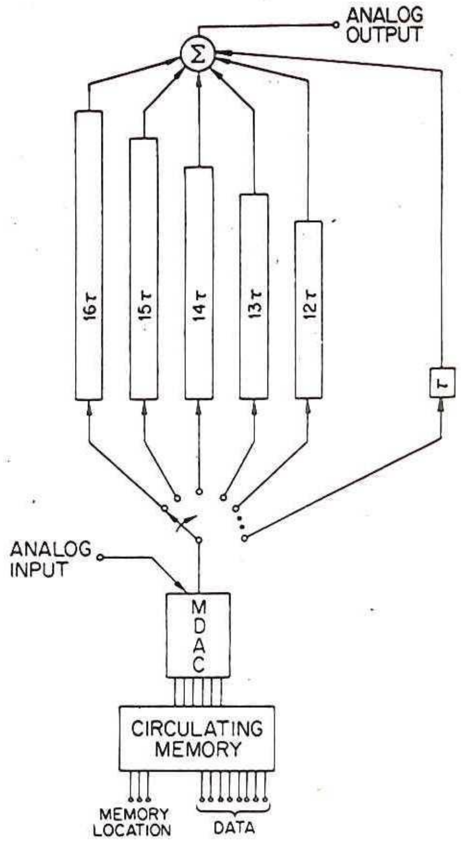


FIG. 12 Low Frequency Programmable Transversal Filter Utilizing A Single Multiplexed MDAC

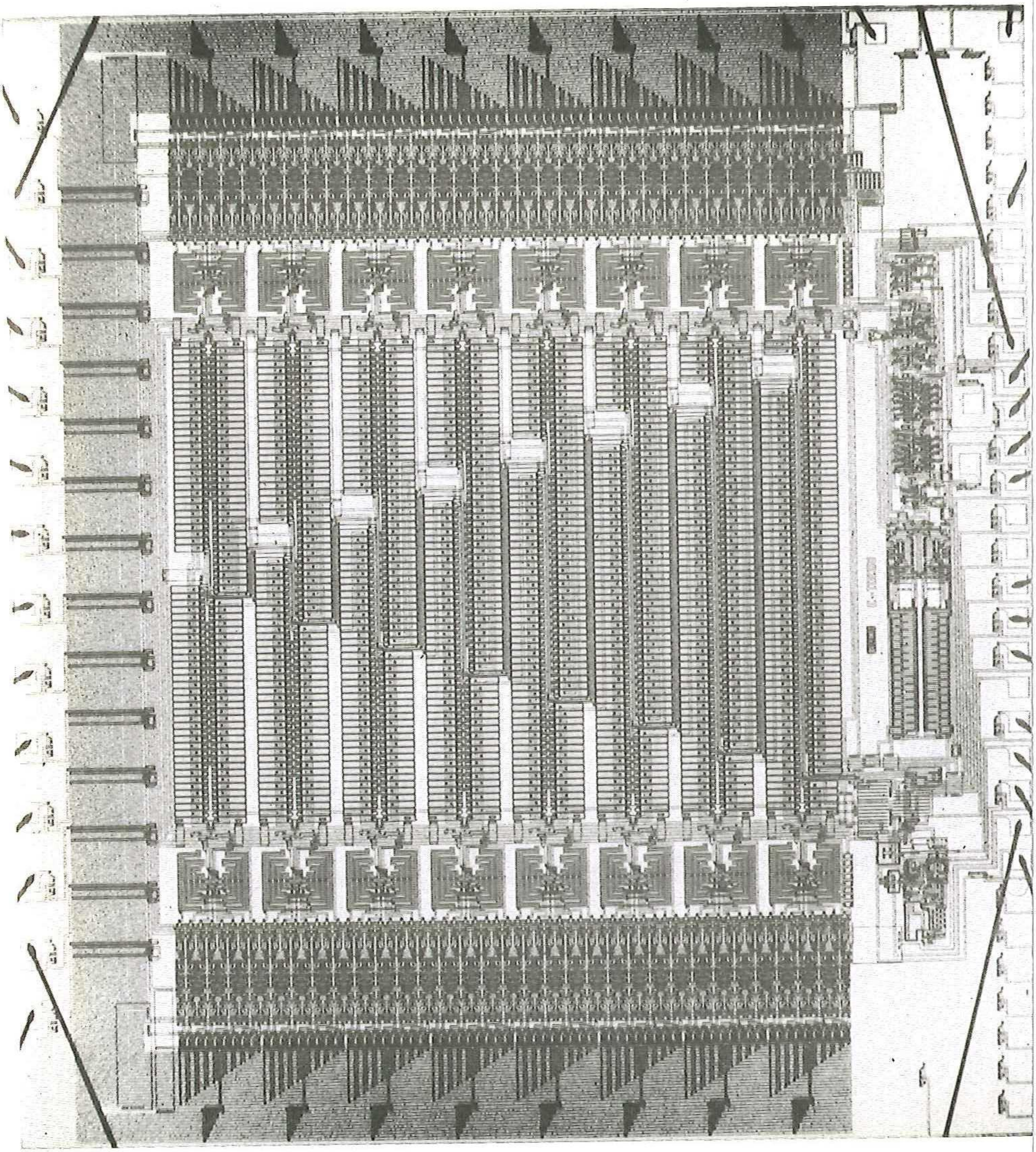
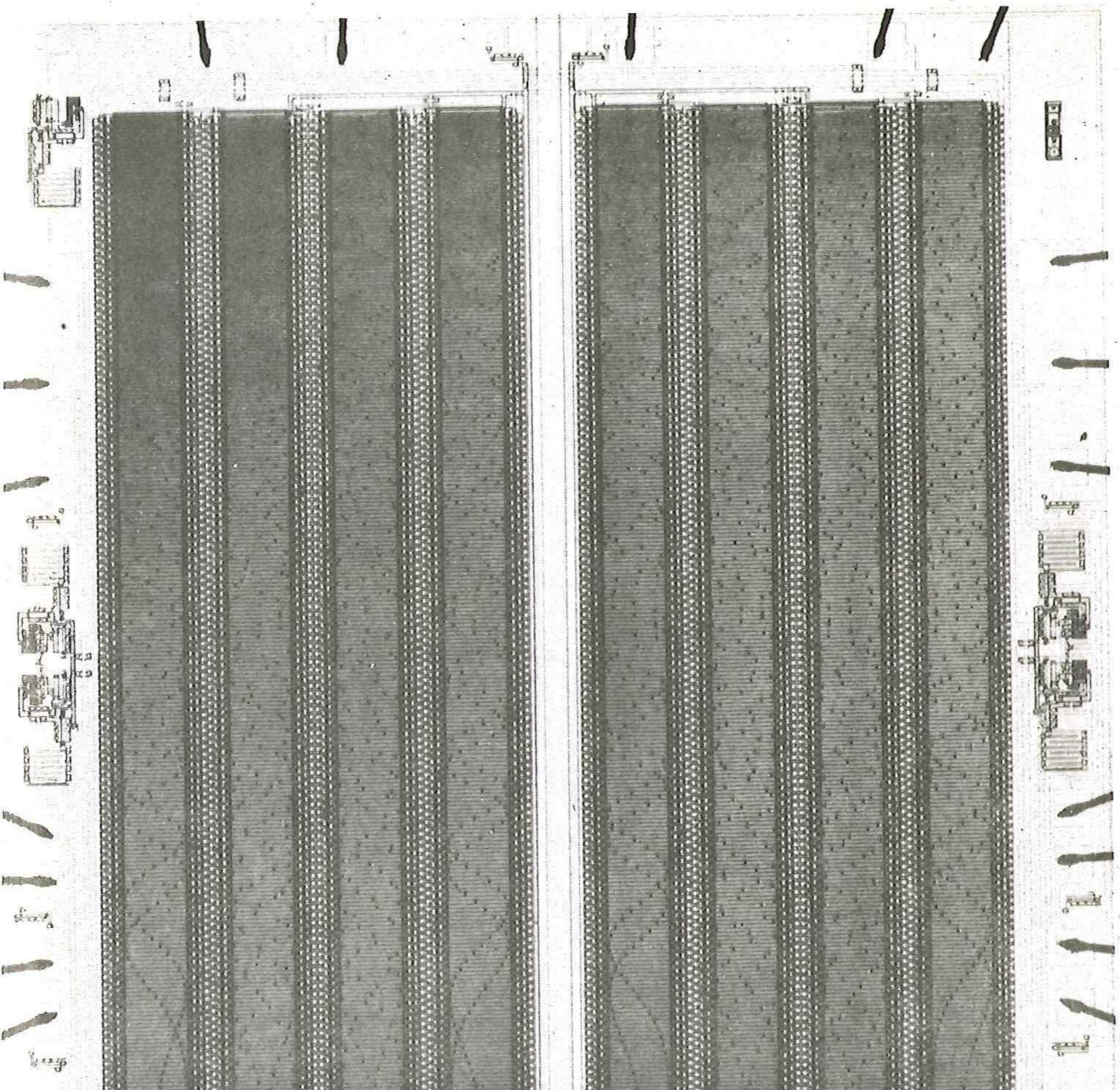


FIG. 13 Programmable Transversal Filter With 16 MDACs Configurable In Three Modes



RETICON R5601 : A CCD Quad Chirped Transversal Filter which implements the Discrete Fourier Transform (DFT) by using the Chirp Z Transform (CZT) algorithm.