DEVELOPMENTS IN CCD MODELLING AND SIMULATION TECHNIQUES

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ABSTRACT

In order to provide an engineering basis for surface channel, charge-coupled device analogue filter design a study of a concise analytic solution has been carried out, which describes the transfer of charge in a floating-gate reset (FGR) tapped CCD. Thus predictions of the performance of the CCD tapped structure can be made as effectively as possible. After presenting an overview of models already derived, this paper discusses the derivations of two models developed in this work and compares the techniques employed with those of existing simulations.

INTRODUCTION

The feasibility of charge-coupled devices (1) for performing complex filtering functions has been widely reported. Such filters - usually in transversal form, having a finite impulse response (FIR) - exploit the unique sampled analogue signal handling capacities of CCD's. The analogue nature of the CCD and associated peripheral circuitry makes the approach sensitive to any bias variations, ambient changes, etc. in common with other analogue circuits. Clearly, a model is needed which provides an engineering basis for designing such filters; it must be both intrinsically simple, so that the analysis of complex filtering structures can be completed rapidly and hence cost effectively, and must be as accurate as required for a design tool by judicious study and choice of the major contributive factors to the charge transfer process in the CCD.

These criteria effectively eliminate the use of most numerical methods for evaluating device performance which have already been evolved in CCD theory and design. These are demanding in terms of computer storage, analysis time and running cost and more importantly are based on models which do not permit certain basic features of charge transfer under modified clocking schemes, e.g. using $(n + \frac{1}{2})$ phase clocking arrangements using floating-gate, reset[2] (FGR) CCD tapping of signal charge used in complex filters.

PROBLEM DEFINITION

In the design of any CCD structure the salient parameter which must be characterised is the intra-cell transfer inefficiency; which is affected by the physical dimensions of the device and also by the clock driving waveforms. Several models have been developed for determining the transfer inefficiency of CCD devices which tend to fall into two categories: in that they are either very simple but unable to predict the effects of

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changes in the physical parameters of the devices or that they are very accurate and sensitive to changes in the physical parameters. They are also computationally involved when used to model a complex CCD structure, especially with associated MOS peripheral circuitry. Furthermore, the models which have permitted closed-form expressions to be derived for charge distribution in the discharging well, and hence permit a time dependent expression for the transfer inefficiency to be derived, have assumed that the charge distribution of the 'lip' of the discharging well is zero which is the case only where stepped clock waveforms are employed. However, if for example, the clock waveforms have exponential decaying edges, then firstly, the boundary condition for the charge distribution on the edge of the discharging well cannot, in general, be assumed to be zero; and secondly, since the driving potential on the discharging well is continually changing, the steady-state conditions, which in the case of the stepped clock waveforms permitted a closed-form solution for charge distribution to be obtained, are not applicable.

In an FGR tapped, two-phase CCD - which is of particular interest to our studies - there are typically multiple transfer stages with the following three basic types of charge transfer between the pairs of adjacent gates (see Fig. 1): (a) untapped to untapped, (b) untapped to tapped, and (c) tapped to untapped. Thus, the problem divides naturally into a fairly detailed analysis of charge transfer from cell to cell, which can then be used as unit models in a second "black box" model to produce a design tool for a complete device. Hence the problem resolves itself into finding a fast, reasonably accurate solution for charge transfer over an FGR tapped cell.

REVIEW OF CCD MODELS

With the invention of the charge-coupled device, an inevitable quest was initiated for a computer model which would permit the theoretical performance of the device to be predicted for changes in either the physical or electrical parameters of the device. Following from the methods suggested by Amelio (3) the problem of charge transfer between gates in a surface channel CCD have usually been tackled with reference to the electrostatic analysis of the MOS transistor.

Starting with the depletion approximation the familiar system of Poisson's equation and the continuity equations is formulated, including the following:

(a) Thermal diffusion;

(b) An electric field component that gives rise to self-induced drift (4) and fringing field effects (5); and

(c) Surface states and trapping effects (6).

Other factors usually debated include recombination and mobility effects and the choice of boundary conditions which can determine the type of voltage pulse analysed (7). Owing to the analogy with Heat Diffusion various numerical methods are readily employed to solve the basic equations. Often the field potential is solved for in two dimensions directly. Recent work in this field illustrates both the completeness of the solution and its limitations (8,9), in that excess computational time in practice determines analysis of only one transfer, usually at the input and output stages.

Other models of surface channel charge transfer fall into the following types:-

(a) Charge Control (10);

(b) Lumped Model (11);

(c) Circuit Equivalent (12);

(d) Distributed Model (13);

(e) A "statistical or particle" model.

Similar limitations to those mentioned above are observed in these methods e.g. an analysis applied mainly to injection of charge; transfer inefficiency obtained for square wave clocking mechanisms.

For the study of charge transfer in a tapped CCD a slightly different approach is required, and as a natural division occurs between the analysis of gate-to-gate charge transfer and that of the overall device transfer inefficiency, it was decided in this work to mirror this macro/micro split in the FGR model.

A ONE-DIMENSIONAL MODEL FOR CHARGE TRANSFER

The first approach which is described in this paper used a hierarchical model which permits sensitivities to changes in the physical parameters of the device structures to be examined whilst producing a model which can be used efficiently when predicting the performance of a complex CCD component configurations. In order to derive an expression for the transfer of charge between devices driven by exponential clock waveforms, a "snap-shot" technique has been developed, which, in effect, converts the continuous process of charge transfer with clock edges having an exponential decay to a form which considers that the clock waveform comprises a series of incremental voltage steps.

Assuming initially that the transfer mechanism is dominated by diffusion and fringing field effects, then during each interval of time the charge transfer can be described by

$$q/\partial t = D\,\partial^2 q/\partial x^2 - Ef\,\partial q/\partial x \qquad \ldots(1)$$

The solution to this equation for the boundary conditions existing in the CCD structure is of the form:

$$q(x,t) = \bar{q} + \sum_{n=1}^{K} An \left(\cos \frac{nmx}{L_1+L_2} - \frac{L_1+L_2}{n\pi} \sin \frac{n\pi x}{L_1+L_2}\right) e^{nx}\, e^{-Bt} \qquad \ldots(2)$$

where $n=\mu E/2D$ $\quad B=-D\left[n^2 + \dfrac{n^2\pi^2}{(L_1+L_2)^2}\right]$

and L_1 = length of discharging well;

L_2 = length of charging well, and $\bar{q}$ and An are given by:

$$q = \int_0^{L_1+L_2} q(x,t')\, e^{-nm}\, dx \Big/ \int_0^{L_1+L_2} e^{-nx}\, dx$$

$$An = \frac{\int_0^{L_1+L_2} (q(x,t') - q)e^{-\mu x} \left(\cos \frac{n\pi x}{L_1+L_2} - \frac{\mu[L_1+L_2]}{n} \sin \frac{n\pi x}{L_1+L_2}\right) dx}{\int_0^{L_1+L_2} \left(\cos \frac{m\pi x}{L_1+L_2} - \frac{L_1+L_2}{n} \sin \frac{n\pi x}{L_1+L_2}\right)^2 dx}$$

At each time step the charge distribution at the end of each time interval has to be computed, and subsequently, this distribution is used at the initial condition at the start of the next time step. A new value of fringing field has also to be computed at each time step in view of the change in potential difference between each potential well and also because of the change in the depletion region depth in the discharging well. This procedure is repeated until the charge transfer process is over. By calculating the amount of charge left over after each time step an expression for the charge transfer inefficiency as a function of time can be derived.

Having derived a value for the transfer inefficiency the CCD can now be represented by a simple systems models with the "bit-group" then represented by the systems model shown in Fig. 3, in which each block can have a different transfer inefficiency value, ϵ. The transfer function across the "bit-group" can then be described as:

$$T = \frac{p'p''p'''e^{-3j\omega T_c}}{(1 - \epsilon' e^{-j\omega t_c})(1 - \epsilon'' e^{-j\omega t_c})(1 - \epsilon''' e^{-j\omega t_c})} \qquad \ldots(3)$$

where p', p" and p"' are the transfer efficiency parameters for each device and ϵ', ϵ'' and ϵ''' are the corresponding values of transfer inefficiency. The inclusion of tapping points can also be readily modelled permitting complex filtering functions to be readily analysed.

PERTURBATION MODEL

After further examination of the charge transfer process in a CCD, another mathematical model has been developed which will be referred to here as the 'perturbation solution'. The model adopted for the charge density, q(x,t) across a pair of adjacent gates of width $\alpha\ell$ and $(1-\alpha)\ell$ is the non-linear, non-autonomous diffusion equation:

$$\frac{\partial q}{\partial t} = \frac{\partial}{\partial x} (R\ (q,t)\ \frac{\partial q}{\partial x} \qquad 0 \leq x \leq \ell \qquad \ldots(4)$$

where, $R(q,t)\ D - \frac{\mu}{C_{ox}} q\ [1+\{= - \frac{2C_o}{B} (V(t) + \frac{q}{C_o})\}^{-\frac{1}{2}}]$

$$= D - \frac{\mu}{C_{ox}} F(q,t)$$

and $\frac{\partial q}{\partial x} = 0$ at $x = 0$ and $x = \ell$ for all $t \geqslant 0$.

Initially, $q(x,0) = N/\alpha\ell$ $\quad 0 \leqslant x \leqslant \alpha\ell$

$= 0$ $\quad \ell \leqslant \quad \leqslant \ell$

A solution for this equation has been sought in the form of a perturbation series which when incorporated into the above differential equation yields a chain of linear, partial differential equations which can be solved analytically. The solution relies on a perturbation series of the form:

$$q(x,t) = q_0(x,t) + \epsilon q_1(x,t) + \epsilon^2 q_2(x,t) + \ldots\ldots\ldots$$

While it is possible in theory to find an analytical expression for $q_2(x,t)$, it may suffice simply to obtain an estimate for its size, thereby providing a measure for the reliability of the two-term series approximation.

SUMMARY AND CONCLUSIONS

A model with engineering emphasis for design of a CCD FGR tapped filter has been developed from an analytical approach. This attempts to retain the accuracy of proven finite-difference and close-form methods with a gain in speed of computation over existent work and also to include exponentially decaying clock waveforms, and the unique tapped gate feature of such devices. These models seem promising and their accuracy is currently under detailed evaluation.

ACKNOWLEDGEMENT

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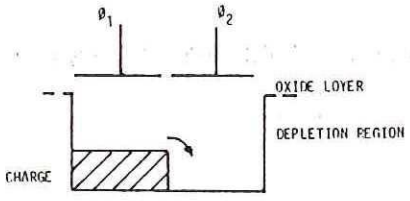
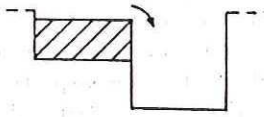
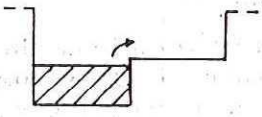


(a) Untapped to Untapped Well Charge Transfer



(b) Tapped to Untapped Well Charge Transfer



(c) Untapped to Tapped Well Charge Transfer

FIGURE 1 CHARGE TRANSFER SITUATIONS IN COMPONENTS WITH FGR TAP STRUCTURES.

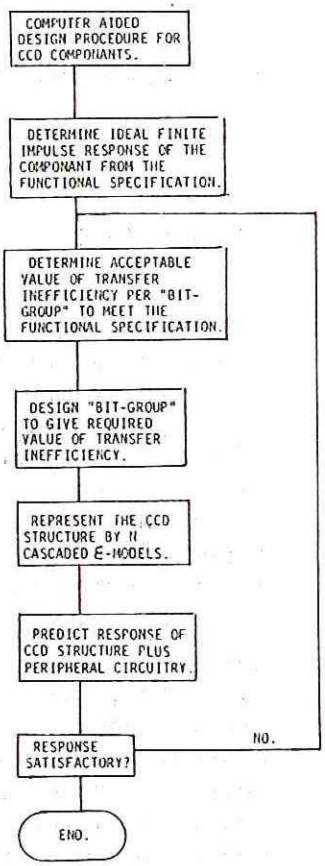
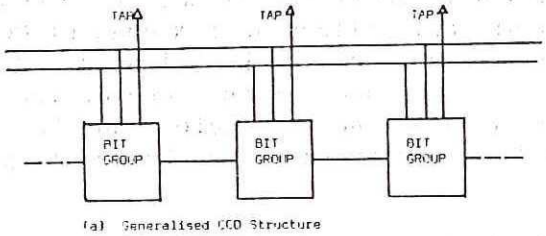
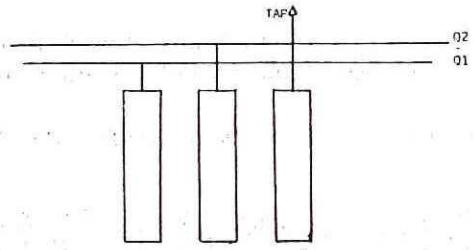


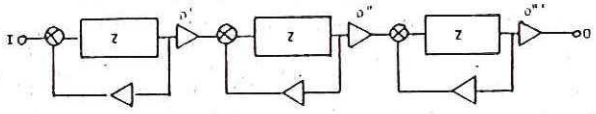
FIGURE 2 COMPUTER AIDED TOP-DOWN DESIGN PROCEDURE FOR CCD COMPONENTS.



(a) Generalised CCD Structure

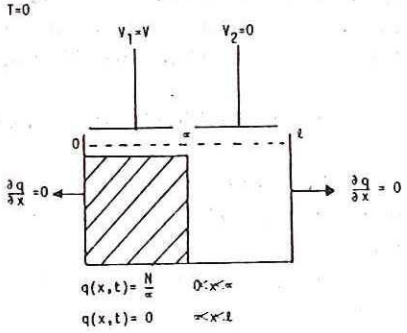


(b) Bit Group



(c) Systems Model for Bit Group

FIGURE 3 BIT GROUP MODEL.



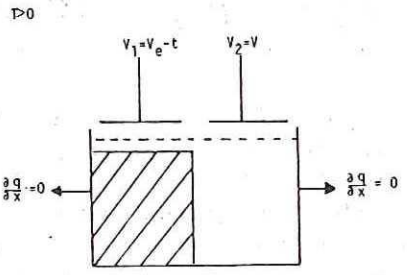


FIGURE 4 PERTURBATION MODEL.