COMPUTER SIMULATION OF CHARGE-COUPLED DEVICES

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ABSTRACT

A computer program employing finite-element techniques has been developed to simulate CCD's in two space dimensions and time. It has been used to study a typical CCD input structure and in particular to calculate the voltage to charge transfer function for "diode cut-off" and "fill and spill" input techniques. The non-linearity of the transfer functions has been used to estimate the distortion versus speed trade-offs for the two input techniques.

INTRODUCTION

The computer package we have used to calculate dynamic properties of CCD uses a finite element format. The motion of both holes and electrons are treated separately in the continuity equation and each have their own field dependent mobility function. The particular problem considered here involves the flow of charge into and out of the input diode diffusion. Simulation difficulties arise owing to the extremely short dielectric relaxation time in this heavily doped region. These have been overcome with a semi-metallic boundary condition which has been shown to be a good approximation.

THE PROGRAM

The charge densities and the potential that exist on a grid of nodal points have been calculated using finite-element techniques. The points are formed at the intersections of two sets of parallel lines, one set being parallel and the other perpendicular to the oxide-semiconductor interface. An arbitrary spacing of the lines is used and is of great importance to surface channel CCD modelling in which minority carrier motion is largely confined to a very thin region at the oxide-semiconductor interface.

Initially, the charge movement due to the potential between adjacent grid-points is calculated and the resulting nodal densities of electrons and holes are then used in the calculation of the nodal potentials. In the latter potential solution, Poisson's equation in two dimensions is reduced to a discrete form using finite elements, and the coefficient matrix so obtained is inverted at the start of the program execution. The potentials at the grid points may then be obtained from the product of this inverted matrix and the vector of nodel charges. The stability of the charge movement process is aided by using Gummel's algorithm[1] in which the current density and the electric field between grid points are assumed to be constant within each time step. This approach avoids implied current discontinuities in between grid points and associated non-physical instabilities.

A problem occurred at the input diode where high doping densities would require a prohibitively small time-step for numerical stability.

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This was overcome by using a constant voltage, or semi-metallic boundary condition. Any holes entering this region were annihilated. The approximation was checked by varying the donor doping density around this boundary to show that it had an insignificant effect on the results.

INPUT TECHNIQUE SIMULATION

The input structure, Fig.1, considered consists of an input diode, an input gate and a second electrode (ϕ_1) under which it was desired to isolate a charge packet. A third electrode running along the bottom of the device is used to supply a constant substrate bias of -3Volts which models a typical flatband voltage for a Si MOS device. Maximum and minimum electrode voltages are 15 and 0 Volts respectively. The two different input techniques will now be discussed in turn.

a) Diode Cut-off

The signal voltage is applied to the input diode and initially a high voltage (15 Volts) is applied to the gate and ϕ_1. Charge flows into the region under the two electrodes until the surface potential under them equilibriates with that of the input diode; when this occurs the 'injection phase' of the process is complete. There then follows the cut-off phase in which the gate voltage is reduced to zero volts, thus isolating a charge packet under ϕ_1.

b) Fill and Spill

The signal voltage is applied to the gate and initially a low voltage (0 Volts) exists on the input diode and a high voltage (15V) exists on ϕ_1. As in the injection phase for diode cut-off, in the fill phase the surface potential under the two gates reaches equilibrium with that of the input diode. In the spill phase the input diode is pulsed to a high voltage allowing the excess charge under ϕ_1 and the input gate to drain into it until the charge under ϕ_1 is isolated from the input diode.

The inject and fill phases were completed to better than 1 part in 10^5 accuracy and the changes in electrode potential took place in 1.125, 5.625 16.875 or 33.75 nanoseconds for diode cut-off. For fill and spill the corresponding change took place in 1.125ns, all changes having a raised cosine profile. The spill phase was terminated after 34ns.

Figs.2 and 3 show the variation of surface potential for a 7.5 Volt signal during a cut-off and a spill phase lasting 1.125ns and 34ns respectively. Fig.2 shows the cut-off process to be far from ideal as some of the charge under the gate clearly finds its way under the ϕ_1 electrode. Fill and spill does not suffer from this drawback but the spill process is still not complete even after 34ns whereas cut-off finishes rapidly after the electrode voltage ceases to change.

RESULTS

Runs for the various times mentioned above were made with signal voltages of 1, 3, 4.5, 6, 7.5, 9, 10.5, 12 and 13.5 Volts and the value of charge under ϕ_1 was recorded at 3, 6, 17 and 34ns (corresponding to fall-time of 1.125, 5.625, 16.875 and 33.75ns for diode cut-off). The transfer functions for both methods are shown in Figs.4 and 5. Neglecting contribution by fourth order or higher harmonics a least square fit of a cubic polynomial was made to each of the 8 sets (4 for each method) of points so obtained. By fitting the cubic to subsets of points within each main set the effect of changing bias and/or amplitude could be shown. The expected trend of lower distortion products for low peak-peak amplitudes could be

clearly seen. However care has to be taken to avoid spurious results when fitting the cubic to few points for small amplitudes. Figs.6 to 9 show the distortion products of two techniques for the four times considered. These show fill and spill to be generally superior. At the shortest times for second order distortion diode cut-off is superior.

This result is similar to many experimental observations but quantitative differences exist . We have not included the effects of signal change during the charge spill. Using a simple quasi-static model similar to that of Sequin and Mohsen[2] we calculate distortion effects shown by the solid lines in Figs.6 to 9. Ignoring any possible cancellation the distortion intercept is given by the smaller of the two values. Distortion due to the dynamics of the charge flow dominates at short acquisition times while effects due to the dynamic signal take over as the time increases.

Experimental work suggests that capacitive feed-through may also adversely affect the input linearity. The input process is not completed until charge has started to move along the device as the surface potential under ϕ_1 rises; before this can happen ϕ_2 must be clocked 'on'. ϕ_2 is therefore clocked during the input window and any voltage spike appearing on the input diode or input gate will cause charge movement. For example a transient rise in input gate voltage during the spill phase of fill-and-spill will momentarily increase the conductance of the channel beneath the input gate, leading to more spill than would otherwise be expected. This results in further distortion, with fill-and-spill suffering more than diode cut-off.

CONCLUSIONS

This study of input linearity has yielded superficial trends but further analysis is required including the effects mentioned in the previous section. Furthermore the effects of a finite sampling window in limiting the inject and fill phases needs to be taken into account even though we expect this process to be much faster than the residual charge transfer effects at the end of the signal acquisition.

ACKNOWLEDGEMENTS

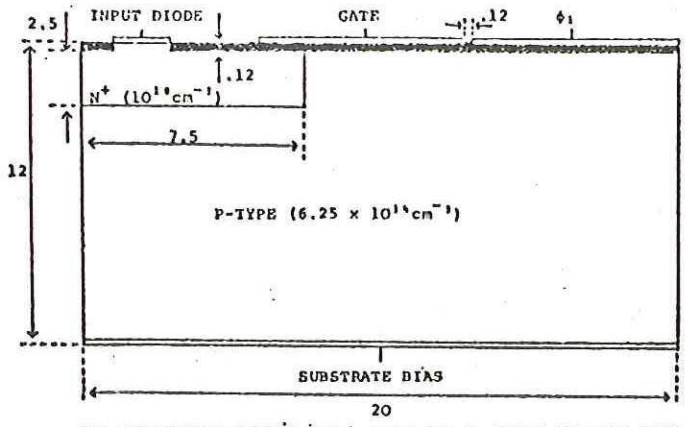
The authors are indebted to Mr. P. Darby for measurements of distortion. This work has been carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD.

REFERENCES

1. Scharfetter, D.L. and Gummel, H.K., "Large-signal analysis of a silicon Read Diode Oscillator", IEEE Trans. on Electron Devices, ED-16, pp.64-77, January 1969.

2. Sequin, C.H. and Mohsen, A.M., "Linearity of electrical charge injection into charge coupled devices", IEE Journal of Solid State Circuits, SC-10, pp.81-92, April 1975.

FIG.1 DIAGRAM OF INPUT STRUCTURE



ALL DIMENSIONS IN MICRONS. GATE AND ϕ_1 ARE 7 MICRONS LONG

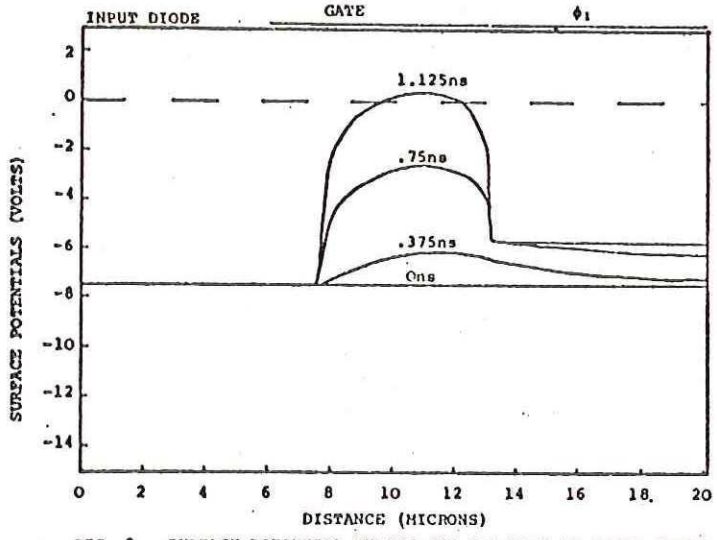


FIG. 2. SURFACE POTENTIAL DURING CUT-OFF WITH AN INPUT DIODE POTENTIAL OF 7.5 VOLTS

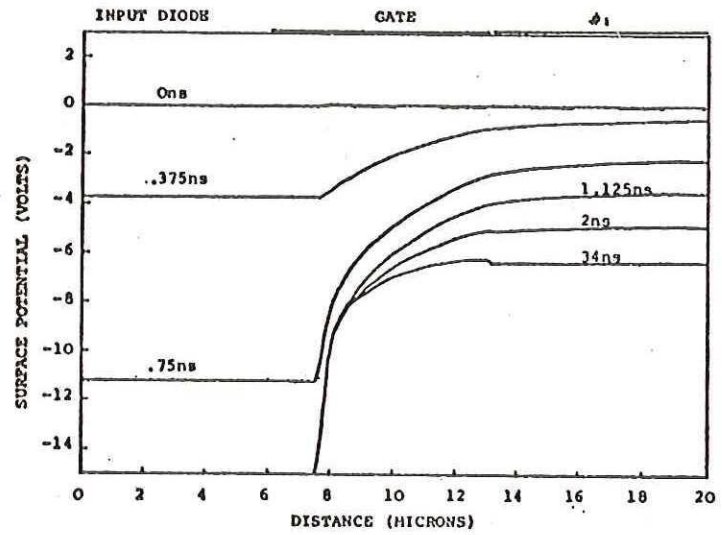


FIG.3. SURFACE POTENTIAL DURING SPILLING WITH A GATE POTENTIAL OF 7.5 VOLTS

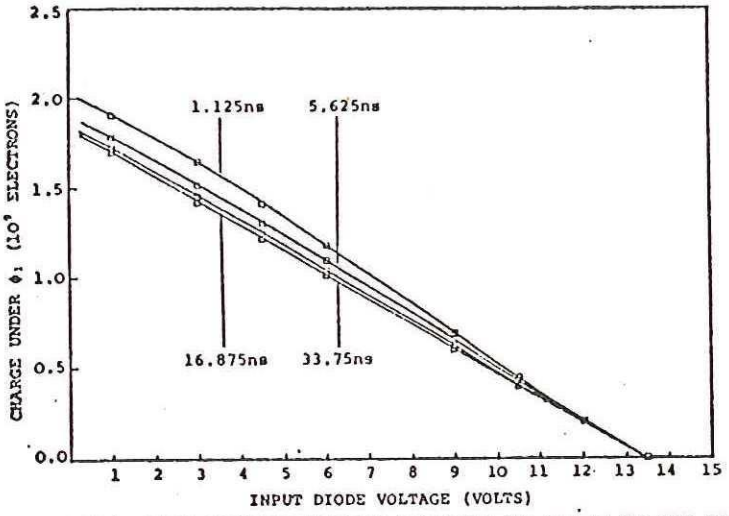


FIG.4 INPUT TRANSFER FUNCTION FOR DIODE CUT-OFF AT VARIOUS SPEEDS

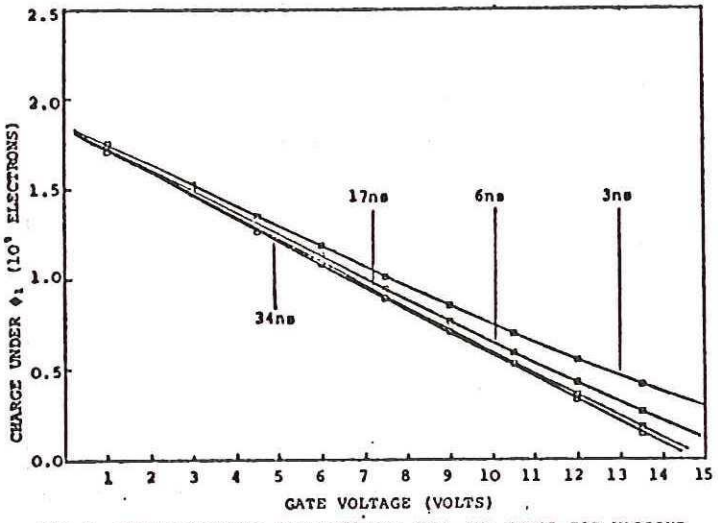


FIG.5 INPUT TRANSFER FUNCTION FOR FILL AND SPILL FOR VARIOUS SPILL TIMES

FIG.6 2ND HARMONIC DISTORTION PERFORMANCE FOR MAXIMUM SIGNAL LEVEL CONSIDERED (-1.6dB) AND CENTRAL BIAS

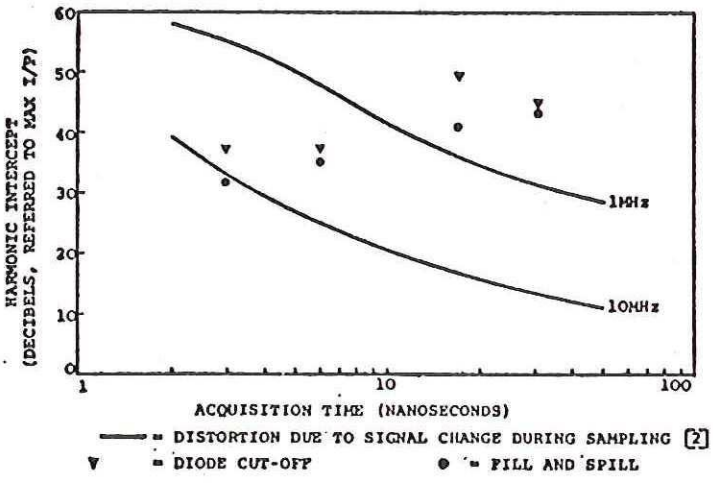
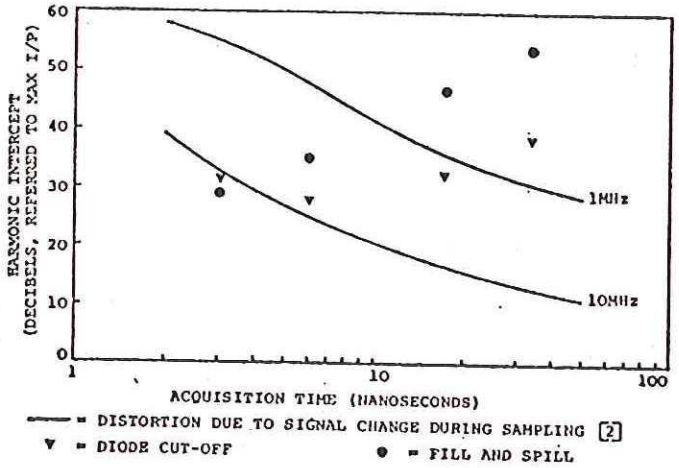
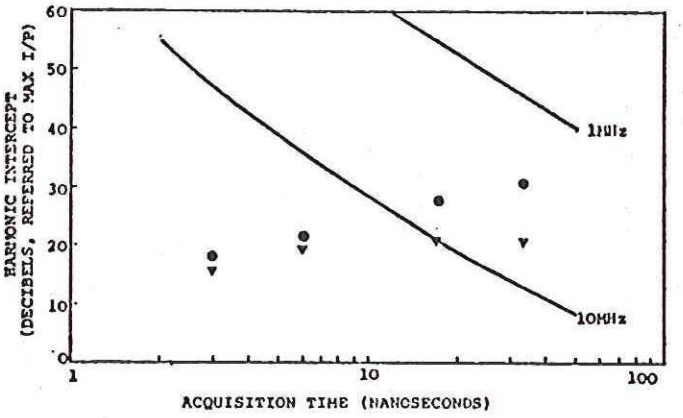


FIG.7 2ND HARMONIC DISTORTION PERFORMANCE FOR REDUCED (-8dB) SIGNAL LEVEL AND CENTRAL BIAS



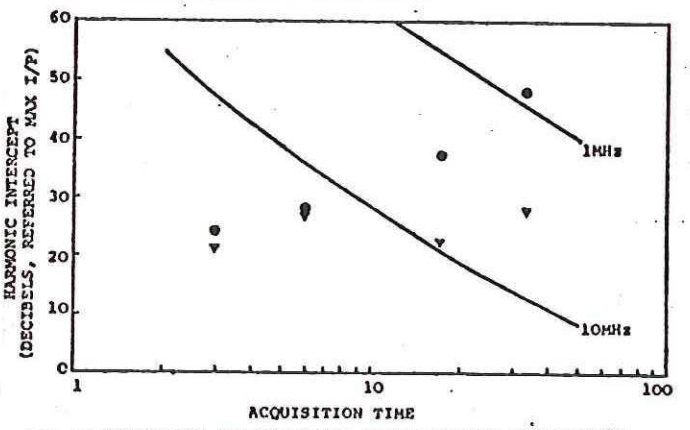
— = DISTORTION DUE TO SIGNAL CHANGE DURING SAMPLING [2]
▼ = DIODE CUT-OFF ● = FILL AND SPILL

FIG.8 3RD HARMONIC DISTORTION PERFORMANCE FOR MAXIMUM SIGNAL LEVEL CONSIDERED (-1.6dB) AND CENTRAL BIAS



— = DISTORTION DUE TO SIGNAL CHANGE DURING SAMPLING [2]
▼ = DIODE CUT-OFF ● = FILL AND SPILL

FIG.9 3RD HARMONIC DISTORTION PERFORMANCE FOR REDUCED (-8dB) SIGNAL LEVEL AND CENTRAL BIAS



— = DISTORTION DUE TO SIGNAL CHANGE DURING SAMPLING [2]
▼ = DIODE CUT-OFF ● = FILL AND SPILL