INVESTIGATIONS ABOUT THE EDGE EFFECT IN SCCDS

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ABSTRACT

To investigate the perpendicular and the parallel edge effects we have measured the transfer inefficiency for various channel widths, electrode lengths and clock frequencies. Since for channel widths W > 50 µm the perpendicular edge effect is the dominant loss mechanism we have developed a model to compute the losses caused by the interface states at the perpendicular edges. The comparison between measured and computed values indicates that the surface state density under a transfer electrode is higher at the edges than in the central region.

INTRODUCTION

For clock frequencies below the cutoff frequency the transfer losses in a SCCD are caused by filling and emptying of traps in the forbidden band. Operating the SCCD with a bias charge (fat zero) the fast interface states (FIS) in the different regions under a transfer electrode were filled and emptied in distinct manners. Previous papers have shown that only the FIS at the edge regions (Fig. 1) underneath the transfer electrodes contribute to the total transfer losses /1/.

In this work we present new results about the different influences of the edges parallel to the direction of charge transfer and those perpendicular to the channel on the total transfer inefficiency.

MEASUREMENTS

To investigate the influences of the parallel and the perpendicular edges we operated the SCCDs with a fat zero charge and measured the transfer inefficiency as a function of the channel width W (Fig. 2), the electrode length L (Fig. 3b) and the clock frequency f_c (Fig. 3a).

The SCCDs used in our measurements were 4-phase devices with overlapping electrodes fabricated with a two-level-poly-silicon-gate technology. The oxide thickness under poly-1-electrodes amounted to 800 Å and 1400 Å under poly-2-electrodes. The SCCDs consist of 40 elements. The devices were made on (100)-p-type substrates. At the input the fill and spill method was used for metering charge packets. To measure the transfer inefficiency we have periodically introduced a group of "ones", which was periodically followed by a constant number of "fat zeros". The rest voltages of the clocks $\emptyset_1$ to $\emptyset_4$ were adjusted to assure equal minimum surface potentials under the different gate oxides.

DISCUSSION

Parallel edge regions

During the time a fat zero is stored under a transfer electrode the charge spreads over the central region (Fig. 1). The transfer losses caused by the FIS in that region can be neglected /1/. If a "one" is

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stored under a transfer electrode the interface states at the parallel and the perpendicular edges were filled, since this charge covers a larger area. As the states at the parallel edges are never filled by the fat zeros the occupation probability of these traps is only governed by the temporal sequency of the "ones". This is similar to the situation in a SCCD operating without a bias charge. Using the analytic model given by Carnes and Kosonocky /2/ the fractional losses of the first "one" due to the parallel edge regions can be described as follows:

$$\varepsilon \sim \frac{A_{pa}}{A_{ele}} \cdot \frac{N_{SSpa}}{n_{SI}} = \frac{\Delta W}{W} \cdot \frac{N_{SSpa}}{n_{SI}} \quad \text{for } L = \text{constant} \tag{1}$$

A_{pa} area of the parallel edge region

$A_{ele} = L \cdot W$ area of a transfer electrode

N_{SSpa} surface state density in the parallel edge region

n_{SI} density of free electrons due to the "one" at the surface

The measured transfer inefficiencies ε as a function of channel width W confirm this dependency (Fig. 2) for $W < 50$ µm assuming a constant parallel edge region. But for $W > 50$ µm the measurements contradict this simple theory.

Perpendicular edge regions

To overcome this problem we have investigated the perpendicular edge effect in more detail. First a simple model was developed using the formulas for the "quasi-fermi-level" E_Q /2/ to compute the transfer losses caused by the FIS at the perpendicular edges. For simplicity we assume that all of the free electrons in a charge packet transfer instantaneously as soon as the clock voltages are switched and that the FIS can be filled immediately. The losses of a "one" preceded by a "fat zero" is then given by:

$$N_{LOSS} = A \cdot N_{SS} \left[E_{QFZ}(t_e = t_{FZ}) - E_{QI}(t_e = t_I) \right] \tag{2}$$

t_e time in which the released electrons can catch up with their original charge packets.

To solve Eq. 2 the time t_e, in which the released electrons can catch up with their original charge packet has to be known. In a four-phase system the available transfer time corresponds to one quarter of the clock period $T_C = 1/f_C$. Since the "one" fills the FIS at the perpendicular edge regions I and II at the same time, the time t_e for a "one-pulse" amounts to $t_e = 1/4 \cdot f_C$.

But for a "fat zero" the situation is quite different. If the background charge is transferred under an electrode, only FIS in region I (Fig. 1) will be filled. During the time the "fat zero" is stored the released electrons from region I can catch up with their original charge packet. If the "fat zero" is transferred again the FIS in region II will be filled. During the following storing time the emitted electrons from both regions (I and II) can join the "fat zero". Thus the time t_e amounts $1/2 \cdot t_C$ for region I and $1/4 \cdot t_C$ for region II. Inserting these results in Eq. 2 the transfer inefficiency ε_{perp} caused by the FIS at the perpendicular edges can be computed:

$$\varepsilon_{perp} = \frac{\Delta L}{L} \cdot \frac{N_{SSperp}}{n_{SI}} \cdot kT \cdot \ln 2 \quad \text{for } W = \text{const.} \tag{3}$$

$\Delta A = \Delta L \cdot W$ area of the perpendicular edge region

N_{SSperp} surface state density of the perpendicular edges

Computer simulations show that the width of the perpendicular edge regions is almost 1 µm and that ΔL is independent of the electrode length L. Since for W > 50 µm the measured total transfer inefficiency is almost inversely proportional to the electrode length L and independent of the clock frequency f_c as predicted by theory above, these losses are caused mainly by the FIS at the perpendicular edges.

Surface state density in the edge regions

Operating the SCCD without a fat zero charge the surface state density in the central region can be measured /3/. However using these values for N_{SS} in Eq. 3 the computed transfer inefficiency was about an order of magnitude lower than the measured ones. Therefore we believe that the surface state density at the edges of a transfer electrode is much higher than in the central region. At the perpendicular edges the higher interface state density can be attributed to the inhomogeneity at the Si-SiO_2 interface between the two gate oxides. A similar situation should exist at the LOCOS-edge. Assuming higher values for the interface state density at the perpendicular edges a good agreement between measured and computed values for $\varepsilon = f(f_c)$ can be achieved (Fig. 4).

CONCLUSIONS

For SCCDs with small channel widths the total transfer losses are caused mainly by the interface states at the parallel edges. But the losses due to the perpendicular edges dominate for longer channel widths (W > 50 µm), although the devices were built with well overlapping electrodes. We can show that the filling and emptying of interface states at the perpendicular edges results in a transfer inefficiency inversely proportional to the electrode length and independent of the clock frequency. Our investigations indicate that the surface state density N_{SS} is higher at the edges of a transfer electrode than in the central region.

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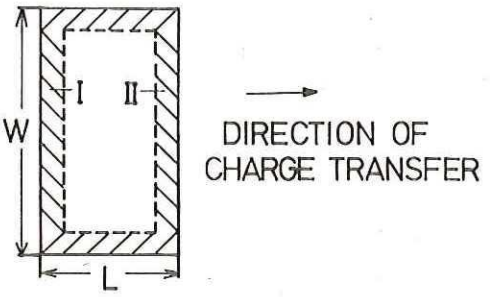

Fig.1 SCHEME OF THE AREAS COVERED UNDER A TRANSFER ELECTRODE BY A "ONE" AND A "FAT ZERO"

- Area covered by a "fat zero" (central region)
- Area covered by a "one"
- Parallel edge regions
- Perpendicular edge regions
- W channel width
- L electrode length

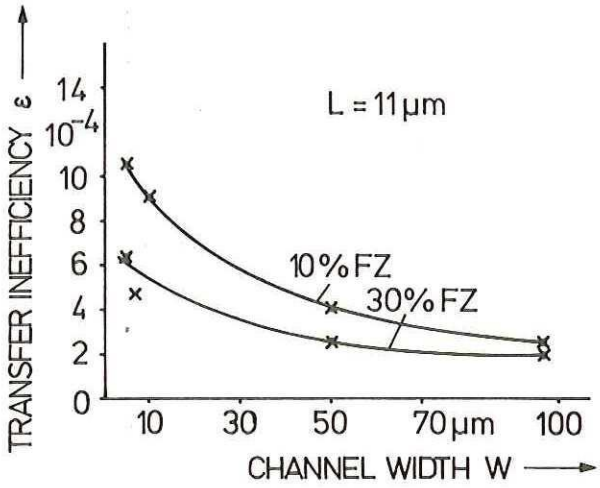

Fig. 2 MEASURED TRANSFER INEFFICIENCY VERSUS CHANNEL WIDTH FOR 10% AND 30% FAT ZERO

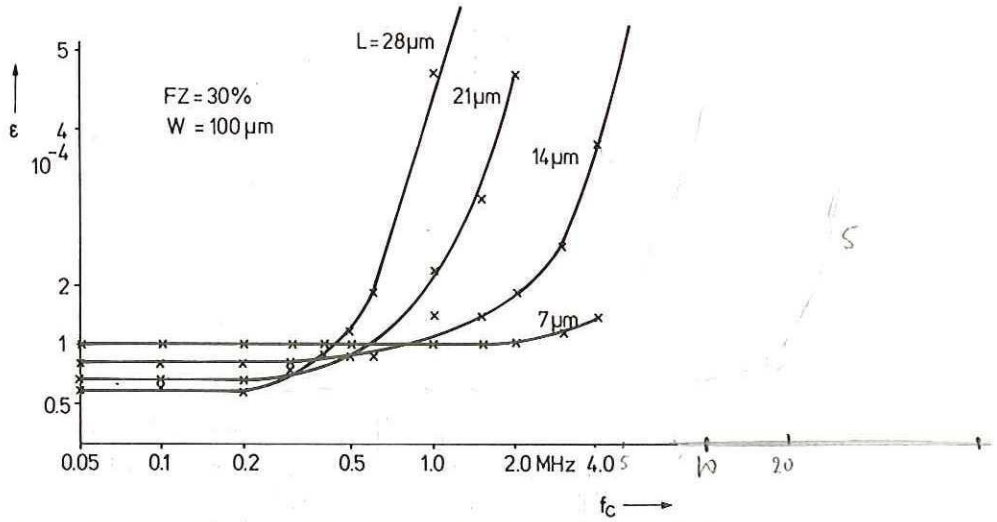

Fig.3a MEASURED TRANSFER INEFFICIENCY ε FOR DIFFERENT ELECTRODE LENGTHS VERSUS CLOCK FREQUENCY f_c

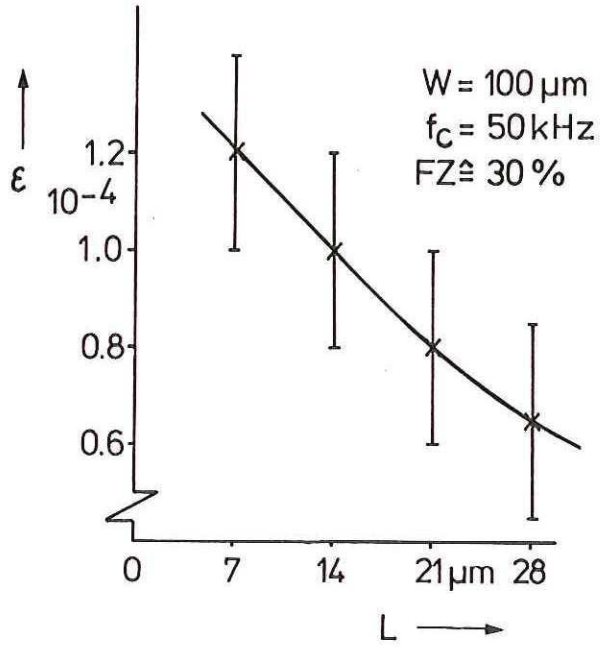

Fig. 3b MEASURED TRANSFER INEFFICIENCY ε VERSUS ELECTRODE LENGTH L

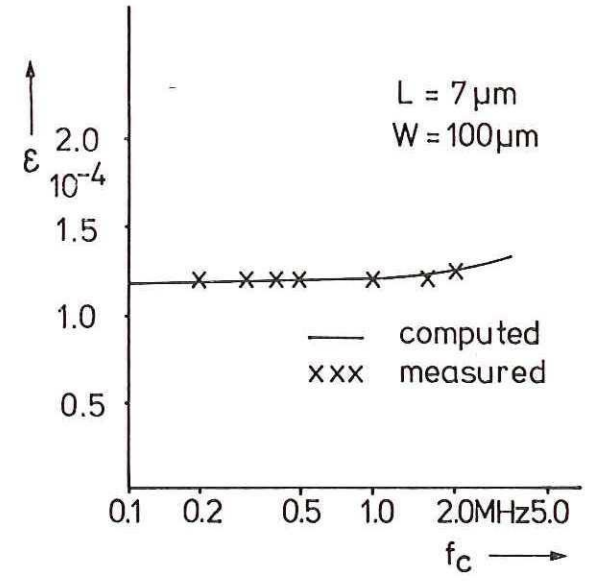

Fig. 4 COMPARISON OF COMPUTED AND MEASURED VALUES OF THE TRANSFER INEFFICIENCY ASSUMING:

$N_{SS\,per} = 4 \cdot 10^{10} cm^{-2} eV^{-1}$

$\sigma_n = 10^{-16} cm^2$