CHARGE COUPLED DEVICE CHARACTERISTICS IN THE PRESENCE OF BACKWARD FLOW.

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ABSTRACT

A model has been developed to give the transfer function of a three phase charge coupled device(CCD), taking into account the backflow of signal charge. From the transfer function obtained through the improved model, the CCD response in the frequency and time domain is analysed by simulating an N-bit CCD on ccmputer. It is concluded, from the analysis that the CCD response is not accurately characterised assuming an effective average inefficiency, particularly if the backflow is large. The presence of backflow has been demonstrated experimentally with a 3 bit 3 phase CCD using biased gate tap.

INTRODUCTION

In a CCD, packets of signal charge are shifted from stage to stage by transferring the charge between closely spaced potential wells, and unidirectionally moving the potential minima. In a 3-phased CCD, when the shifting of charge is done at a high frequency, that is the time duration for a well to collapse is less than that required for complete charge transfer to the following well, a significant portion of this charge flows back into the preceding stage[1]. In ref 1 the back flow was conceived as an effective inefficiency and no attempt was made to obtain the transfer function of CCD in presence of backflow.

In the present work, mathematical and circuit models have been derived based on the physical mechanism of backflow and an improved response of CCD has been obtained in the time and frequency domain.

An alternate approach is also considered in which, by suitable approximation, it is shown that backflow effectively adds to and increases the inefficiency. The response curve obtained through this is compared with that obtained from the above mentioned exact model.

MECHANISM OF BACKFLOW.

A part of signal charge packet can flow back under two conditions; (i) when the device is operated with short turn off time of the clock, leading to incomplete charge transfer, and if the resting potential of the clock is above the threshold voltage, then the leftover charge flows back as shown in Fig.1. (ii) when the device structure has interelectrode gaps potential well could be formed[2] thus trapping the signal charge and this trapped charge will flow back.

In the first case, if one follows the diagram of charge flow with time, it is seen that when charge flows from region below ϕ_3 of(I-1)th stage to that of Ith stage in three successive transfers, for two transfers there is backflow from Ith stage to (I-1)th stage and for one transfer the backflow is

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within the (I-1)th stage. In the second case only in one transfer backflow occurs from Ith to (I-1)th stage and in remaining two transfers, within the stage. In both, the backflow is proportional to the signal charge and there is interstage coupling for backflow in one clock period. This is to be taken into account in the modelling of the device. While the intrastage backflow will effectively modify the value of inefficiency of the given stage, the interstage backflow may be viewed as a feed back phenomenon.

Model for Backflow

We assume that 'β' times the original charge packet moves in the backward direction taking into account all the intermediate transfers. Also assume that there is no appreciable change in the signal packet size along the length of CCD to cause a change in β ,that is β is same in all the stages. Fig.2 gives a black box representation of charge transfer in presence of backflow. It is obvious from the argument given above that, when a given stage transfers charge to the following stage, the preceding stage also receives a fraction of this charge. Thus for complete description of the charge transfer process form a given intermediate Ith bit in the presence of backflow, both (I-1)th and (I+1)th stages are coupled. η_o and ε_o in fig.2 are the fractions of the charge that is transferred and that which is left untransferred respectively. $V_I(n)$ represents the charge in the Ith packet at the instant n. η_o and ε_o are characteristic of a stage(bit) and all the stages are considered to be identical. The mathematical expression for the charge in the Ith stage at the instant n can be written as

$$V_I(n)=(1-\beta)[\eta_o V_{I-1}(n-1)+\varepsilon_o V_I(n-1)]+\beta V_{I+1}(n) \quad (1)$$

Three methods of approach are dealt with to solve for the transfer function and their validities are discussed in the end.

(1) Exact analysis:- Rearranging the terms in equation(1) and taking z transforms on both sides, we get

$$V_{I-1} = V_I \frac{(z-\varepsilon)}{\eta} - \frac{\beta}{\eta} z V_{I+1} \quad (2)$$

where $\eta=(1-\beta)\eta_o$, $\varepsilon=(1-\beta)\varepsilon_o$

Starting from the output end of an N bit CCD and writing the equation for charge in the previous electrode, from (2)

$$V_N = V_N,$$

$$V_{N-1} = (z-\varepsilon)/\eta \; V_N + 0,$$

$$V_{N-2} = (z-\varepsilon)^2/\eta^2 \; V_N - \beta z/\eta \; V_N$$

similarly proceeding we can write V_o at the input end as

$$V_o = \sum_{n=0}^{N} C_N (1-\varepsilon z^{-1})^n z^{(N+n)/2} V_N \quad (3)$$

where $C_N=(-1)^{(N-n)/2}\binom{\frac{N+n}{2}}{n}\left[\frac{1+(-1)^{N-n}}{2}\right]\left\{\frac{\beta}{\eta^{(N+n)/2}}\right\}$

Inefficiencies included by the input and output ports are

considered less significant and so are neglected. From equations(3) we get the transfer function as

$$H(z)=1/\sum_{n=0}^{N-1} C_N(1-\varepsilon Z^{-1})^n z^{(N+n)/2}+\frac{1}{\eta^N}(1-\varepsilon z^{-1})^N z^N \qquad (4)$$

The above expression with $\beta=0$ reduces to $H(z)=z^{-N}\eta^N/(1-z^{-1})^N$ well established transfer function of a CCD without backflow.

Frequency and Time Domain Response

From equation(4), frequency response obtained using the relation $H(W)=H(Z)|_{Z=e^{JWT}}$ is computed and by using HP 9830 the magnitude response $|H(W)|$ with respect to W is plotted for different ε_o and β values (see Fig.3). Equation(4) can also be written in the form

$$H(z) = z^{-N}\eta^N \{1+K_1 z^{-1} + K_2 z^{-2}+\ldots K_N z^{-N}\}^{-1}.$$

where Ki's are given by the following expression for even no. of bits

$$K_i=(-1)^i \{\binom{N}{i}\varepsilon^i+\sum_{n=1}^{a} N-n!\ \varepsilon^{i-n}(\eta\beta)^n/(N-i-n)!\ i-n!\ n!\}; i=1\ldots N-1$$

$$K_N=(-1)^N \varepsilon^N$$

where

$$a=i \quad \text{for} \quad i=1,\ldots N/2$$
$$=N-i \quad \text{for} \quad i=N/2,\ldots N-1$$

$$H(z)=z^{-N}\eta^N\{1-K_1z^{-1}+(K_1^2-K_2)z^{-2}-\ldots\}$$

It is easy to obtain the impulse response h(n) of H(z) from the above expression.

(2) Circuit model approach:- The equivalent circuit for any intermediate state, from the transfer equation of a CCD with backflow is given in fig.2a. The expression obtained, from the circuit model approach, for the K_i's for a simple 3 bit CCD is in agreement with that obtained from exact analysis.

(3) Effective ε approach:- Eqn.(1) can be expanded as

$$V_I(n) = (1-\beta)(\eta_o V_{I-1}(n-1)+\varepsilon_o V_I(n-1))+$$
$$\beta\{(\eta_o V_I(n-1)+\varepsilon_o V_{I+1}(n-1))(1-\beta) + \beta V_{I+2}(n)\}$$

Neglecting second order term involving $\varepsilon\beta$ and β^2 we get

$$V_I(n) = \eta V_{I-1}(n-1)+(\varepsilon+\eta\beta)V_I(n-1) \qquad (6)$$

This shows that transfer inefficiency merely manifests into a new value $(\varepsilon+\eta\beta)$ because of backflow.

In Fig.3 curve 3 is obtained for a 16 bit CCD when effect of backflow is taken to be just increasing the overall transfer inefficiency as from effective ε approach. The values of ε_o and β are typically 10^{-3} and 10^{-2} respectively, and $\eta_o=(1-\varepsilon_o)$. Curve 2 for the same ε_o and β is obtained through the exact analysis and the magnitude response shows a definite deviation from the effective ε approach. Sets of curves1(a)

and 1(b) are plotted using exact analysis for two different sets of values for εo and β such that the quantity $N\varepsilon'=N(\varepsilon+\eta\beta)$ is of magnitude 10^{-1} and 4×10^{-1} respectively. The arrow indicates that there is an increase in β along with it from curve to curve. In the effective ε approach these sets of curves 1(a) and 1(b) will just be replaced by single curves corresponding to the given values of $N\varepsilon'$. From this it is apparent that presence of backflow does not merely manifests itself, into an addition in the transfer inefficiency but causes a definite change in the response and cannot be overlooked particularly for higher 'β' values, typically for 10^{-2} and above.

The impulse response coefficient h1 is given by $h1=k1=m\varepsilon+(m-1)\eta\beta$ from the general expression for Ki, in the exact analysis. Calculating from the approach(3), $h1=m(\varepsilon+\eta\beta)$ which shows a 10 p.c. increase in the value corresponding to the values of $\varepsilon o=10^{-3}$ and $\beta=2\times10^{-2}$ for a 16 bit CCD.

EXPERIMENTAL EVIDENCE

The charge flowing back from the collapsing well joins that in the preceding well, which is also collecting, at the same time, the forward flowing charge from its previous stage. If the charge back flow is to be sensed, the well that is collecting this backflow charge should be devoid of any other charge inflow. An experimental set up shown in Fig.4 realises the sensing of backflow.

A three bit three phase CCD is fabricated with facilities to sense the charge at any intermediate bit by making one of the phase electrodes(ϕ_2) of all the stages independently accessible, and using biased gate tapping[3]. Initially, a unit step or a train of pulses is injected in. At an instant corresponding to fig.4a under the gate 2 of second bit when this charge comes, a single pulse is given out. 4(b) illustrate this charge being emptied out into the next ϕ_3. In the next instant when ϕ_3 collapses and if the turn off time is very large there will not be any backflow, as shown by 4(c).4(d) is a particular case of 4(c)when turn off time is very small. It is evident that if, under the gate ϕ_1, the well is just filled by the forward transfer from bit 1, the backflow charge will be equally shared under ϕ_1 and gate 2 as shown. Backflow does not occur in bit 1 or 3 as the resting potential of the clock is below the threshold voltage.

Thus at this instant a relatively smaller pulse corresponding to this backflow charge is seen at the output.

Figure 5a and 5b show the output corresponding to the situation described in Fig 4(c) and 4(d) for the three bit CCD, whose output is being tapped from the second bit. The clock frequency is 100 KHZ, and the turnoff time is 10 µsec. and 1 µsec. respectively for 5a and 5b. Fig.5 c is the expanded version of 5 b and the delay of $1\frac{1}{3}$ bit is clearly seen.

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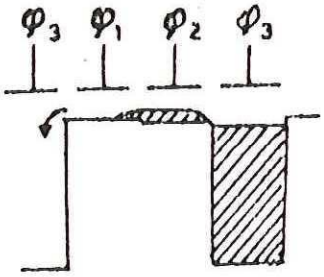

Fig.1 Backflow due to small turn-off time.

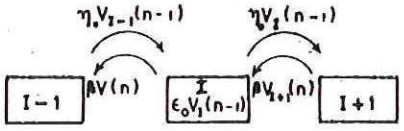

Fig.2 Black box representation of per stage backflow.

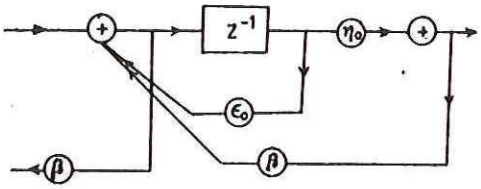

Fig.2 a Circuit model

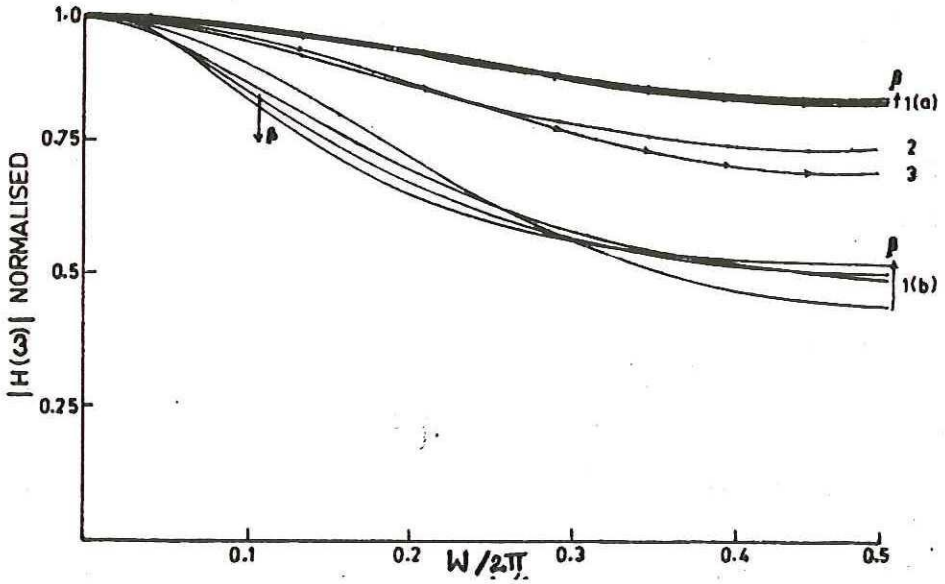

Fig. 3 Magnitude response of C.C.D with β

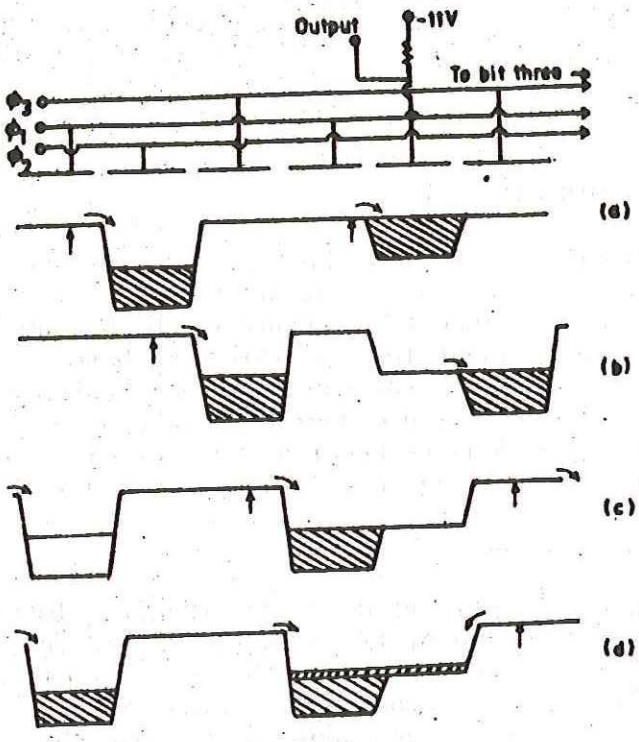

Fig.4 ϕ_1, ϕ_2, ϕ_3 clock excursion -5 to -15V.

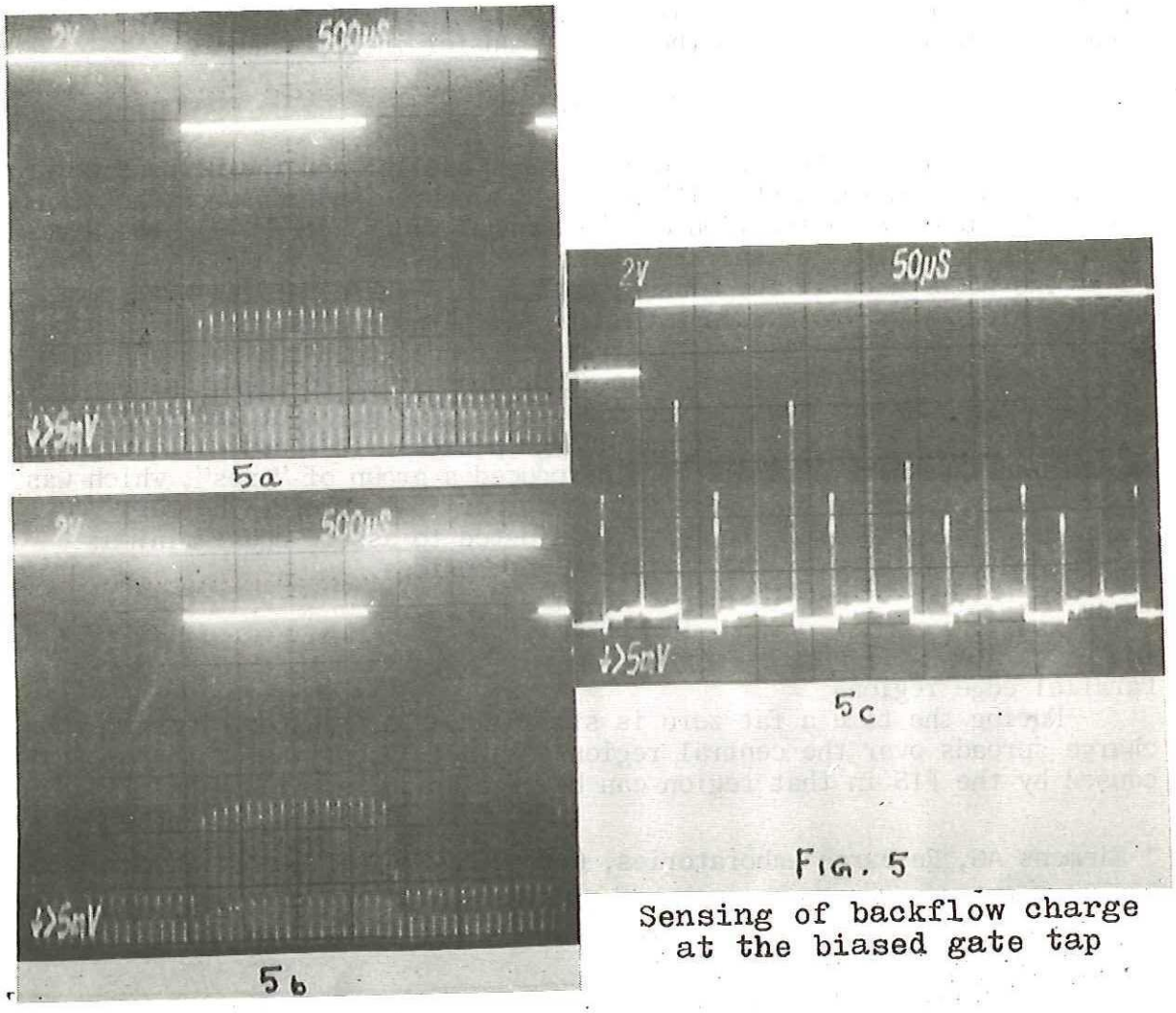

FIG. 5

Sensing of backflow charge at the biased gate tap