HARMONIC DISTORTION IN SPLIT-ELECTRODE CCD TRANSVERSAL FILTERS

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ABSTRACT

The effects of input distortion, non-linear depletion capacitance, and transfer inefficiency variations on the frequency dependence of distortion in CCD split-electrode filters are discussed. Theoretical results obtained from simulation of the CCD filter are supported by extensive distortion measurements on various surface- and buried-channel low-pass filters.

INTRODUCTION

Many possible applications of CCD split-gate transversal filters[1] (e.g. antialiasing filters for telephone codecs) impose stringent limits on the noise and distortion introduced by the filter. Distortion may be reduced by attenuating the input signal, but this brings the output signal closer to the noise level. A trade-off must thus be made at the design stage between distortion, output signal-to-noise ratio, and output circuit complexity.

Little attention appears to have been paid as yet to theoretical studies of the various distortion sources in the device, and distortion measurements in the literature have only been given at spot frequencies (e.g. 1, 2, 3). In this paper we first review our work on modelling these distortion sources and then show how practical measurements of harmonic distortion as a function of signal frequency support this modelling.

INPUT DISTORTION

The non-linearity of the conversion from input signal voltage to a train of signal charge packets at the input of a CCD inevitably introduces harmonic distortion. Typically this is mainly second harmonic at 40 to 50dB below the fundamental for input signal voltages of about 1V rms. Distortion introduced at the input stage appears as harmonic signal charge components superimposed on the fundamental. Such components are filtered by the frequency response of the filter at the frequencies at which they fall.

NON-LINEAR VARIATION OF SURFACE POTENTIAL WITH SIGNAL CHARGE

If a signal charge q_{sig} per unit area is clocked under a gate held at a constant voltage V_{GO}, the surface potential changes by $\Delta\phi_s$ and an image charge per unit area $\Delta q_G = C_{ox}\Delta\phi_s < q_{sig}$ appears on the gate. In fact we have previously shown[4] that

$$\Delta q_G = q_{sig} - C_{ox}\left(\sqrt{V_O^2+2V_OV'_{GO}} - \sqrt{V_O^2+2V_O(V'_{GO}-q_{sig}/C_{ox})}\right) = F_c(q_{sig},V'_{GO}) \quad \ldots(1)$$

where $V_O = q\varepsilon_s N_A/C_{ox}^2$, $V'_{GO} = V_{GO}-V_{FB}$, q is the electronic charge, ε_s is absolute permittivity of silicon, and C_{ox} is the oxide capacitance per unit area. The non-linearity of this relationship between Δq_G and q_{sig}, caused by the variation of the channel-substrate depletion capacitance, introduces harmonic distortion.

For a complete filter with N taps with areas $\{A^+_{G,i}, A^-_{G,i}; i = 1,N\}$

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connected to positive and negative busses the total output gate charge $\Delta Q_G = \sum(A^+_{G,i}-A^-_{G,i})\Delta q_{G,i} = \sum(A^+_{G,i}-A^-_{G,i})C_{ox}\Delta\phi_{s,i}$. If the input is pre-distorted to give $\Delta\phi_s = V_{in}$ (as with an idealised diode cut-off scheme) then the overall filter would be linear. Without this predistortion of the input charge packets, harmonic components of $\Delta\phi_s$ of magnitude obtainable from eqn. 1 are injected along the filter and are filtered by the frequency response of the filter in the same way as is input distortion.

NON-LINEAR VARIATION OF SURFACE POTENTIAL WITH GATE VOLTAGE

Practically, the detection of the image charge at constant gate voltage requires a virtual-earth trans-susceptance amplifier for each bus (fig. 1). To avoid the complexity and speed limitations of such a circuit, the sensing gate arrays may be isolated and connected to ground through a sense capacitor C_s (fig. 2). The variations of the surface potentials as signal charges move under the sensing phase are then capacitively coupled to the gate array to give an output voltage swing which may be monitored by a high impedance, low capacitance buffer. However, this gate voltage swing also modulates the surface potential, to give outputs ΔV^+_G and ΔV^-_G where[4]

$$C_s\Delta V^{\pm}_G = \sum A^{\pm}_{G,i}\Delta\phi^{\pm}_{s,i}C_{ox} = \sum A^{\pm}_{G,i}\left\{F_c(q_{sig,i},\ V'_{GO}-\Delta V^{\pm}_G) - F_c(0,V'_{GO})\right\} \quad ...(2)$$

In a filter structure, the full effect of the non-linear feedback caused by having $\Delta V^{\pm}_G$ on both sides of eqn. 2 is only felt at low frequencies ($<F_c/N$), when the filter is essentially a single split-gate with areas $\sum A^+_{G,i}$ and $\sum A^-_{G,i}$. At higher frequencies this distortion component is reduced as some of the $q_{sig,i}$ appear locally out of phase with the output ΔV_Gs and attenuate these voltage swings. This is confirmed by the theoretical results presented later, obtained by simulating the transfer of charge sinusoids along the CCD register and extracting harmonic components from the output calculated from eqn. 2.

BURIED-CHANNEL FILTERS[5]

Buried-channel filters typically have a more non-linear V_{ch}-q_{sig} characteristic than the $\Delta\phi_s$-q_{sig} relationship of a surface-channel device. (V_{ch} being the potential of the signal charge in the buried-channel.) However, since both the gate-channel and channel-substrate capacitances decrease with signal charge, the Δq_G-q_{sig} characteristic is in fact typically more linear than that for a surface-channel device on the same substrate according to one-dimensional analysis. For a rectangular doping profile with net surface doping N^*_D and with a gate voltage $V'_{GO} = 2q\varepsilon_s N^*_D/C^2_{ox}$ a perfectly linear characteristic is predicted and shallow gaussian profiles should also give good linearity. In practice, however, the distortion appears to be limited by two-dimensional spreading of the signal charge.

TRANSFER INEFFICIENCY EFFECTS[5]

The degradation of the effective tap weights of the filter by a transfer inefficiency ε causes a roll-off in the fundamental response in the passband and a reduction in the sharpness of the stopband ripple as the z-plane zeros leave the unit circle. If ε is independent of signal charge packet size, the system remains linear and no harmonic distortion is introduced. However, any variation of ε with signal charge modulates the transfer function of the filter and does induce distortion.

For a straightforward p-phase delay line, because any charge lost by one charge packet is gained by the next one, the distortion after Np transfers is proportional to $Np\ \sin(\pi F/F_c)$ where F is the frequency of the harmonic component. The constant of proportionality may be deduced by

evaluating the output explicitly at say $F_c/4$: for instance, for $\varepsilon = \varepsilon_{av}Q$ with input signal swinging between 0 and 2 this constant is approximately ε_{av}.

For an N-bit linear-phase low-pass filter the output and its harmonic components in the passband are roughly equal to that from an N/2-bit delay line. In the stopband, the output is no longer mainly from the main central lobe and the harmonic components falling there are attenuated by the stopband attenuation of the filter smoothed out by the transform of a ramp function due to $n\varepsilon$ steadily increasing along the filter. These effects have been confirmed by direct computer simulation of the action of the filter.

EXPERIMENTAL PLOTS

The filters investigated were 32-tap Parks-McClellan low-pass filters (F_p/F_c = 0.21875, F_s/F_c = 0.28175, δ_1 = 0.3dB, δ_2 = -49dB) fabricated at Honeywell SSEC as 2-poly, 4-phase, n-channel structures with the sensing-phase gates split by a channel-stop. Each gate was 900μm by 10μm giving an oxide capacitance of about 45pF for each gate array. The devices were clocked in 3½-phase mode with clock pulses swinging between 1V and 10V with 3.5V substrate bias. The gate bias voltage allowing for feedthrough was about 5.5V and the clock was 50kHz. Except where otherwise stated the phase-referred input scheme was used, with a 500mV rms input sinewave (250mV rms for buried-channel devices) at various bias levels. The fundamental and second harmonic components of the output were measured using a HP310A Wave Analyser over a range of input signal frequencies. The results as presented here are compensated to allow for the $\mathrm{sinc}(\pi F/F_c)$ roll-off due to sample-and-hold circuits before the output and to allow for the gain of the output differential amplifier.

a) Constant-gate-voltage sensing: The circuitry of fig. 1 holds the sensing gates at a constant potential V_{GO}, detects the image charge ΔQ_G, and gives an output voltage $\Delta Q_G/C_f$. Fig. 3 shows the frequency dependence of the second harmonic distortion for three signal bias levels. For minimal fat zero, the distortion mimics the fundamental response at the frequency of the harmonic: this is symptomatic of input distortion. As the input bias is increased to 1.7V, the distortion remains fairly flat at around 48dB below the fundamental - similar curves were obtained at biases from 1.2V to 2.7V. When the bias is increased to 3.2V, the signal is clipped at the input to again give input-type distortion. A diode cut-off input was also tried, with similar results (fig. 4) except that the largest bias charge now gave transfer-inefficiency-type distortion as the charge in the CCD was now limited by transfer down the CCD rather than by the input stage. Fig. 5 shows the dependence of distortion on bias level for this configuration. The three parts of the curves shown correspond to input distortion, depletion-capacitance-induced distortion, and transfer-inefficiency (overflow) distortion.

b) Gate-voltage-sensing: The simpler voltage-sensing output circuit of fig. 2 was also investigated. Figs. 6, 7, and 8 show the observed frequency dependence of output second harmonic using sense capacitances C_s of 28, 74 and 118pF (including 18pF interelectrode and stray capacitance). Also shown are theoretical predictions of this distortion. As expected, the harmonic peaks in the passband become more pronounced with decreasing C_s. The discrepancies between the theoretical and experimental curves for C_s = 28pF are thought to be due to imperfect splitting of charge at the channel splits caused by transients on the electrodes.

c) Buried-channel devices: A buried-channel version of this filter was also investigated, but it proved impossible to balance out the clock transients on the two gate arrays finely enough to prevent charge being hogged by one or the other. Nevertheless (fig. 9), 30dB of stopband attenuation could be achieved independently of charge bias level, and distortion was more than 40dB below the fundamental. A 200μm wide filter with a designed 26dB stopband attenuation proved less critical to align and achieved its desired response with harmonic 38dB down at optimum signal bias (fig. 10). Larger signal biases caused transfer-inefficiency-type distortion which correlates with that expected theoretically (fig. 11). The deviation of the fundamental response at about $0.3F_c$ is due to inprecise knowledge of the tap weights, the original specification having been lost.

A version of the 200μm wide filter with the splits defined by n^+ diffusions rather than channel-stop was also available: fig. 12 shows that the extra 'bucket-brigade' transfer inefficiency of such a design does indeed cause a marked passband roll-off.

CONCLUSION

We have briefly sketched out the reasons for the different characteristic frequency dependences of distortion caused by the various sources listed above. Our experimental plots of distortion vs. signal frequency have been correlated with this theory and this has demonstrated the usefulness of such plots in eliciting details of the operation of CCD split-gate filters.

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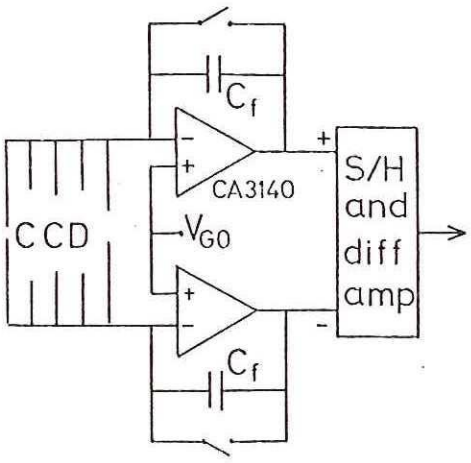

Fig. 1: Constant-gate-voltage output circuitry.

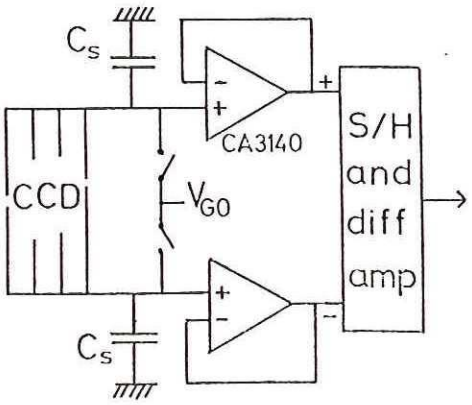

Fig. 2: Gate-voltage-sensing output circuitry.

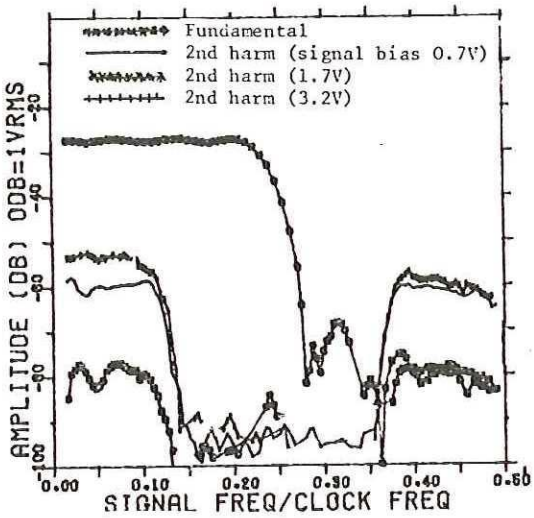

Fig. 3: Surface-channel filter: constant-voltage output, phase-referred input.

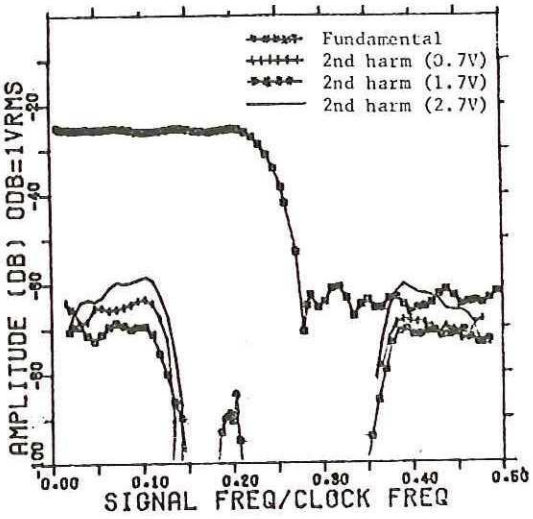

Fig. 4: Surface-channel filter: constant-voltage output, diode cut-off input.

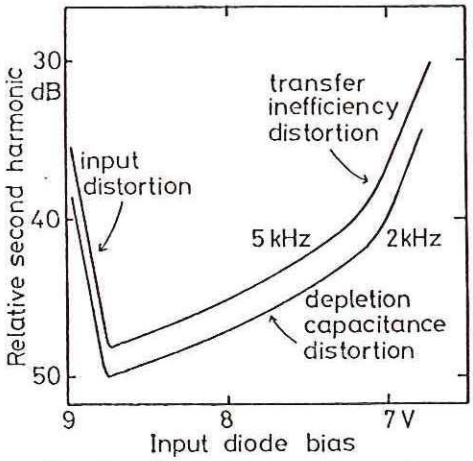

Fig. 5: Distortion vs. signal bias level from Fig. 4.

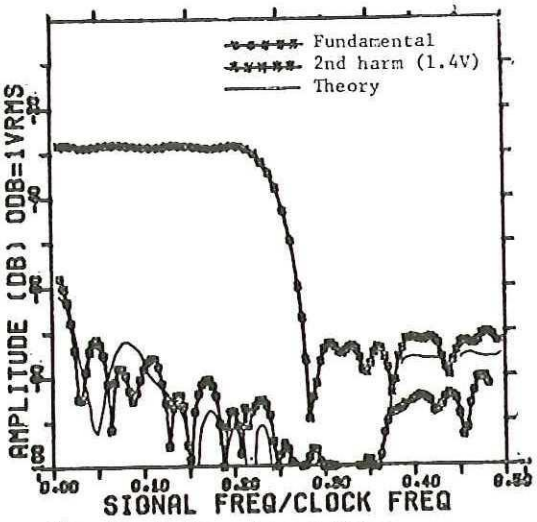

Fig. 6: Surface-channel filter, voltage-sensing output, C_s = 28pF.

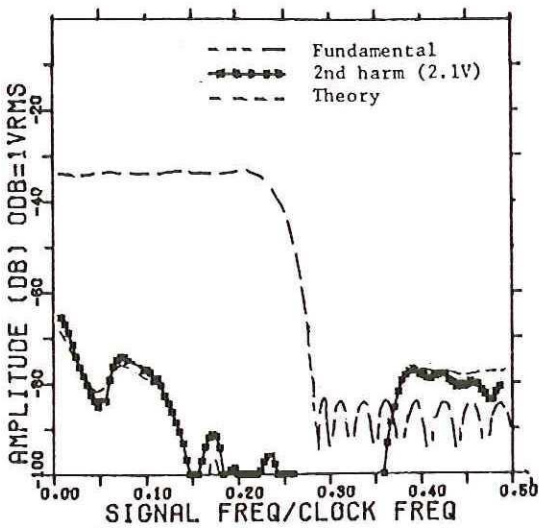

Fig. 7: Surface-channel filter, voltage-sensing output, C_s = 74pF.

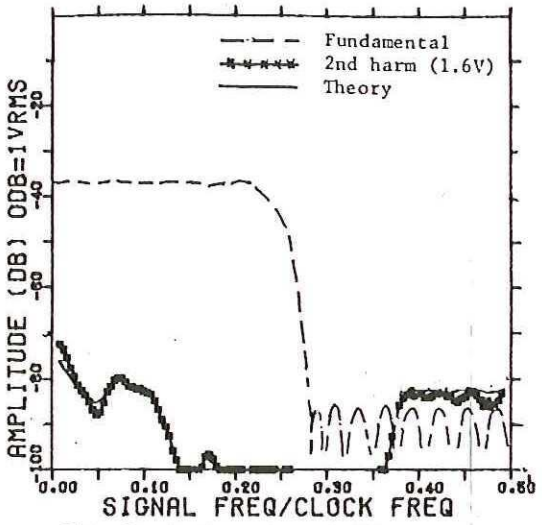

Fig. 8: Surface-channel filter, voltage-sensing output, C_s = 118pF.

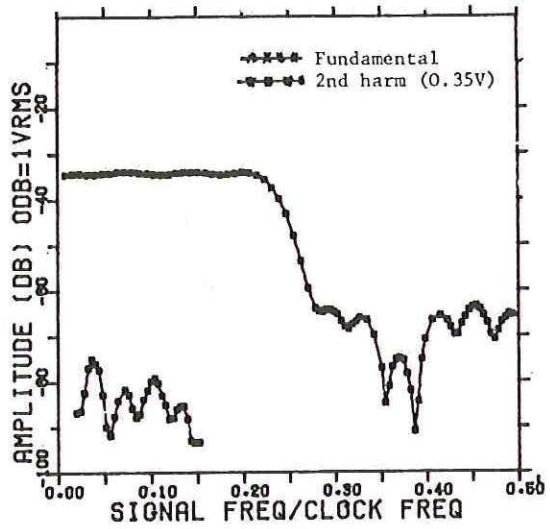

Fig. 9: Buried-channel filter (900μm). Constant-voltage output.

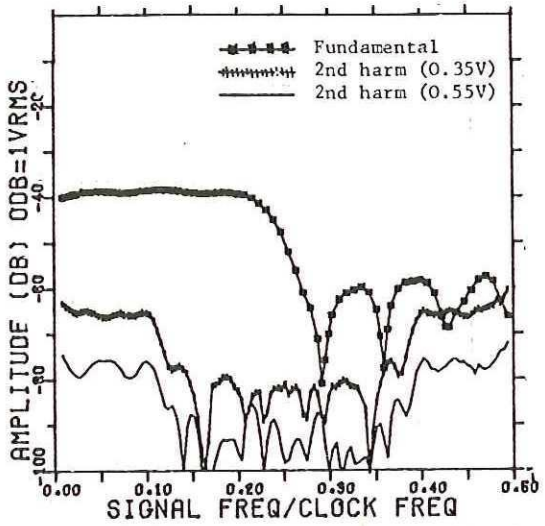

Fig. 10: Buried-channel filter (200μm). Constant-voltage output.

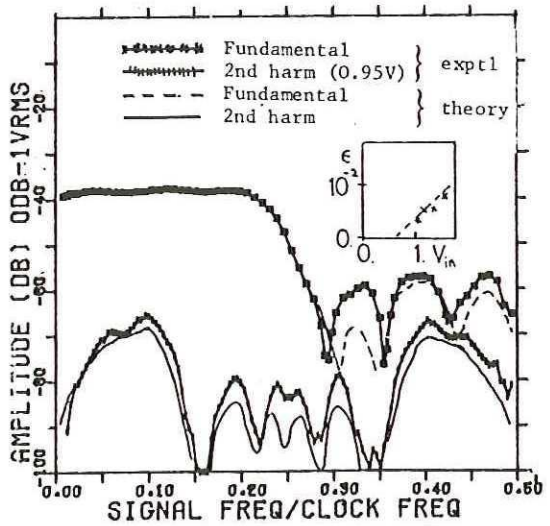

Fig. 11: 200μm buried-channel filter, constant-voltage output.

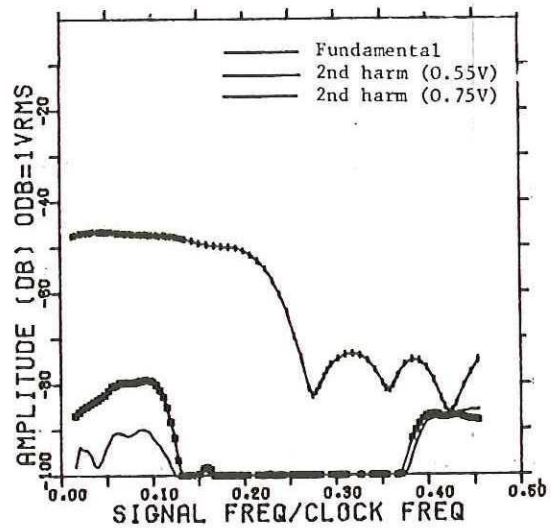

Fig. 12: 200μm buried-channel, conductively-coupled, gate-voltage-sensing, C_s = 50pF.