SURFACE POTENTIAL SENSING OUTPUT STAGE FOR CCDS

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ABSTRACT

A small diffusion next to a CCD electrode allows to sense nondestructively the surface potential. No additional reset clock is needed. Because of the dominating oxide capacitance linearity is good. The circuit is compatible with a standard double-polysilicon process used for high volume production of RAMs.

INTRODUCTION

Output stages to detect the charge packets transferred within a CCD are well known and documented. Besides new developments using operational amplifiers /1, 2/ on the same chip the most widely used output stage is still the floating diffusion output /3, pp 52/.

For analog signal processing one is interested in having a nondestructive readout, e.g. a regeneration stage /3, pp. 58/. Because of the diffusion under a gate this stage is not compatible with a standard double-poly process. The implementation with a floating gate amplifier having a reset clock /4/ has some critical timing requirements. The floating gate amplifier with a dc voltage at the gate /5/ leads to some design limitations - e.g. the electrode length of the bias electrode becomes fairly large.

The surface potential sensing output stage combines the positive features of both - the floating gate and the floating diffusion output stage. The main advantages are nondestructive readout with a minimum of distortion, a match of the charge size transferred within the CCD to the useful voltage range at the output, simplified clocking and compatibility with a standard process.

CIRCUIT DESCRIPTION

Fig. 1a gives a cross section through the surface potential output stage arranged in a 4-Phase-CCD. Here the sensing diffusion which in the actual circuit is located besides the sensing electrode $\emptyset_3^*$ is shown schematically underneath it. Below this cross section the surface potential and charge distribution for one period is depicted.

The electrodes $\emptyset_1$ - $\emptyset_4$ are clocked according to a 4-Phase-CCD but the sensing electrode $\emptyset_3^*$ is connected to a dc voltage. Assuming no charge is transferred through the CCD the potential of the sensing diffusion equals the surface potential under the sensing electrode $\emptyset_3^*$. This starting point shows Fig. 1b. Then a charge packet is transferred from gate $\emptyset_1$ to $\emptyset_2$ by going $\emptyset_2$ high and $\emptyset_1$ down. At the next time (fig. 1c) the charge packet is pushed under gate $\emptyset_3^*$. The variation of the surface potential is sensed via the small diffusion and is measured by the output transistor T1.

After sensing the charge packet is transferred under gate $\emptyset_4$ by going $\emptyset_4$ high. The sensing diffusion node is automatically reset to the

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surface potential under gate $\O_3^*$. This potential is determined by the dc voltage on gate $\O_3^*$. An equivalent circuit is shown in fig. 2.

To evaluate the sensitivity and linearity we computed the output signal $\Delta\O_S$ as a function of the signal charge Q.

In the ideal case without a load capacitance C_L the surface potential for a charge packet Q is given by the following equation /3/:

$$\O_S = V_G - V_{FB} - \frac{Q}{C_{ox}} - V_O + V_O\sqrt{1 - 2(V_G - V_{FB} + \frac{Q}{C_{ox}})/V_O} \tag{1}$$

with

$$V_O = - \frac{e\cdot N_A\cdot\varepsilon_{si}\cdot\varepsilon_O\cdot t_{ox}^2}{(\varepsilon_O\cdot\varepsilon_{ox})^2} \tag{2}$$

The output swing $\Delta\O_S$ is defined by the difference of the surface potentials with and without signal charge:

$$\Delta\O_S = \O_S - \O_{SO}\ . \tag{3}$$

For a charge packet consisting of a fat zero Q_{FZ} and a signal $\hat{Q}\sin\omega T_n$ the harmonic components can be obtained from eq. (3) using the approximate formula

$$1 - x = 1 - \frac{x}{2} - \frac{x^2}{8} \ \ldots :$$

$$\Delta\O_S = \frac{\hat{Q}\sin\omega T_n}{C_{ox}} - \frac{1}{K}\frac{\hat{Q}}{C_{ox}}\sin\omega T_n - \frac{1}{2}\frac{1}{V_O K^3}(\frac{\hat{Q}}{C_{ox}})^2\sin^2\omega T_n \ \ldots \tag{4}$$

with

$$K = \sqrt{1 - 2(V_G - V_{FB} + \frac{Q_{FZ}}{C_{ox}})/V_O}$$

Because the oxide capacitance C_{ox} of the sensing electrode is dominating distortions due to the nonlinear diffusion and depletion capacitances are minimized.

The additional load capacitance C_L decreases the output amplitude $\Delta\O_S$ because charge flows from C_L to the sensing capacitance $C_{ox}//C_D$. In this case the surface potential is described by

$$\O_{S1} = V_G - V_{FB} + \frac{Q-Q_L}{C_{ox}} - V_O + V_O\sqrt{1 - 2(V_G - V_{FB} + \frac{Q-Q_L}{C_{ox}})/V_O} \tag{5}$$

with

$$Q_L = C_L(\O_{S1} - \O_{SO}).$$

This leads to

$$\Delta\O_{S1} = \frac{\frac{Q}{C_{ox}}\left[1 - \frac{V_O}{\sqrt{V_O^2 - 2(V_G - V_{FB})\cdot V_O}}\right]}{1 + \frac{C_L}{C_{ox}}\left[1 - \frac{V_O}{\sqrt{V_O^2 - 2(V_G - V_{FB})\cdot V_O}}\right]}, \tag{6}$$

that is the output signal diminished by the small factor C_L/C_{ox}. The analysis outlined neglects that C_L is voltage dependent.

The realized circuit is shown in fig. 3. It consists of an 3-electrode input stage, two surface potential output stages at the begin and end of the delay line and at last a conventional floating diffusion output stage. Each of the 25 elements has a surface potential sensing diffusion.

The circuit was fabricated in the standard double-polysilicon locos process used for dynamic RAMs. The substrate doping was $1.5 \cdot 10^{15}$ cm^{-3}, the two oxide thicknesses were 80 nm and 140 nm.

MEASUREMENTS

To evaluate the performance static and dynamic measurements were conducted. The clock voltages were 10 V and 15 V due to the different oxide thicknesses.

First we have measured the transfer inefficiency of the surface potential sensing stage. It was determined by the leading edge losses of a string of "ones" at the last output. For a clock frequency of 100 kHz the values were $\varepsilon = 1.8 \cdot 10^{-3}$ without fat zero and $5 \cdot 10^{-4}$ with 20% fat zero. Compared with a normal delay line the losses are 5 times greater for the surface potential output stage.

Next we have investigated the linearity of the new output stage. To minimize signal dependent feedback through the gate-source capacitance of the output transistor this stage was operated as an inverter and not as a source follower.

The input-output characteristic was measured in a quasistatic manner varying the input level. The curves a, b in fig. 4 represent the values for the fill and spill and diode cut off input technique, respectively. In contrary to the fill and spill input the diode cut off input is inverting.

Also the harmonic contents a_{k_2} and a_{k_3} were determined by means of a signal analyzer. The input signal was kept constant at 0.2 of the maximum allowable range and the operating point was varied. The frequency of the test signal was 5 kHz. The overall distortion versus the operating point is shown in fig. 5 for the fill and spill and diode cut off input techniques. In both cases the attenuation of the second harmonic was more than 50 dB. The third harmonics are not included. They are more than 65 dB below the signal in the interesting range.

Besides the distortion the S/N-ratio is very important. Here we measured an absolute noise level of -85 dBm within a bandwidth of $\Delta f = 1.74$ kHz. The signal amplitude was -10 dBm. The noise level of the surface potential output stage was 10 dB below that of the floating diffusion output stage at the end of the test circuit.

CONCLUSION

The surface potential sensing output stage was presented. Good linearity, low noise level, nondestructive readout and the elimination of a special reset clock are main advantages. This output stage is especially useful for a tapped delay line.

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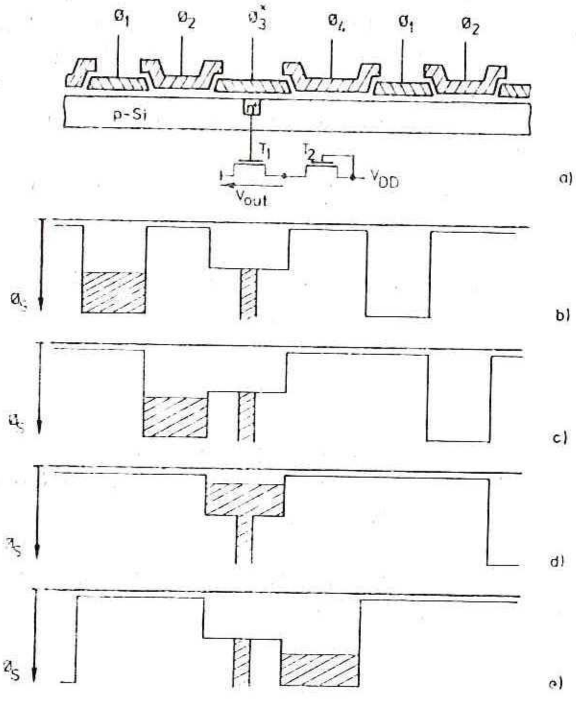
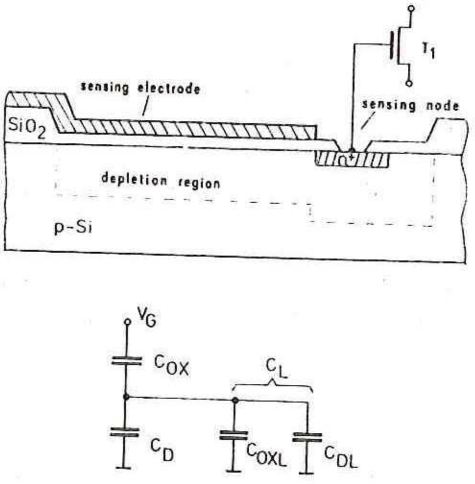


FIG 1. a) Cross section through a 4-Phase-CCD with a surface potential sensing output stage.
b-e) Surface potential and charge distribution.



C_{OX} oxide capacitance
C_D depletion capacitance
C_{OXL} oxide capacitance of the sensing node
C_{DL} depletion capacitance of the sensing node

FIG. 2. Equivalent circuit.

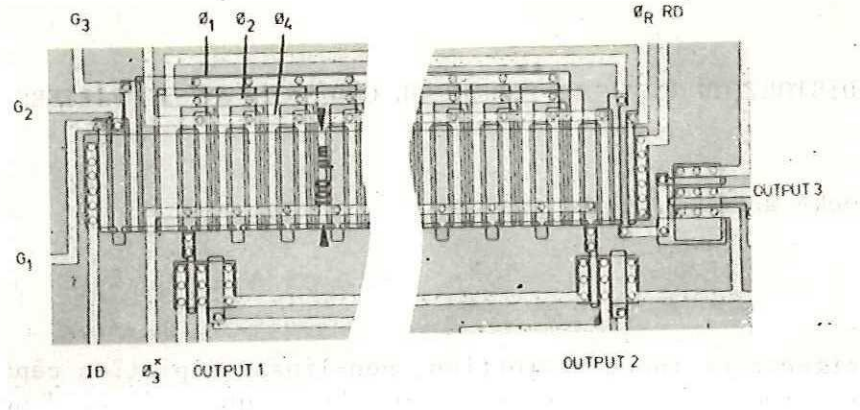


FIG. 3. Microphotograph of the realized circuit.

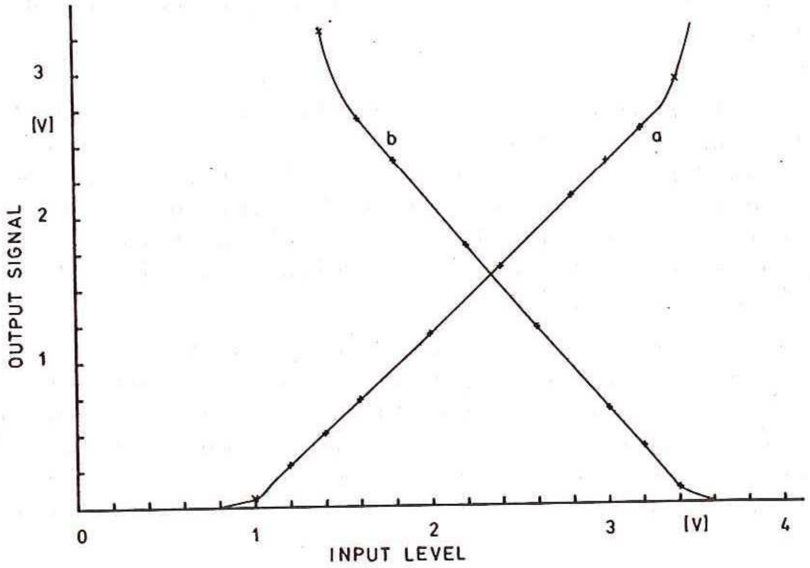


FIG. 4. Measured input-output characteristic for (a) fill and spill and (b) diode cut off input technique.

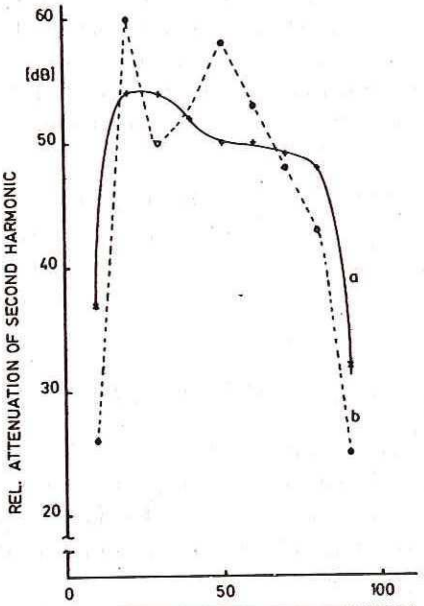


FIG. 5. Measured overall second harmonic distortion versus operating point for (a) fill and spill and (b) diode cut off input technique.